Simulation, Design, and Fabrication of Thin-Film Resistive-Gate GaAs Charge Coupled Devices

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ABSTRACT

Computer simulation of high-speed Gallium Arsenide Charge Coupled Devices is performed using an established two-dimensional semiconductor device simulation program. The effect of active layer thickness on the Charge Transfer Efficiency (CTE) and the dynamic range is investigated using different active layers. Also, different gate architectures are compared for optimum dynamic range and compatibility with GaAs MESFET technology. Both Capacitive Gate CCD (CGCCD) and Resistive Gate CCD (RGCCD) are considered. Measured performance of fabricated GaAs CCD's is compared with modeled results.

I. INTRODUCTION

We are developing high speed GaAs CCD's for the capture of single-event electro/photo-transients in scientific experiments. We have adapted the two dimensional device simulation program BAMBI (Basic Analyzer of Mos and BIpolar devices) [1] for GaAs devices. BAMBI is a two dimensional numerical solver for Poison's equation, the continuity equations for electrons and holes, and the two corresponding current relations.

The models for the doping concentrations N_d and N_a, carrier mobilities μ_n and μ_p, the generation and recombination rates, surface recombination velocities and the clocking sequence are supplied as external subroutines. At present a simple model for electron mobility is being used which takes into account the lattice scattering at 300K. and velocity saturation. The lattice scattering model uses a power law whose coefficients are obtained by fitting experimental mobility values [2].

II. DEVICE STRUCTURE AND MODELING RESULTS

In a 4-phase CCD cell, the n-type active layer is first depleted by applying a positive bias via an ohmic contact. The interface of the n-GaAs active layer and semi-insulating GaAs substrate is modeled as a reverse-biased p-n junction [3]. The formation of the potential well under the biased gate is observed. An excess electron-hole pair is then generated and collection of electrons into the potential well is simulated in transient mode. The transfer of the charge packet is observed under various clocking conditions. The CTE and the maximum speed of operation are determined as a function of active layer thickness.

Figure 1 shows a simple 4-phase GaAs CCD cell. The 4 phases of the cell are isolated from the ohmic contact, V_s, by an isolation gate, IG_1. The active layer was varied from 0.8μm to 1.2μm. Figure 2 shows the clock sequence. The formation of the potential well under gate 2 before any excess ehp generation is shown in Figure 3. In this case the active layer is 0.8μm thick. After the generation of excess carriers, the electrons are collected in the potential well under gate 2, as shown in Figure 4. The dynamic range is estimated by varying the generation rate up to the point where electrons cannot be contained by a single phase. Figure 5 shows the electron charge packet for a 0.8μm active layer CGCCD with a doping level of $1x10^{16}cm^{-3}$ in such a situation where the charge starts to spill to the adjacent gate. The dynamic range is about $1.2x10^7$ electrons (per cm of gate length) for a 2V peak-to-peak clock. The dynamic range of a 1.0μm active layer CCD for identical clocking is about 35% greater and for 1.2μm about 75% greater. This translates to a maximum well capacity of about 2.4, 3.2 and 4.2 ($x10^3$) electrons, respectively, for 20μm wide gates. If the active layer becomes too thick, however, V_s must be correspondingly increased so that the layer is fully depleted (an undesirable

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situation, as it creates a potential slope towards the source contact). On the other hand, if the active layer thickness is comparable to the inter-electrode gap, electrons get trapped in potential wells of the gap [4].

The maximum charge transfer frequency is found by transferring a small charge packet from phase 2 to phase 3. For the 0.8μm active layer, a charge packet of about $2.3x10^4$ electrons/cm is transferred from phase 2 to phase 3 under varying clock frequencies. The transferred charge packet is then counted under gate 3 and the frequency at which the CTE drops below 0.999 is taken as the maximum transfer frequency. The charge packet of Figure 4 is shown after undergoing this transfer to gate 3 in Figure 6. For this case, the maximum transfer frequency is found to be about 555MHz. For the 1.0μm active layer case, the maximum transfer frequency is about 3.3GHz. This is as expected, due to the higher fringing field for the thicker active layer device. The above numbers are conservative, in that for larger charge packets the self-induced fields are higher.

Both CGCCD's and RGCCD's [5,6] have been simulated. For the RGCCD case, the cermet (a thin film of resistive Cr/SiO alloy, forming Schottky contacts with GaAs layer) [7] is simulated using a series of gates having distributed potentials. The device cross-section of a 0.2μm active layer RGCCD is shown in Figure 7; the clock sequence is shown in Figure 8. The tendency of electron trapping is found to be more pronounced for a thinner active layer than for thicker layers. The simulation results showed no electron trapping in the inter-electrode gap when a cermet layer is used. For our structure, the maximum transfer frequency is about 100MHz. Figures 9 and 10 show the transfer of charge between two gates of the above CCD.

III. EXPERIMENTAL RESULTS

The modeling results of both CGCCD's and RGCCD's were compared with the measured performance of such devices fabricated at Lawrence Livermore National Laboratory. The experimental RGCCD has a 0.2μm active layer thickness and a doping level of $3x10^{17}cm^{-3}$. The gates are 1.75μm by 20μm. The inter-electrode gap is 1.25μm. A cermet layer is deposited covering both the inter-electrode gaps and the Cr/Au gate electrodes. The simulated maximum clocking speed (at reasonable CTE) is about 100MHz. The experimental measurements of the fabricated GaAs RGCCD generally agree with this value. Degradation of CTE is measured as the clock frequency is increased. This can be seen in Figures 11 and 12 which show measured input and output signals at 20MHz and 290MHz, respectively.

IV. CONCLUSIONS

We have seen that both dynamic range, and to a greater extent, CTE, decrease with decreasing active layer thickness. In general, thicker active layer CCD's have higher dynamic range and faster operating frequencies. Compatibility with established GaAs MESFET technology requires thinner active layers. This can be partially achieved by balancing dynamic range and CTE with active layer thickness and using RGCCD's. The correlation of simulation results, obtained using a 2-dimensional device simulator, provides a powerful means to optimize the architecture of the GaAs CCD cell for maximum CTE and dynamic range.

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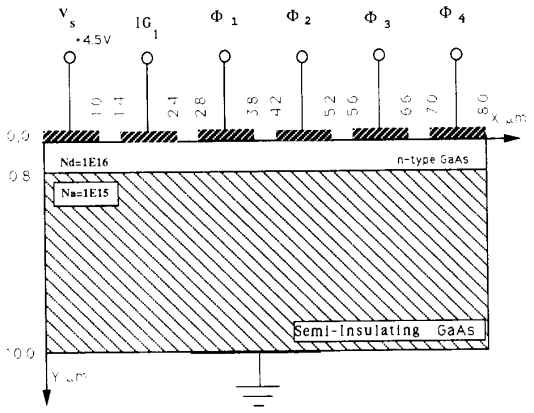

Figure 1: The cross-section of a 0.8μm channel 4-phase GaAs CGCCD showing the simulation domain.

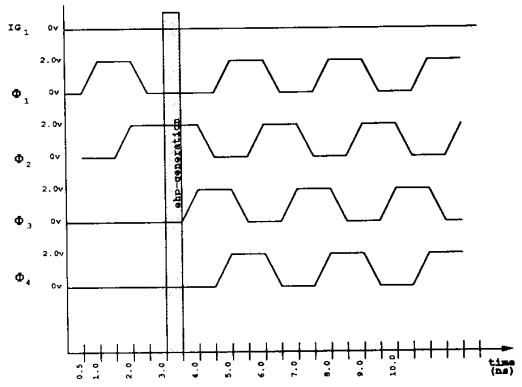

Figure 2: The clocking sequence used for the CGCCD. Also note the electron-hole pair generation between 3.0 and 3.5ns.

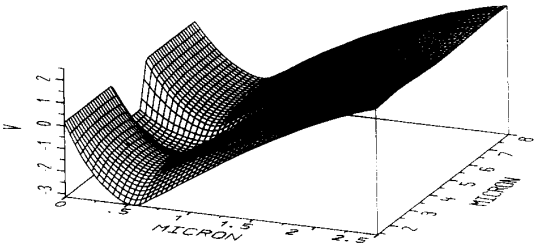

Figure 3: Electrostatic potential (inverse) showing the empty potential well under gate 2. Only part of the total cell is shown.

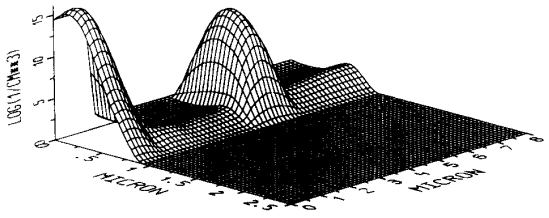

Figure 4: The collected electron charge packet under gate 2 at time t=3.5 ns.

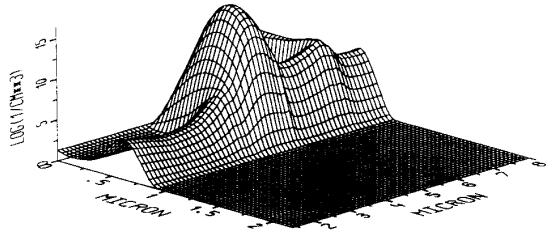

Figure 5: Situation where the charge starts to spill to the adjacent gate. The dynamic range is determined by varying the generation rate up to the point where electrons cannot be contained by a single phase.

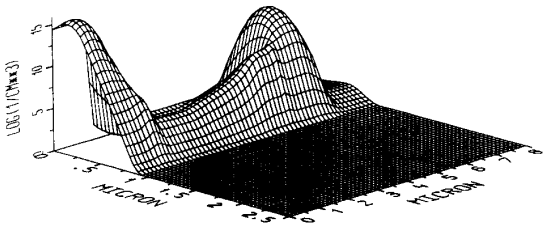

Figure 6: The electron charge packet of Fig. 4 after 99.9% transfer of charge from gate 2 to gate 3 at time t=4.5 ns.

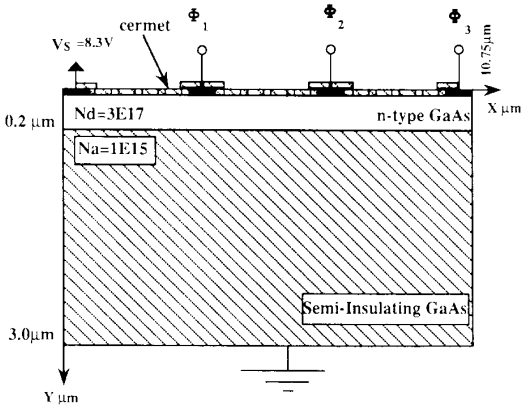

Figure 7: The cross-section of a 0.2μm channel 3-phase GaAs RGCCD showing the simulation domain.

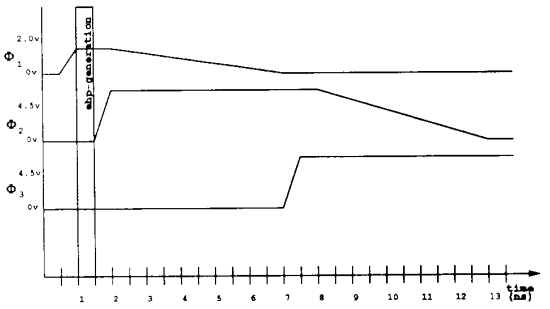

Figure 8: Clocking sequence used for the 0.2μm active layer 3-phase RGCCD. Excess carrier is generated between 1.0 and 1.5ns.

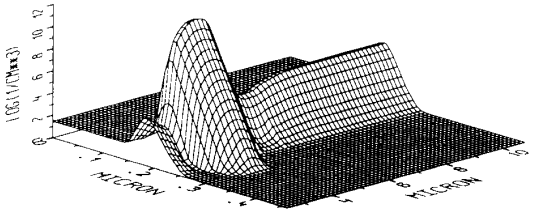

Figure 9: Collected electron charge packet under gate 1 at time t=1.5 ns

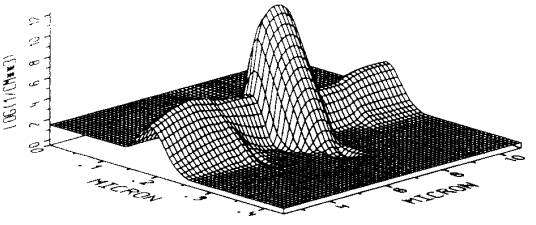

Figure 10: The Electron charge packet of Fig. 9 after 99.9% transfer of charge from gate 1 to gate 2 at time t=7.0 ns

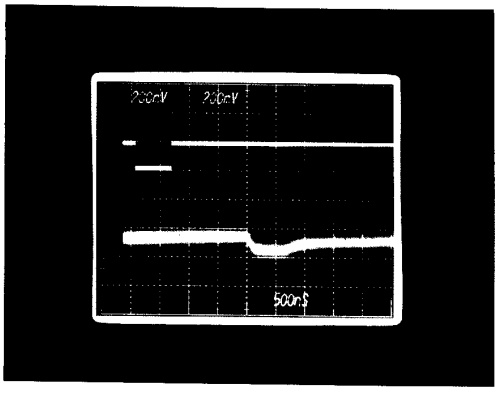

Figure 11: Measured electrical input and delayed output signal, with 20MHz clock, for a 0.2μm active layer 16 cell RGCCD.

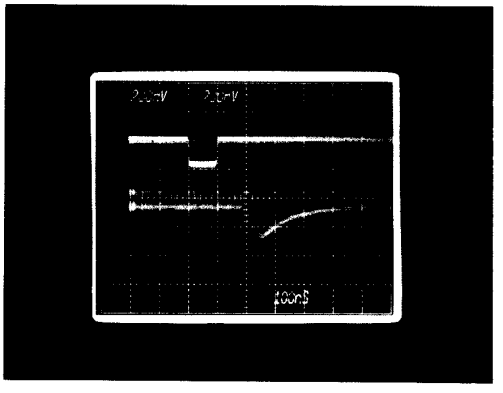

Figure 12: Measured electrical input and delayed output signal at 290MHz for the same CCD of Fig.11, showing distortion of signal charge at higher clock frequency.