Transient spectroscopy of deep levels in thin semiconductor films

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Characterization of deep levels in thin-film semiconductors by capacitive pulse transient spectroscopy has been analyzed and verified by measurement. Numerical calculations show that highly resistive thin films create a degradation of signal and possible sign inversion of the signal. Experiments on silicon on insulator and molecular beam epitaxy GaAs Schottky barrier capacitors verify the calculated signal deviation.

Capacitive pulse transient spectroscopy, or deep level transient spectroscopy (DLTS) is an established characterization technique for measuring concentration, activation energy, and capture cross section of midgap traps in semiconductors.[1] Although DLTS and its variants has been successfully used to characterize bulk elemental and compound semiconductors, certain problems have been noticed in measuring thin-film semiconductors by capacitive DLTS. This is particularly true in low-doped films where non-negligible series resistance with the capacitive structure being measured occurs; the result is a significant alteration of the quality factor (that is, from purely capacitive) of the overall structure being measured by the instrument or bridge. Examples of where this problem have been seen are compound semiconductor layers deposited by molecular beam epitaxy (MBE) on semi-insulating substrates[2] and silicon on insulator (SOI) layers.[3] Although some relief from the series resistance problem is found by using current DLTS,[4] the defect nature of the thin-film semiconductor layer to be tested is altered in the process of making the current DLTS test device: the film must be made highly doped before functional test devices can be fabricated.

This communication shows from analysis and experimental measurements how capacitive DLTS measurements on resistive structures can lead to erroneous DLTS signals. It is proposed that an understanding of the effect of quality factor within the test structure can be used to develop a DLTS signal analysis method which will provide numerically correct values of activation energy, concentration and capture cross section even from these distorted signals.

The effect of a lateral series resistance, R_s, on DLTS capacitance transients was investigated. Although this resistance has a negligible effect on the charge kinetics within the device itself, it does significantly alter the output signal of the capacitance bridge circuit. Capacitance meters used for DLTS measurements are typically based on the Boonton 71C bridge. For this experiment a Boonton 72BD capacitance meter was used. The bridge circuit of this meter is shown in Fig. 1. The output reading from such a capacitance bridge with quiescent components balanced is

$$C_{pi} = C_{si} \frac{(1-\omega^2 R_s^2 C_{sQ} C_s)}{(1+\omega^2 R_s^2 C_s^2)} (1+\omega^2 R_s^2 C_{sQ}^2)^{-1}, \quad (1)$$

where ω is the meter frequency and C_{pi} is normally interpreted as the equivalent incremental parallel capacitance of the test device. In this expression, C_{si} and C_{sQ} are the incremental and quiescent values, respectively, of the series capacitance. The instantaneous capacitance, C_s, must satisfy the relationship, $C_s = C_{si} + C_{sQ}$. The quality factor is defined by the expression, $Q = \omega R_s C_s$. Although approximations have been used by other investigators, the above expression has no restriction on the magnitude of the incremental capacitance, C_{si}. For devices incorporating large series resistance and incremental capacitance, it is more accurate to use the complete expression given in Eq. (1).

Numerical simulations of DLTS transients were carried out for $Q \ll 1$, $Q = 1$, and $Q \gg 1$. Both single and double trap levels were simulated. The results for the single trap case ($\Delta E = 0.28$ eV) are shown in Fig. 2(a). The double trap results ($\Delta E = 0.18$ and 0.29 eV) are shown in Fig. 2(b). The simulation results showed that the series resistance effects could be considered in three categories. (1) For $Q \ll 1$, Fig. 2 shows that the meter measurements are accurate and the sensitivity is good for both single and double traps. (2) For $Q = 1$, non-negligible errors occur; the measured capacitance transient is non-exponential and the system sensitivity is poor. It is important to notice that both direct and inverted peaks are found even for the single trap case in Fig. 2(a). Likewise, two direct peaks and an inverted peak are found for the case of Fig. 2(b). An inverted peak is normally interpreted as a minority carrier trap but, in producing Fig. 2, only majority-carrier traps were considered (i.e., Schottky barrier devices). Consequently, the inverted peaks in Fig. 2, which represent the normalized DLTS signal that would be obtained from devices having a large series resistance, are physically unrealistic. (3) For $Q \gg 1$, the spectrum is com-

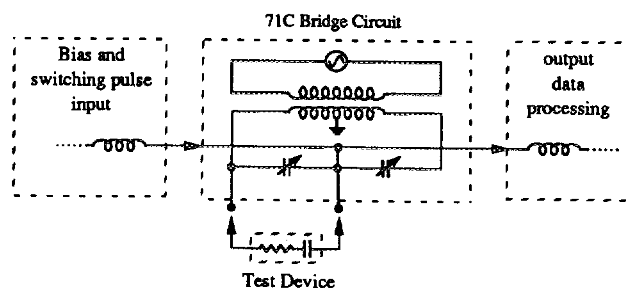

FIG. 1. Basic circuit structure for the 72BD capacitance meter.

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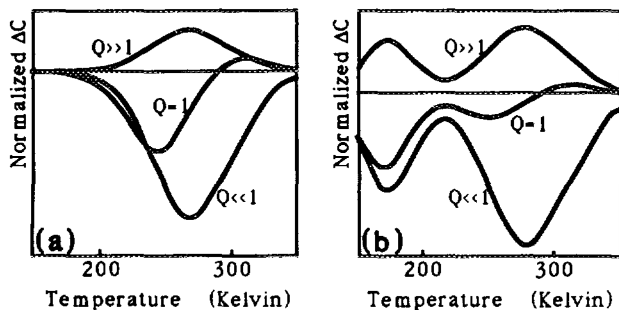

FIG. 2. Simulated DLTS signal for varying series resistance values. (a) Single trap. Rate window described by $t_1 = 0.1$ s, $t_2 = 1$ s. (b) Two trap. Rate window described by $t_1 = 0.1$ s, $t_2 = 1$ s.

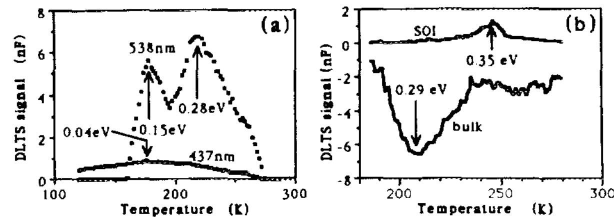

FIG. 3. DLTS spectra. (a) GaAs samples: $t_1 = 4$ ms and $t_2 = 8$ ms. (b) SOI and bulk Si diodes: $t_1 = 10$ ms and $t_2 = 30$ ms.

pletely inverted both for single and double traps. As long as Q is very much greater than 1, the locations of the trap peaks in the DLTS signals will be correct but with a degraded S/N ratio. However, there may exist certain ranges of values for Q such that even though the peaks are inverted, their position along the temperature axis may not yield the true energy levels for the traps.

The DLTS technique was applied to bulk silicon on insulator (SOI) and thin layers of GaAs formed on semi-insulating materials. A Boonton 72BD capacitance meter and a digitizing oscilloscope were used to measure and store the capacitance transients, respectively.

The GaAs material used in this work was grown on top of a semi-insulating material by MBE. The film thicknesses are 538, 437, and 200 nm with 10^{16}, 10^{17}, and 10^{17} per cm^3 donor concentration, respectively. Schottky diodes are fabricated on these thin films. The area of the depletion capacitor is 7.2×10^{-5} cm^2. Measured saturation current densities are less than 2 mA/cm^2; the ideality factors are between 1.1 and 1.2.

1 Ω cm bulk and 5 Ω cm (1 μm thick) SOI *n*-type wafers are used for the bulk and SOI samples, respectively. An interdigitated structure[5] is used to minimize the reverse-biased PtSi Schottky diode's series resistance. Measured reverse saturation current densities are < 0.2 mA/cm^2; the ideality factors for the bulk and SOI diodes are 1.2 and 2.5, respectively. The area is 7.5×10^{-3} cm^2.

The capacitance of the depletion region and the resistance of the neutral region of these thin-film diodes form a distributed RC network represented to the first order as a capacitor in series with a resistor. The room temperature Q measured by the Boonton 75 impedance bridge under 1.5-V reverse bias for the 538- and 437-nm GaAs samples is 0.83 and 1.34, respectively. The Q of the SOI sample, at a bias of 3 V, is 1.5.

A majority carrier pulse with 1-V reverse bias is applied to the 200-nm-thick GaAs sample. The DLTS spectra show no traps in this sample above the detection limit of our apparatus. Larger reverse bias cannot be applied to this thin device because it will fully deplete the GaAs layer and make the DLTS measurement invalid.

A majority carrier pulse with 1.5-V amplitude and 20-ms pulse-width is applied to the 538- and 437-nm-thick samples. The DLTS spectra are shown in Fig. 3(a). Two traps (0.15 and 0.28 eV) are observed from the 538-nm sample and only one trap (0.04 eV) is observed from the 437 nm sample. It is not clear why the samples with different thicknesses appear to have different trap levels.

A majority-carrier pulse with reverse bias of 3 V and a pulse-width of 20 ms is applied to the SOI and bulk Schottky diodes. The DLTS signals are shown in Fig. 3(b). Since the SOI and the bulk materials are made by different techniques, they should have different trap levels. Thus, the position of their DLTS peaks should not be compared with each other.

Positive DLTS signals are observed from the GaAs and SOI samples even though no minority-carrier pulse is applied. A positive signal is usually interpreted as a minority-carrier trap, however, such a conclusion is not realistic from these majority-carrier devices. Nevertheless, in the device tested here, a positive peak is reproducibly observed. We conclude, therefore, the positive peak is observed because, according to Eq. (1), C_{pi}/C_{si} is negative for Q greater than 1, such that the measured transient is being reversed due to the sample's series resistance. Furthermore, adding an external 2- and a 5-kΩ resistor in series with the SOI and the GaAs samples, respectively, would not reverse their transients although they do reverse the transient of the bulk sample; therefore, it can be concluded that the sign of the SOI transient is reversed from the start. The positive peaks for the SOI and MBE samples should therefore be interpreted as majority carrier traps.

For the 538-nm GaAs sample, inverted signals are found to occur for values of Q less than the predicted value $Q > 1$, an observation also made by Broniatowski et al.[6] The discrepancy may be due to the neglect of shunt resistance in the series RC equivalent circuit, and/or different meters being used to measure the transient and the Q. The DLTS peak is also shifted because the Q varies as the resistivity changes with temperature and the capacitance changes during the transient. Consequently, the trap activation energy cannot be determined with precision because the Arrhenius plots for emission rate depend on the accurate determination of peak position. The trap density cannot be calculated using the techniques normally used for DLTS measurements on bulk materials because of the inversion of the transient.

It has been shown that distorted capacitive DLTS signals can be measured in device structures which have any series resistance significant enough to alter the quality factor of the device under test. These distortions can be explained from an analysis of the circuit configuration of the test device and the capacitive bridge circuit used in the measurement

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instrumentation. The distortions are such that signals are measured which, using established calculation techniques for bulk DLTS analysis, give erroneous values for activation energy, concentration, and capture cross-section for the mid-gap traps being measured. It is also shown that for some conditions nonexistent traps may be inferred from the measurements. An understanding of the effect of the quality factor of the test device structure, as well as the circuit configuration of the instrumentation being used, may make it possible to derive correct trap parameter values from these distorted signals.

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