Highly Selective Etch Stop by Stress Compensation for Thin-Film BESOI

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A limiting issue in the application of the BESOI technique to whole wafers is the final film thickness nonuniformity, which typically totals approximately 40nm using etch-back techniques presented to date. Such variation makes BESOI impractical for thin-film SOI (eg. ≤ 300 nm) and applications to fully-depleted MOS. The etch-back process is a major contributor to the final film thickness nonuniformity[1]. We demonstrate here a reliable technique for formation of highly selective etch stops for BESOI.

Typical BESOI etch stops are formed by implanting or depositing boron p+ layers over which an epitaxial layer (the final SOI layer) is grown. If the peak concentration of the p+ layer is 10^{20} cm^{-3}, the selectivity of KOH etchants reaches approximately 100, and EPW about 20% higher[2]. Higher boron concentrations make the etch stop significantly more selective (eventually reaching approximately 5000 when etching with KOH), however, above 8 x 10^{19} cm^{-3} the tensile stress induced in the p+, due to the smaller atomic number of boron, causes the formation of misfit dislocations in the SOI epilayer.

We demonstrate here a highly selective etch stop of 2 x 10^{20} cm^{-3} boron concentration, stress compensated by introducing Ge (a high atomic number species). The $Si_{1-x-y}Ge_xB_y$ etch stop is selective through the reduction of the passivation potential in KOH to a point where negligible etching occurs. The stress compensation gives the wafer surface an exact Si lattice constant. Epitaxial layers are grown over this etch stop without misfit dislocations.

Experimental samples have been prepared by two methods: (1) low-energy Ge implantation to amorphize the device wafer surface before B or BF_2 implantation and RTA[3], followed by low-temperature (850° and 950°C) epitaxy, and (2) *In-Situ* growth of the $Si_{1-x-y}Ge_xB_y$ etchstop and the ensuing undoped epitaxial layer by low-temperature RT-CVD[4]. Figure 1 depicts the film system in the device wafer before bonding. The wafers are then bonded and etched back by the typical process[5] to complete the BESOI. Submicron epilayers have been grown on both types of etch stop. The results using both techniques will be contrasted. Figure 2 shows spreading resistance (SRP) concentration profile data from an implanted sample. Although the SRP data suggests a boron peak at less than 10^{20} cm^{-3}, it is found that the stress compensation causes the calibration standard to be in error for $Si_{1-x-y}Ge_xB_y$ material. SIMS measurements verified that the 2 x 10^{20} cm^{-3} peak concentration of boron is indeed retained.

CH2891-0/90/0000-0145$01.00

The selectivity in etching is caused exclusively by the high boron concentration. The low Ge content (≈ 3%) in the layer does not measureably alter the etching characteristics in the silicon; therefore, the chemical process of this etch stop differs significantly from techniques using a Si-Ge "strain layer" as the etch stop (typically ≥ 30% Ge)[6]; the selectivity of this etch stop is correspondingly in excess of 30 times higher and does not require expensive MBE fabrication processing. The concentrations of Ge and B are high enough, however, that simple estimates by atomic radius models are incorrect in predicting the Ge:B ratio at which exact stress compensation occurs. Measurements by x-ray rocking curve spectroscopy are used to verify, experimentally, the residual stress. In agreement with findings in Si membrane experiments[7], the correct ratio appears to be closer to 3.5 rather than 5.7 as predicted by the models.

The results of experimental stress measurements, SIMS, SRP profiles, and defect analysis of both the implanted and *in-situ* etch stop methods will be shown. It is believed that this technique can be incorporated into normal IC process lines to make the BESOI technique practical for thin-film SOI formation. The authors gratefully acknowledge the assistance of Prof. M. C. Ozturk of North Carolina State University in providing the high-current Ge implants.

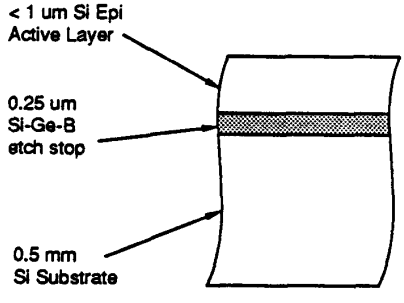

Figure 1: Device wafer films, before bonding and etch-back

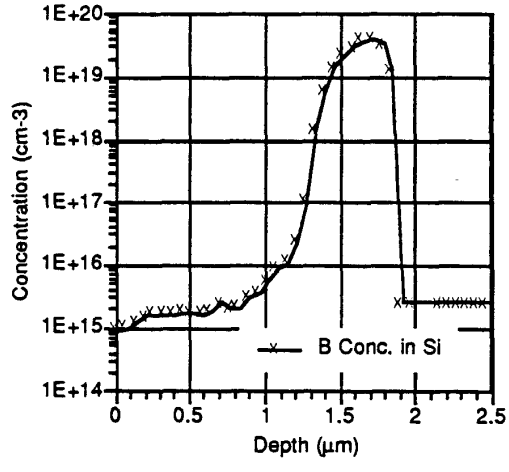

Figure 2: Concentration Profile From SRP Data. Calibrated to B in Si without Ge

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