Film Uniformity in Bond and Etch-Back Silicon On Insulator (BESOI)

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Bond and Etch-Back SOI (BESOI) has been proposed [1] as a variant on the established DI technology (used predominantly by the power electronics industry) which has application to *thin-film* electronics presently targeted by SIMOX, ZMR, FIPOS, and other SOI materials techniques. BESOI is made by epitaxially growing a high-resistivity layer on a low-resistivity substrate, oxidizing the epilayer, and then thermally bonding a second oxidized wafer (the handle) onto the oxidized epilayer. The SOI film is then formed by etching the original substrate up to the epilayer, leaving the handle as the new substrate. The major incentive for using this technology is the thermal Si/SiO_2 interface between the SOI layer and the insulator. It has been shown that BESOI can have minortity carrier lifetimes and MOSFET operating characteristics comparable to bulk values [1]. Major problems with BESOI technology include non-uniform bonding (formation of voids between the handle and epilayer oxides) and non-uniform SOI film thickness. This presentation addresses the film thickness problems and techniques whereby these problems can be minimized.

The etch-back technique relies on the type-sensitive anisotropy of the etchant . In the simplest case, certain well-known wet chemical formulations [2] have been used which demonstrate a reasonable selectivity between the original substrate ($N_A \approx 10^{18}$ cm^{-3}) and the grown epilayer ($\approx 10^{15}$ cm^{-3}). The surface variation using this technique will exceed 75nm; this is reasonable for thick film SOI, eg. for lateral power switches, but is unacceptable for ranges of MOSFET device application (0.1-0.5μm film thickness). The film thickness variation is due largely to the sensitivity of the etchant selectivity to variations in epilayer strain resultant from fluctuations in doping concentration incorporated during the growth process, either due to out-diffusion or mechanisms of autodoping. Measured results from BESOI samples with epilayers deposited at various temperatures (≥800°C) demonstrate this phenomenon.

The fluctuation in film thickness can be reduced by incorporating an *etch stop* layer on the original substrate surface before epilayer growth. The simplest etch stop is a B diffusion layer (surface $N_A \approx 10^{19}$cm^{-3}) on a 5+Ω-cm substrate. The original substrate is thinned to ≈20μm using a standard isotropic Si polish and a concentration-sensitive etchant [3,4] is used which stops in the highly-doped layer. A slow isotropic chemical polish is then used to remove the etch stop. Samples made using several variations of the etch stop technique are demonstrated.

Finally, film uniformity varies strongly according to the etch-back formulation chosen. A comparison of etch-back chemistries, both electro-activated and non-electrochemical, will be presented. A novel technique using etch stop anodization will also be demonstrated. Recommendations for obtaining films useful in analog and digital CMOS applications will be discussed.

[1] J. B. Lasky, *Appl. Phys. Lett.* **48** (1), 78 (1986)

[2] H. Muraoka, T. Ohhashi, and Y. Sumitomo, in *Semiconductor Silicon 1973*, H. R. Huff and R. R. Burgess, Ed.s, The Electrochemical Society (1973), p. 327

[3] J. B. Price, *Ibid.*, p. 339

[4] A. Bohg, *J. Electrochem. Soc.***118**, 401 (1971)