Low Voltage Silicon Field Emitters With Gold Gates

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Gated silicon field emission cathodes have been fabricated by the self-aligned lift-off method. The addition of a gold gate not only simplifies processing, but also facilitates easy packaging and allows the placement of many devices on a single chip. Currents have been measured on 2500 tip arrays which follow Fowler-Nordheim characteristics over several decades. Field emission from these arrays begins at less than 20 V. Low frequency noise measurements exhibit spectral power density indices from 1.18 to 1.55. Single tip and small array devices are being characterized.

Introduction

Low voltage operation is a desirable goal for most vacuum microelectronics applications. The primary method of achieving this is by minimizing the tip to gate spacing. Silicon field emission devices with very low operation voltages can be fabricated using the common cap lift-off fabrication method.[1,2,3] This method provides a means of fabricating cathode-gate structures with submicron gate openings while not requiring expensive lithography techniques.[4,5] Additionally, using silicon as the emitter material offers the advantage of oxidation sharpening.[6] In this study, gold-gated silicon field emission arrays have been fabricated which are capable of producing emission currents of 1 μA at gate voltages of less than 20 V. By utilizing gold as the gate material, single tip or array devices requiring only two masking steps may be fabricated quickly and simply.

Fabrication

Gated silicon field emission devices having gate openings as small as 400 to 500 nm in diameter have been fabricated and tested. An example of a device having a gate diameter of 800 nm is shown in Figure 1. The tips were formed in 1-10 Ω-cm, n-type silicon by reactive ion etching. We have extended our lift-off process using angled evaporation of the gate metal as suggested by Urayama et al.[7] which allows the formation of narrow gate openings. In this case, the process has been simplified by the use of a gold gate. A 600 Å gold gate is deposited onto a 100 Å

thick chromium adhesion layer at a deposition angle of 75 degrees to the evaporation direction. The Cr/Au gate offers two advantages over other gate materials used. First, both Cr and Au are unaffected by hydrofluoric acid, allowing for simple final cap removal. Second, having a gold gate facilitates easy packaging of devices containing many contacts such as addressable arrays. From an experimental standpoint, many devices may be placed on a single die, thus reducing the need for sample transfers. An example of a packaged multi-device chip is shown in Figure 2.

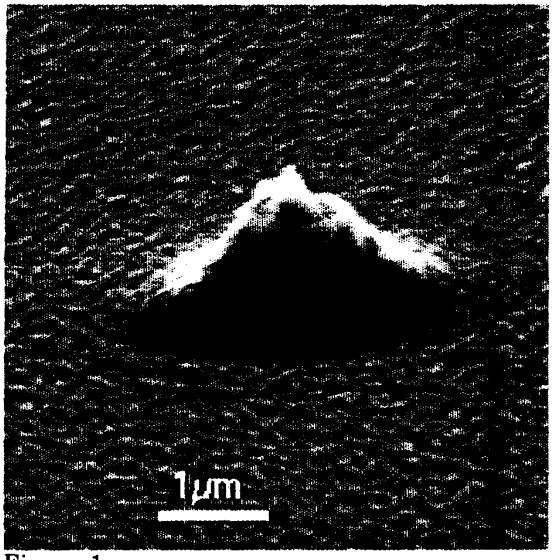

Figure 1:
A single gated field emitter.

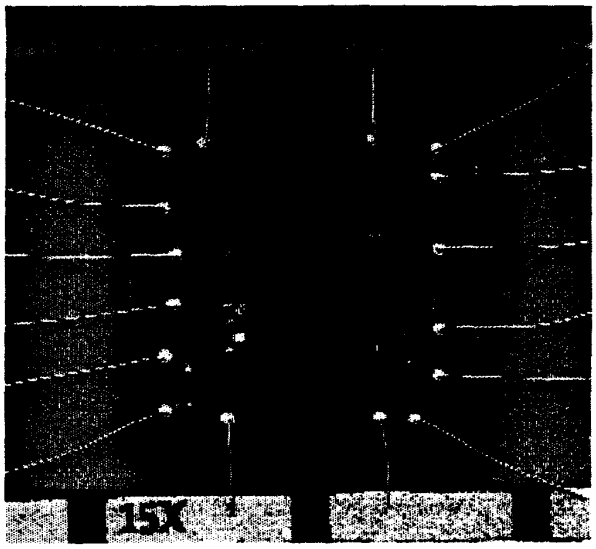

Figure 2:
An SEM of a wire-bonded multi-device chip. The gates and bond pads are part of the same metal deposition. Devices include both arrays of various dimensions and single emitters.

Measurements

Arrays of 50x50 emitters have been shown to produce gate controlled currents on both metallic and phosphor-coated anodes located between 0.5 and 5 mm away from the cathode/gate package. Anode currents vary from 1 μA at a gate voltage of 16 V to 15 μA at a gate voltage of 30 V. Figure 3 shows gate-voltage-controlled anode current as a function of anode voltage. Fowler-Nordheim plots of anode current and voltage at constant gate voltages are linear over several orders of magnitude as shown in figure 4. Field emission parameters extracted from the

plot below give a field enhancement factor, β, of 127 and the total emitting area estimated to be, A = 1.4×10^{-13} cm^{-2}.

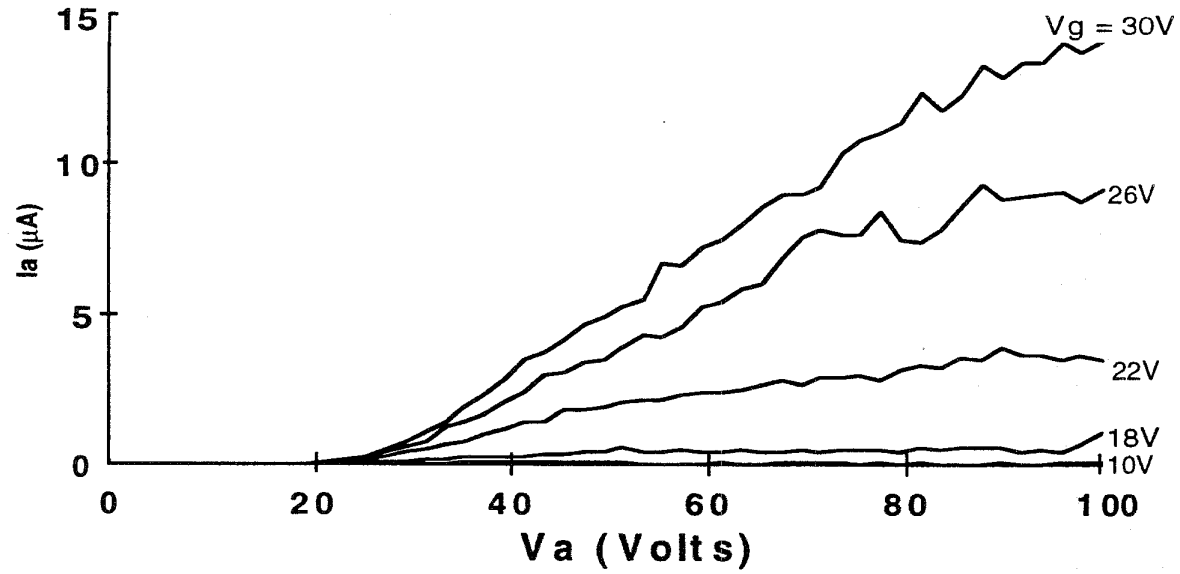

Figure 3: A plot showing gate-voltage-controlled anode current for a 2500 tip array.

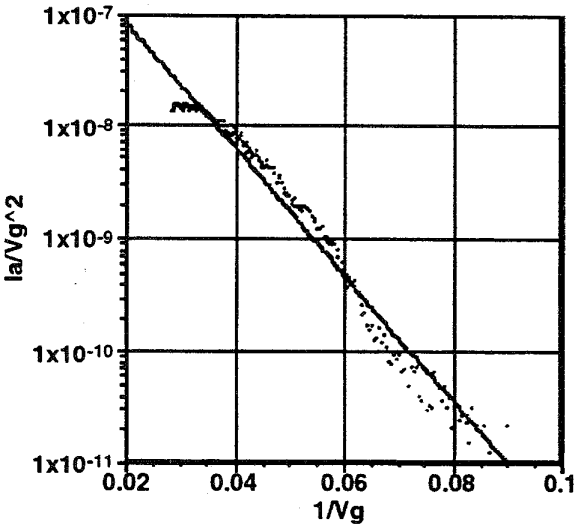

Figure 4: Fowler-Nordheim plot of anode current as a function of gate voltage taken from a 2500 tip array.

Emission currents have shown considerable amounts of noise which can visibly be observed on a phosphor screen when the devices are operated at DC or low frequency. This noise has been measured at low frequencies. An example of the

noise spectrum data measured at a gate voltage of 25V and a pressure of $2x10^{-6}$ Torr is shown in figure 5. These data can be fit to the function for 1/f noise:

$$S(f) = \frac{C}{f^{\gamma}}, \qquad (1)$$

When this is done, γ, the spectral density index, is found to be in the range of 1.18 to 1.55, which is comparable to values measured in P-type devices having similar substrate resistivity and no additional resistive layer.[8] The value of C, which is dependant on the average current is, in this case, $1.76x10^{-11}A^2$.

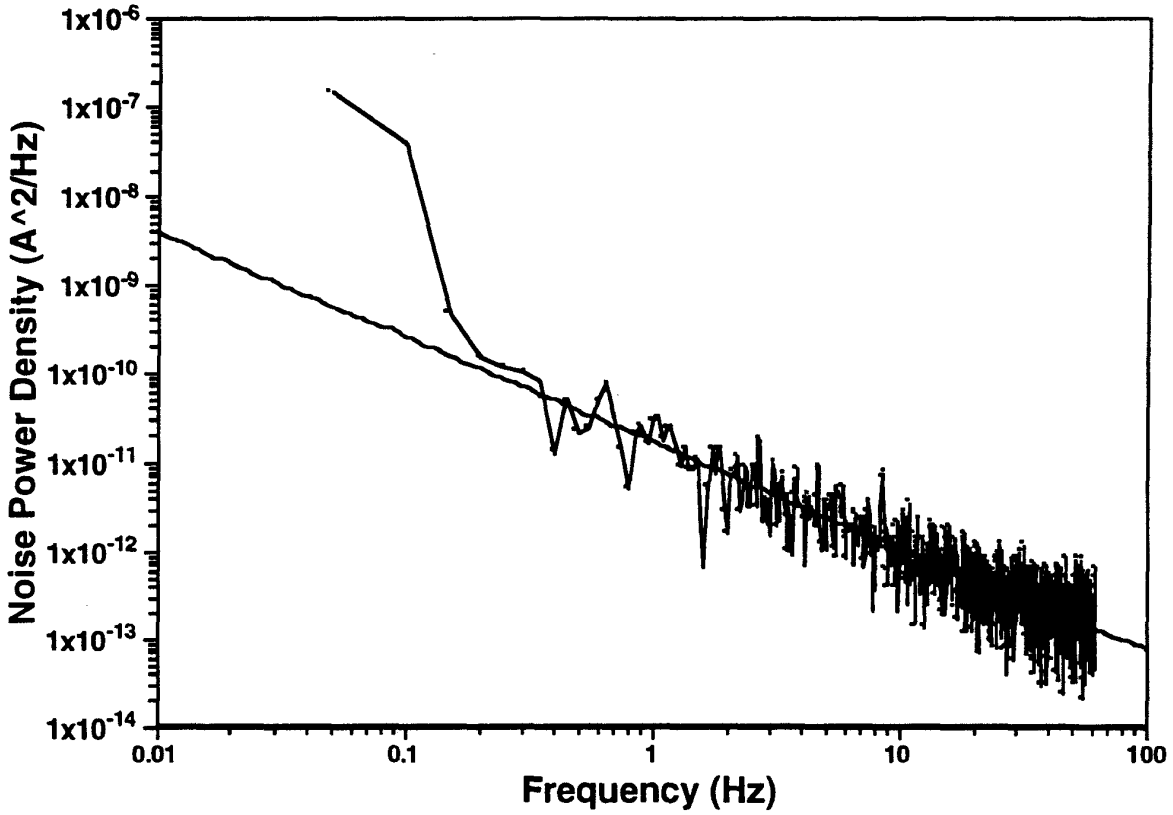

Figure 5: Low frequency noise spectrum of a 2500 emitter array. Si = $1.76x10^{-11}*f^{-1.18}$

Summary

The above data was measured on arrays containing 2500 gated emitters. Smaller arrays and single emitters have been fabricated and are being characterized. By studying the various sized devices it should be possible to ascertain the number of

emitters that are working in the larger arrays. This information will be useful in studying the uniformity of the fabrication process. The various device sizes will also be used to further characterize the noise.

Acknowledgment

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References

1. J.T. Trujillo and C.E. Hunt, "Fabrication of gated silicon field-emission cathodes for vacuum microelectronics and electron-beam applications," J. Vac. Sci. Technol. B, Vol. 11, No. 2, Mar/Apr 1993, pp. 454-458.

2. N.E. McGruer, K. Warner, P. Singhal, J. J. Gu, and Chung Chan, "Oxidation-Sharpened Gated Field Emitter Array Process," *IEEE Trans. Electron Devices*, vol. 38, no. 10, 1991, p. 2389 - 2391.

3. K. Betsui, *4th International Vacuum Microelectronics Conference Technical Digest*, p. 26, 1991.

4. H. Löschner, H. Stengl, A. Chalupka, J. Fegeri, R. Fischer, G. Lammer, L. Malek, R. Nowak, C. Traher, and P. Wolf, "Ion projection lithography for vacuum microelectronics," J. Vac. Sci. Technol. B, Vol. 11, No. 2, Mar/Apr, 1993, pp. 487-492.

5. C.A. Spindt, C.E. Holland, I. Brodie, and P. Schwoebel,"The Fabrication and Performance of Gated Field-Emitter Arrays with Nanometer Feature Sizes," 7th International Vacuum Microelectronics Conference, Revue "Le Vide, les Couches Minces"-Supplément au N° 271,March-Apr.,1994, p. 57

6. R.B. Marcus, T.S. Ravi, T. Gmitter ,K. Chin, D. Liu, W.J. Orvis, D.R. Ciarlo, C.E. Hunt, J.T. Trujillo, "Formation of silicon tips with <1 nm radius," *Appl. Phys. Lett.*, vol. 56, no. 3, pp 236 - 238, Jan. 15, 1990.

7. M. Urayama, T. Ise, Y. Maruo, A. Kishi, R. Imamoto, and T. Takase,"Silicon Field Emitter Capable of Low Voltage Emission," Jpn. J. Appl. Phys. Vol. 32, 1993, pp. 6293-6296

8. R.Z. Bakhtizin, S.S. Ghots, and R.N. Amirkhanov, "Time Stability of Electron Emission and Noise from P-type Si Field Emitters," 7th International Vacuum Microelectronics Conference, Revue "Le Vide, les Couches Minces"-Supplément au N° 271, March-Apr., 1994, pp. 203-206