Fabrication of gated silicon field-emission cathodes for vacuum microelectronics and electron-beam applications

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(Received 13 July 1992; accepted 12 October 1992)

Two types of silicon gated field-emission cathodes have been fabricated. The first is fabricated using a phosphosilicate glass insulation layer and a non-self-aligned etched polysilicon gate. The second type is formed by evaporating silicon dioxide and chrome onto a field-emission point capped by its etch mask. The self-aligned gate is then patterned by lifting-off the cap. Cathode current of the etched-gate structure was not measured until 150 V, at which value the device also failed. Current was measured, however, between the gate and the anode of this structure. This gate-anode current is attributed to a nonplanar gate structure and a gate-anode spacing of ~ 0.5 μm. Gate-anode currents follow a Fowler–Nordheim characteristic, emitting 0.16 μA/gate at 4 V. Current from the lift-off structure was measured between the cathode and the gate. Currents averaging to 0.2 μA/tip at 23 V on the gate have been measured. These devices are intended for application to vacuum microelectronics, flat-panel displays, and cold-cathode electron-beam instruments.

I. INTRODUCTION

Gated field-emission structures are a promising new form of electron-beam source. Fabrication of such devices using silicon integrated circuit (IC) processing technology has the advantage of compatibility with the very mature practices used in modern electronics manufacturing. The resulting electron sources can be used in various applications, including flat-panel displays, vacuum microelectronic circuits, microscopy, lithography, and sensors. The electron beam from a silicon emitter poses many intriguing scientific questions pertaining to physical properties which include spectral distribution properties, beam divergence, and temporal coherence. Furthermore, there are variations in operation which can be observed depending on ambient and pressure; most of these are not fully understood. In previous work, diode arrays of field emission tips were shown to provide reasonable current at low voltages.[1] This work builds on that foundation adding a gate structure which is intended to provide third terminal control of the emission current. Once such a structure can be fabricated reliably, investigation in various applications or of scientific properties may proceed.

In this work, we add a gate to the vertical cold cathode structure; two different methods of obtaining this are demonstrated. The first method, which we call the "etch-gate" technique, uses a grid formed by etching holes into polysilicon which has been deposited over a glass dielectric layer on an array of field-emission tips. This results in a non-self-aligned structure somewhat similar to those formed by Lee *et al.*[2] or Adler *et al.*[3] The second method of forming the gate, which we call the "lift-off" structure is a variation on techniques used by McGruer *et al.*[4] and Betsui.[5] This is a self-aligned device formed by evaporating a silicon dioxide spacer layer and a chrome grid layer over the wet chemically etched field-emission tip array.

II. FABRICATION AND EXPERIMENTAL PROCEDURES

The silicon points for both types of structures were formed in the same manner. *N*-type, (100) Si, 3–5 Ω cm, was covered with a thermally grown, 0.4 μm thick masking oxide. The oxide was patterned to form single 50×50 arrays of 3 μm square point masks spaced on 20 μm centers inside of 3 mm^2 die, as illustrated in Fig. 1(a). The field emission points were formed by isotropically etching in a $HF/HNO_3/CH_3COOH$ solution[6] and sharpened using a low temperature dry oxidation.[7] After this, the fabrication sequences for the etched-gate and the lift-off gate structures differ.

Points used for the etched-gate structure were etched until the oxide cap was removed, leaving structures similar to that shown in Fig. 1(b); after this, they were sharpened. Four sharpening cycles of low temperature oxidation were used. Each cycle consisted of a dry oxidation at 950 °C followed by the removal of the oxide layer with a buffered hydrofluoric acid solution (BOE). The last layer of oxide was removed immediately before the deposition of a 2.3 μm layer of phosphosilicate glass (PSG, $\sim 7\%$ phosphorous), shown in Fig. 1(c). The PSG was reflowed at 1100 °C in N_2 for 30 min, smoothing the deposited layer.

Following the reflow step, the PSG was planarized, as shown in Fig. 1(d). A method similar to that of Lee *et al.*[2] was used. In this case, photoresist was used as the sacrificial layer. One micron of photoresist was applied and etched in a reactive ion etcher (RIE) using $CF_4 + O_2$. The photoresist layer was assumed to not produce a conformal, but rather a level coating. This leaves the photoresist directly above the points thinner than over the remainder of the surface, as shown in Fig. 2(a). Etching then removes both the photoresist and the protruding PSG [Fig. 2(b)]. For this technique to be optimum, the etch rate of the PSG and the photoresist need to be identical, which, in fact, is never the case. Consequently, it was not possible to obtain

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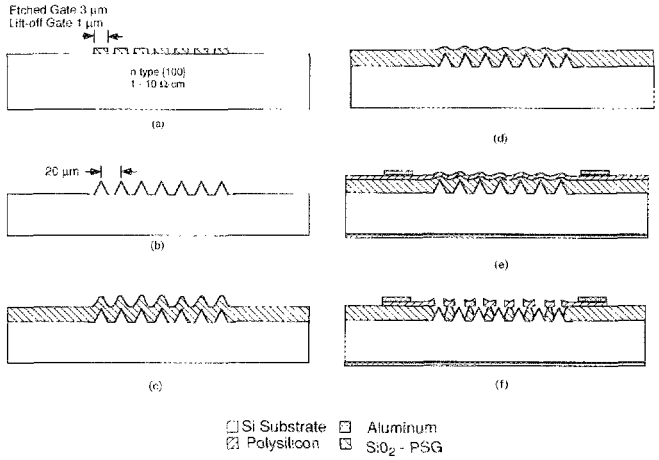


FIG. 1. Fabrication stages of the etched-gate structures. (a) Point mask delineation; (b) point etching and sharpening; (c) PSG deposition; (d) planarization, polysilicon deposition, and aluminium contact patterning; (e) polysilicon gate is etched; (f) the completed structure.

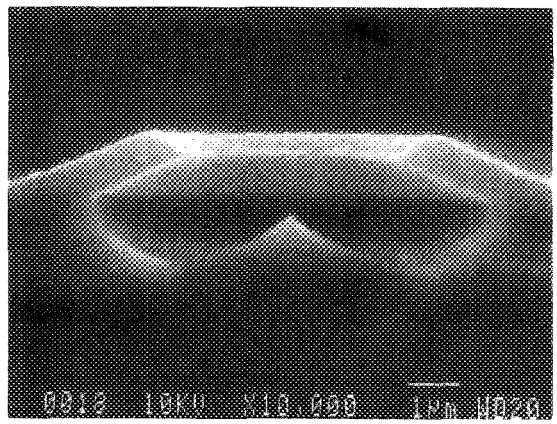


FIG. 3. Scanning electron micrograph (SEM) of the completed etched-gate structure. Note the sloped, rough gate caused by incomplete planarization.

perfectly planar surfaces with the single planarization step used to fabricate these devices.

After planarization, 0.8 μm of polysilicon was deposited onto the wafers. The polysilicon was doped to ~ 5 mΩ cm. The polysilicon and the oxide on the back side of the wafers was then removed using RIE and BOE, respectively. Aluminium was then deposited onto the wafer back sides to ensure ohmic contact to the cathode. Aluminium contact pads were also deposited onto the grid side of the wafers [Fig. 1(e)].

The final mask (an inverse of the original point mask) was used to pattern 3×3 μm^2 holes in the polysilicon, forming the gate openings. The polysilicon was etched using RIE with SF_6–O_2 gas. Following the polysilicon etch, the wafer was sawed for dicing (half-way through), but the die were not separated. It was necessary to do this operation prior to opening the tip cavities to avoid contamination or damage. The PSG spacer between the gate and the points was then etched back in BOE, exposing the tips and resulting in the structure shown in Fig. 1(f). An electron micrograph of the completed structure is shown in Fig. 3 where the tip to gate spacing is ~ 1.2 μm. The finished die could then be separated, packaged, and tested. This completed the process of the etch gate device.

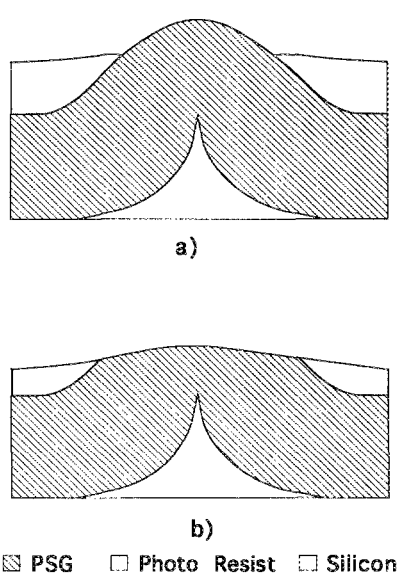


FIG. 2. Schematic of the expected profile of a point covered in PSG and photoresist before and after planarization. (a) Before planarization; (b) after half of the photoresist is etched. Equal selectivity between resist and PSG is assumed.

The lift-off device structure was fabricated as follows. The field-emission points were removed from the isotropic etchant just before the oxide caps were etched free [Fig. 4(a)]. The points were then sharpened using only a single cycle of the low-temperature oxidation (as discussed above), however, the oxide was not immediately removed, as shown in Fig. 4(b). Leaving the oxide "cap" on the points provides a shadow mask for the insulation layer and the gate metal. Silicon dioxide (~ 1.8 μm) was evaporated over the points and, without breaking vacuum, ~ 0.2 μm of chrome was evaporated, as shown in Fig. 4(c). Finally, the oxide supporting the point mask was removed using BOE giving the final structure shown in Fig. 5.

The tip to gate spacing was expected to be ~ 0.8 μm, however, the spacing in Fig. 5 is ~ 1.2 μm. This is believed to be due to nonuniformities in the silicon etch. It is expected that a significant number of points have the correct spacing. It is also possible that the point in Fig. 5 was damaged during SEM sample preparation. (The wafers were then diced and the devices packaged.)

Both microstructures were packaged using standard dual-in-line packages (DIP). The die was attached to the DIP using silver epoxy and gold wire ball bonds were attached to the leads. The etched-gate structure was originally tested in a triode configuration. An anode, similar to that used in previous work,[1] consisted of a die of p-type wafer with a 0.5 mm^2 window etched through a 0.5 μm spacer layer. This anode was placed directly onto the

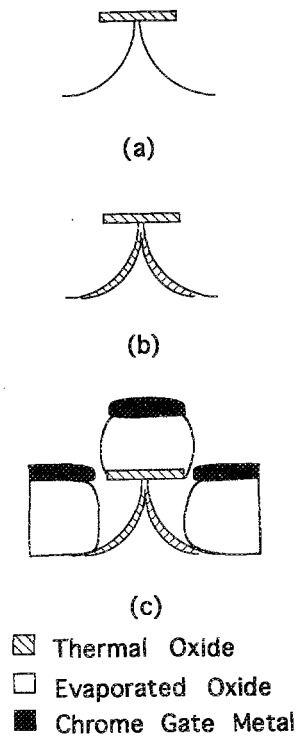


FIG. 4. Fabrication stages of the lift-off gated structure. (a) Points etched, but caps remaining; (b) points oxide sharpened; (c) after SiO_2 and chrome evaporation.

cathode-gate microstructure. This type of anode provides a point to anode spacing of ~ 2.5 μm and a gate to anode spacing of ~ 0.5 μm on the etched-gate structure. Connection to the anode was made via a wire bond to the back side aluminum. A new anode is presently being designed allowing electrons to be collected at various distances away from the cathode-grid structure.

The finished package was placed into a vacuum chamber and connections were made to the terminals. We used a cryostat chamber, diffusion pumped to attain pressures of $\leqslant 1\times 10^{-5}$ Torr. Electrical measurements were made using a digitizing curve tracer. When testing in the triode configuration, the cathode voltage was held constant, the grid voltage was stepped to different voltages, up to a maximum of 40 V, and the anode was voltage swept in both the positive and negative directions. In the diode configuration, the cathode voltage was again held constant and the gate voltage was swept. For the etched-gate structures, testing was also done between the gate and anode in a similar fashion. In each case, the current was measured only at the swept electrode.

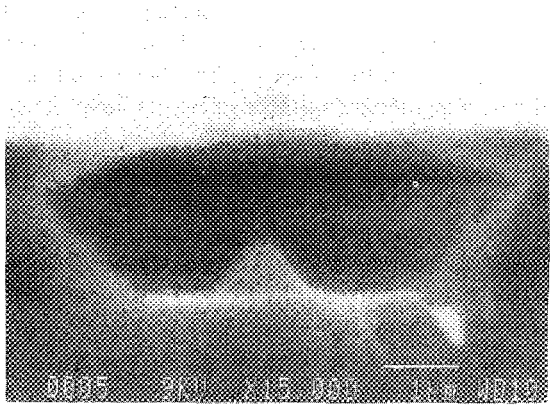


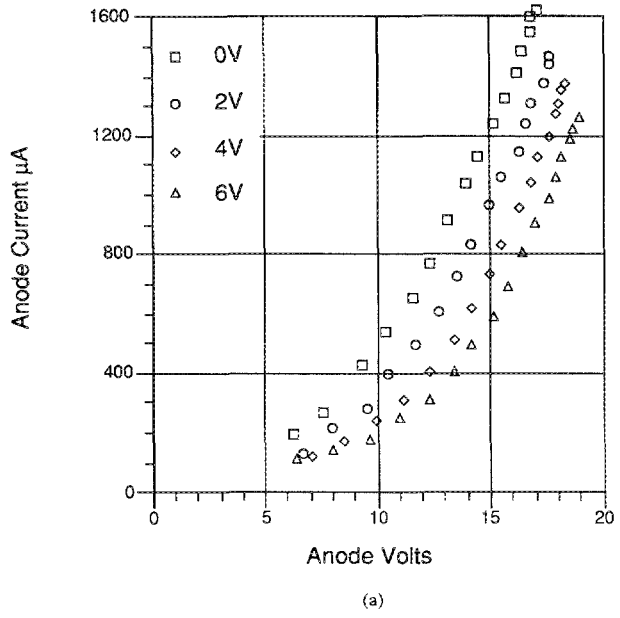
FIG. 5. SEM of the completed lift-off gated structure.

III. RESULTS AND DISCUSSION

The etched-gate structures were first tested in the triode configuration with the p-type die anode. The current–voltage and Fowler–Nordheim results of one of these tests are shown in Figs. 6(a)–6(b). Figure 6(b) shows the straight line characteristic of a Fowler–Nordheim emission mechanism. In Fig. 6(a), the current is controlled by the gate voltage; however, as the gate voltage increases, the anode current decreases. This implies that either a significant amount of the cathode current is being collected by the grid as the grid voltage is stepped, or that most (if not all) of the anode current is actually obtained via field emission from the grid (and therefore, the total anode current decreases as the grid is stepped up). We believe the latter situation to be the explanation as verified by the following measurements.

Measuring current in the diode configuration (e.g., ground cathode, sweep gate, float anode) produced one of two results. The first was a short circuit of the device. The second result was that no gate current was measured until voltages on the order of 150 V were placed between the cathode and the gate. When a current did appear, only a limited number of tips appeared to be emitting, and failure of the devices ensued quickly. A high current density through a few points would most likely cause the devices to fail. This result may be attributed to the following possibilities. First, the sharpness of the points may have been compromised either by the PSG deposition or by over sharpening. Second, the device in Fig. 3 has a gate slope similar to that of the point slope due to insufficient planarization. This would tend to reduce field enhancement at the point, thus increasing the turn on voltage of the device. The insufficient planarization also resulted in a greater tip-gate spacing than expected.

The gate-anode current was also measured in diode mode, by grounding the gate and sweeping the anode while the cathode was left disconnected. Figure 7(a) shows a typical current–voltage characteristic and Fig. 7(b), the corresponding Fowler–Nordheim plot of these data. The straight Fowler–Nordheim characteristic suggests field emission from the gate to the anode is occurring. In this example, emission begins taking place near 3 V. The presence of a field emission current from the gate to the anode is reasonable, considering the gate-anode spacing. Furthermore, the upward-pointing polysilicon grid edges in Fig. 3 are rough, providing many possible emission sites. Also, the gate openings on some points were not completely etched and a thin, sharpened film following the residual contour of the PSG was left intact. This was likely caused



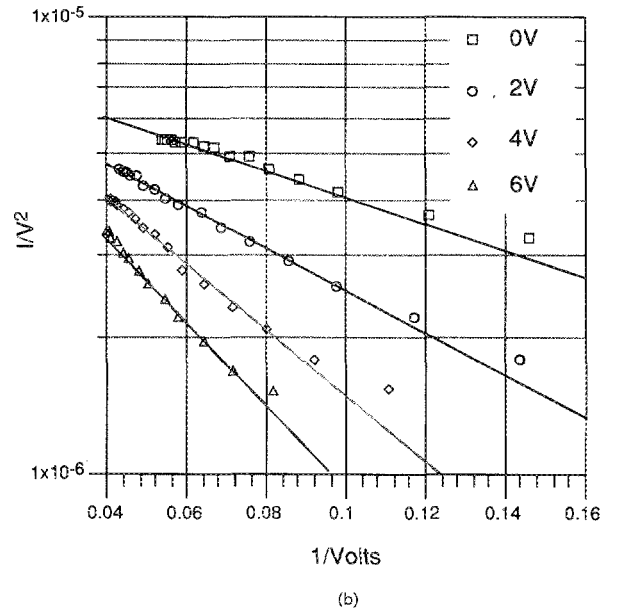
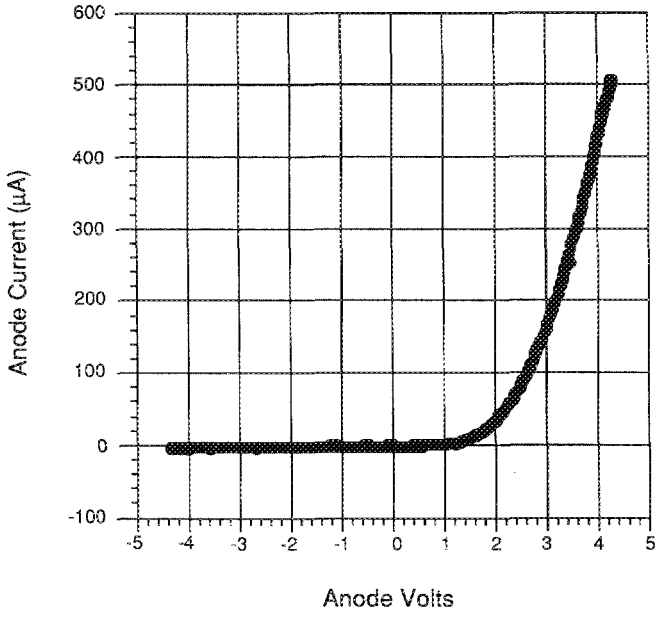


FIG. 6. Current–voltage and Fowler–Nordheim characteristics of a 2500 point etched-gated device measured in triode configuration using a p-type anode with a 0.5 μm spacing oxide. Anode current is measured. The anode voltage is swept, the grid voltage is stepped in increments of 2 V to a maximum of 6 V, and the cathode voltage is held at ground. (a) Current–voltage plot; (b) Fowler–Nordheim plot.



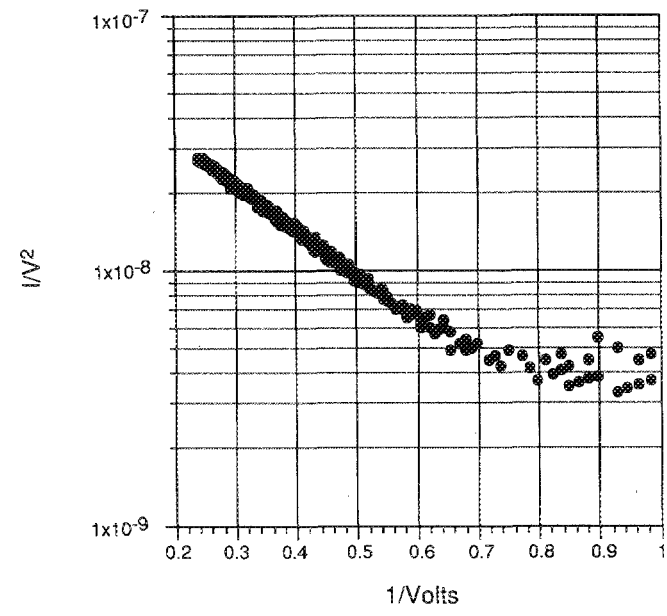


FIG. 7. Current–voltage and Fowler–Nordheim characteristics of a 2500 point etched-gated device measured between the gate and the anode. The anode current is measured, and the gate is grounded. (a) Current–voltage plot; (b) Fowler–Nordheim plot.

by nonuniformities in the etch introduced by the nonplanar surface combined with some nonuniform polysilicon thickness resultant from the planarization process. This condition was random over the wafer and could vary the turn-on voltage of a particular device.

Due to unwanted gate-anode current problems encountered in testing the etched-gate pattern, the lift-off structure was tested in a diode configuration only. That is, current was measured between the cathode and gate. Measurements of the lift-off structure in the diode configuration have produced the current–voltage characteristic shown in Fig. 8. The turn-on voltage of these devices is ~4 V, agreeing the values we found in our previous studies of field-emission diodes.[1] Current averaged of 0.2 μA/point at 23 V. Figure 8(b) shows that these data follow a Fowler–Nordheim characteristic. Also, the presence of the low-voltage slope change in Fig. 8(b) is noted. This two-slope Fowler–Nordheim characteristic has been previously observed by others, including Adler *et al.*,[3] Harvey *et al.*,[8]

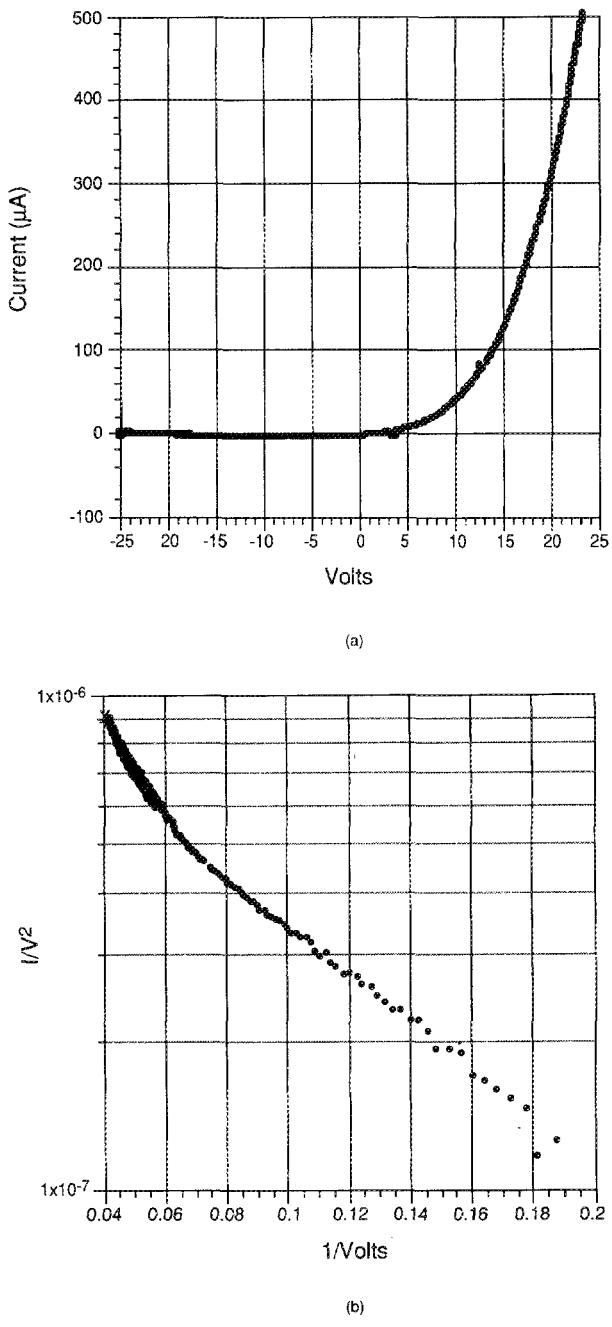


FIG. 8. Current–voltage and Fowler–Nordheim characteristics of a 2500 point lift-off gated device. The device was tested in the diode configuration with the cathode grounded and the gate swept. (a) Current–voltage plot; (b) Fowler–Nordheim plot.

Hunt *et al.*,[1] and Makhov *et al.*[9] The cause of this phenomenon is under investigation; but, it has been attributed to a thin oxide on the tip surface[9] as well as a statistical variance in tip distribution.[8]

Measurements of the lift-off gate structure (Fig. 8) do not include a third terminal measurement of current at a remote anode. These measurements are preliminary, work is progressing towards obtaining three-terminal measurements of anode current from this device.

IV. CONCLUSIONS

Two gated vertical silicon field-emission devices have been fabricated and demonstrated. Both device types are fabricated using standard silicon IC fabrication techniques. The etched-gate structure shows emission between the gate and the anode dominating over poor cathode response. If the gate can be planarized, the problems of gate emission should be solved. A flat gate should etch more uniformly and would also provide higher field magnification at the tip. Further work is continuing with this method.

The lift-off gate structure shows promise and further investigation is proceeding. Measurable conduction in this device appears at ~4 V. More advanced measurements are underway using a variably spaced remote anode as well as characterization over a range of temperatures. These measurements will show clearly the full conduction characteristics of this device. Comparisons of the two device types will demonstrate a preferred structure for examination of the beam characteristics of these gated-emitter devices, as well as provide a foundational device for applications to flat-panel displays and vacuum microelectronic circuits which are being designed.

ACKNOWLEDGMENTS

The authors would like to thank W. Dawson Kesling for his helpful discussions and the following people from Lawrence Livermore Laboratory; Bill Orvis for his assistance with the device modeling, Dino Ciarlo and Ed Hee for their assistance with the CVD systems, and Bill Goward for his help with the SiO_2 evaporation.

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