Optimization of Thin-Film Resistive-Gate and Capacitive-Gate GaAs Charge-Coupled Devices

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Abstract—**Computer simulation of high-speed gallium arsenide charge coupled devices is performed using a two-dimensional semiconductor device simulation program. The measured performance of fabricated GaAs CCD's is compared with modeled results. The effect of active layer thickness and doping concentration on the charge transfer efficiency (CTE) and the dynamic range is investigated using different layers. Various gate architectures are compared for optimum dynamic range and compatibility with GaAs MESFET technology. The effect of clock shape on CTE is studied. Sensitivity analysis is performed on output structures. Both capacitive-gate CCD (CGCCD) and resistive-gate CCD (RGCCD) techniques are considered.**

I. Introduction

FROM THE FIRST introduction of charge-coupled devices (CCD's) in the early 1970's [1], [2], the Si CCD's have matured to the point where there is widespread use of CCD's in consumer products and scientific applications. For high-speed applications, the low electron mobility of Si (1400 $cm^2/V \cdot s$) limits the maximum operating frequency of Si CCD's to about 500 MHz.

We are developing high-speed GaAs CCD's for the capture of single-event electro/photo transients in scientific experiments. High-speed electrical transient recording systems rely on either very fast analog-to-digital converters (ADC's) coupled with fast digital memory, or some form of analog storage medium. CCD's are analog sampling and storage devices that operate in a first-in, first-out manner and are ideally suited as recorders where random access is not required. For frequencies above 250 MHz, the performance of silicon CCD's is severely degraded due to Si carrier mobility or the constraint of raising the operating voltages. The high electron mobility of GaAs can overcome these limitations of silicon CCD's and a fair amount of work has been done on design and optimization of GaAs CCD's [3]–[9] and their applications [10]–[15]; GaAs CCD's operating up to 4.2 GHz have previously been reported [16]. Most of the modeling work previously reported has been done using an in-house program and used relatively thick active layers. In this paper, modeling of GaAs CCD's using a readily available general-purpose semiconductor device simulator is reported for the first time. We also report operation of very-thin-film (0.2-μm) GaAs CCD's.

We have adapted the finite-difference device simulation program. BAMBI (**B**asic **A**nalyzer of **M**OS and **BI**polar devices) [17] for GaAs devices. BAMBI is a two-dimensional numerical solver for Poisson's equation, the continuity equations for electrons and holes, and the two corresponding current relations, respectively, (1)–(3) as follows:

$$\nabla^2\psi = -\frac{\rho(x)}{\epsilon_s} = -\frac{q}{\epsilon_s}(p - n + N_d - N_a) \tag{1}$$

$$\frac{\delta n}{\delta t} = \frac{1}{q}\nabla J_n + G_n - R_n \qquad \frac{\delta p}{\delta t} = -\frac{1}{q}\nabla J_p + G_p - R_p \tag{2}$$

$$J_n = q\mu_n n\xi + q\mu_n \frac{KT}{q}\frac{\delta n}{\delta x} \qquad J_p = q\mu_p p\xi - q\mu_p \frac{KT}{q}\frac{\delta p}{\delta x} \tag{3}$$

where ψ is the potential, ρ is the charge density, ϵ_s is the semiconductor permittivity, n and p are the electron and hole concentrations, respectively, q is the electron charge ξ is the electric field, J_n and J_p are the electron and hole current densities, and KT/q is the thermal voltage. The doping concentrations N_a and N_d, models for the carrier mobilities μ_n and μ_p, the generation and recombination rates G_n and R_n, surface recombination velocities, and the clocking sequence are user supplied to BAMBI as external subroutines.

The mobility model being used takes into account the

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lattice scattering at 300 K and velocity saturation

$$\mu_n^L = \mu_n^0 \left[\frac{T}{300\ \text{K}}\right]^{-\alpha_n}. \tag{4}$$

An analogous model is used for μ_p^L. The zero-field electron and hole mobilities μ_n^0 and μ_p^0, are 7345 and 400 $\text{cm}^2/\text{V} \cdot \text{s}$ [18], respectively.

The power coefficients α_n and α_p are obtained by fitting experimental mobility values [19]. The electron mobiliy model, including velocity saturation, is given by

$$\mu_n^{LE} = \frac{\mu_n^L + v_n^{\text{sat}} \dfrac{(E_n)^3}{(E_n^{\text{crit}})^4}}{1 + \left[\dfrac{E_n}{E_n^{\text{crit}}}\right]^4} \tag{5}$$

where μ_n^L is the lattice scattering mobility, v_n^{sat} is the electron saturation velocity (8.5×10^6 cm/s), E_n is the electric field, and E_n^{crit} is the critical electric field (4.0×10^3 V/cm).

In this paper, the effect of active layer thickness, doping profile, gate length, and clock shape on the CTE and well capacity are evaluated, by modeling and experiment, using a given cell structure. The input and output gates are then added to the basic cell and charge sensing is simulated to determine the sensitivity of the output structure.

II. Device Structure and Modeling Results

A. Active Layer Thickness

The interface of the n-GaAs active layer and the semi-insulating GaAs substrate is modeled as a reverse-biased n-p^- junction because of difficulties in modeling the compensated substrate material. The semi-insulating substrate is lightly doped p-type but compensated by deep level donor defects, so that the net carrier concentration in the deep bulk substrate is effectively zero. In the region near the interface, in equilibrium, the residual shallow acceptors in the substrate will be charged negatively. The adjacent n-type channel region will be charged positively with the silicon donors. The substrate behaves like a depleted low-doped p-layer [20]. In our four-phase CCD cell, the n-type active layer is depleted by applying a positive bias with respect to the gates via an ohmic contact. A gate is then biased to form the potential well. Excess electron–hole pairs (ehp) are then generated and collection of electrons into the potential well is simulated in transient mode. Generation/recombination of excess carries are controlled by a routine, where generation/recombination rate, time, and area can be specified. The adjacent gates are then clocked to observe the transfer of the charge packet. In this fashion, CTE and the maximum speed of operation are determined as a function of active layer thickness.

Fig. 1 shows a simple four-phase GaAs CCD cell. The four phases of the cell are isolated from the ohmic contact V_s by an isolation gate IG_1. The gates are 1.0 μm long and the interelectrode gaps are 0.4 μm. The active layer

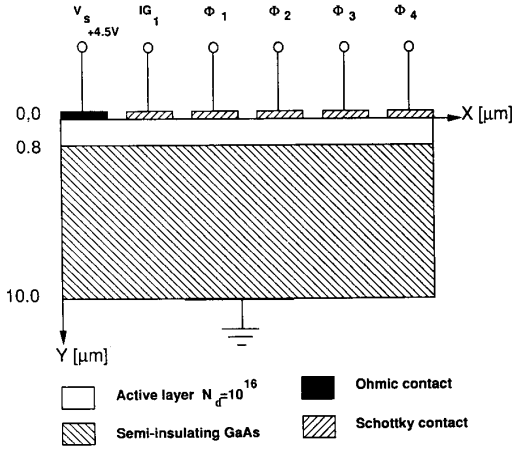


Fig. 1. The cross section of a 0.8-μm channel four-phase GaAs capacitive-gate charge-coupled device (CGCCD), showing the simulation domain. The gates are 1.0 μm long, and the interelectrode gaps are 0.4 μm.

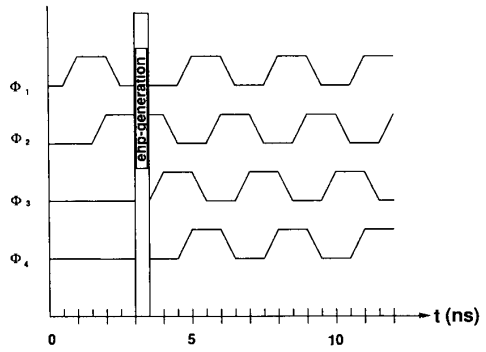


Fig. 2. The relative clocking sequence used for the CGCCD. The voltage swing is between 0 and 2.0 V. The electron–hole pair generation under gate 2 is in the time space between 3.0 and 3.5 ns.

TABLE I
Comparison of Well Capacity and CTE of an $N_d = 1 \times 10^{16}/\text{cm}^3$ Doped Channel CGCCD with Various Active Layer Thicknesses

Active Layer Thickness	Maximum Well Capacity ($\times 10^7$ e^-/cm of gate width)	Maximum Transfer Frequency at 0.999 CTE
800 nm	3.0	555 MHz
1.0 μm	3.93	3.3 GHz
1.2 μm	4.85	5.5 GHz

thickness was varied from 0.8 to 1.2 μm. Fig. 2 shows the clock sequence.

The maximum well capacity is estimated by increasing the generation rate up to the point where electrons cannot be contained by a single phase; at this point, the channel potential is very near the pinch-off voltage. Table I shows the effect of active layer thickness on the maximum well capacity and the CTE when the active layer was varied between 800 to 1200 nm, with an active layer doping level of $1 \times 10^{16}/\text{cm}^3$, which agrees with buried-channel silicon CCD results. As we completely deplete the active

layer by applying a potential equal to the pinch-off voltage through the source contact, the maximum layer thickness that can be simulated is limited by this pinch-off voltage. Higher applied potentials at the source contact create a potential slope towards the source contact and charge starts to spill toward the source contact long before it spills toward the opposite direction. On the other hand, when the active layer becomes thinner and is comparable to the interelectrode gap, electrons get trapped in potential wells of the gap [21]. As the source potential is increased up to the pinch-off voltage, the depletion region starts to widen, both from the gate Schottky junction and the underlying p-n junction. If the interelectrode gap is greater than the channel layer thickness, then the depletion layers associated with the surface and the GaAs/SI-GaAs interface merge before the depletion layers of two adjacent gates extend to each other. This creates a neutral region between the gates which traps the electrons in these regions.

The maximum frequency of charge transfer was found by transferring a small charge packet from phase 2 to phase 3. The transferred charge is then counted by integrating the charge over the area under phase 3 and the frequency at which the CTE drops below 0.999 is taken as the maximum transfer frequency. The charge packet of Fig. 3 is shown after undergoing this transfer to gate 3 in Fig. 4. For thicker active layers the fringing field reaches farther under the adjacent gates and expedites the charge transfer. The charge-transfer inefficiency is an exponential function of fringing field, which in turn is directly proportional to the active layer thickness [22], [23]. The numbers shown in Table I may be conservative, in that for larger charge packets the higher self-induced repulsive fields will improve the initial transfer of the charge packet for a very thin active layer where the effect of fringing field strength is very weak. On the other hand, large charge packets may shield the fringing field longer and hence hinder transfer of the last few electrons [24]. The results shown in Table I follow the trend of previously published results [9], [25].

B. Doping Density

For the four-phase, 0.8-μm active-layer CGCCD, the doping level is varied from 5×10^{15} to 1×10^{16} cm^{-3} to determine the effect of active layer doping concentration on the CTE and well capacity. For the structure of Fig. 1, the well capacity varied from 1.7 to 3.0 ($\times 10^7$) electrons (per centimeter of gate width). The corresponding maximum frequency of operation, based on 0.999 CTE, varied from 555 MHz to 1.66 GHz, as shown in Table II.

C. Asymmetric Clock

We also observed that the CTE is dependent not only on the clock frequency but also on the clock waveform shape. The CTE can be increased by using asymmetric, rather than symmetric clock. In our simulations, we varied independently the rise and fall times of the transfer clock to determine the effect of clock shape on the CTE.

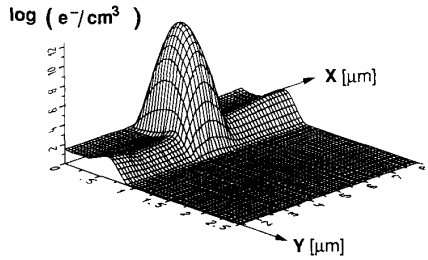


Fig. 3. The collected electron charge packet under gate 2 at time t = 3.5 ns.

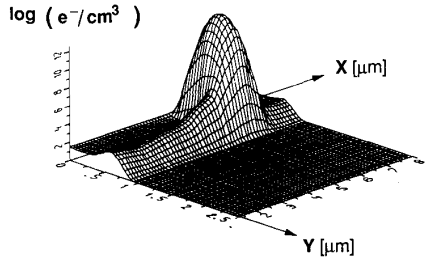


Fig. 4. The electron charge packet of Fig. 3 after 99.9% transfer of charge from gate 2 to gate 3 at time t = 4.5 ns.

TABLE II
COMPARISON OF WELL CAPACITY AND CTE OF A 0.8-μm CHANNEL CGCCD AT VARIOUS ACTIVE LAYER DOPING DENSITIES

Doping Density (per cm^3)	Maximum Well Capacity ($\times 10^7$ e^-/cm of gate width)	Maximum Transfer Frequency at 0.999 CTE
5×10^{15}	1.7	1.66 GHz
8×10^{15}	2.6	833 MHz
1×10^{16}	3.0	555 MHz

Three different cases are simulated. In the first case, the clock period and the fall time are constant, and the rise time is varied. No significant change is observed in the CTE with the variation of rise time. In the second case, the period and the rise time are fixed, and the fall time is varied. In this situation, the CTE improved significantly with increased fall time. The third case is where the clock period is constant, but both rise and fall times are varying. That is, when the rise time is decreased, the fall time is increased by the same amount. In this case also the CTE improved with increasing fall time. It is observed that for a fixed clock period, the best CTE is achieved by using a faster rise time and a slower fall time.

Fig. 5(a) and (b) demonstrates this phenomenon by illustrating charge transfer between two gates with a clock having a pulsewidth of 0.4 ns. The CTE is more than 0.999 when a slower fall time of 0.3 ns is used, as shown in Fig. 5(a). On the other hand, when a faster fall time of 0.1 ns is used, the CTE drops below 0.987 as illustrated in Fig. 5(b). Both the above cases have the same clock period and the same rise time.

The above observations can be explained in terms of the electric fields responsible for charge transfer between

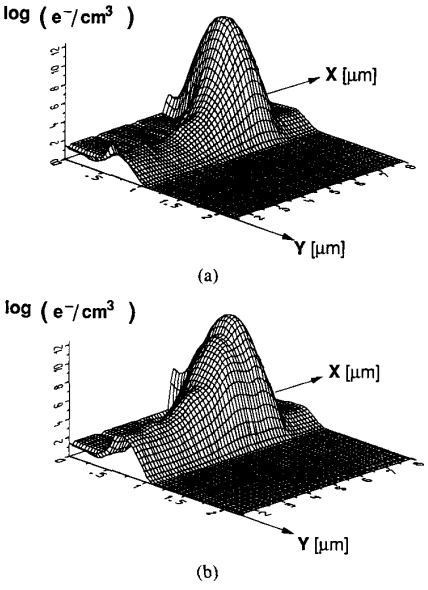


Fig. 5. An asymmetric clock is used to obtain improved CTE. Using a 1.25-GHz clock with (a) rise time of 0.1 ns, zero hold time, and fall time of 0.3 ns, the charge transfer is nearly 100%. (b) Considerable degradation of CTE is observed at the same frequency and rise time, but with fall time shortened to 0.1 ns.

two adjacent gates. The lateral electric field in a CCD can be divided into two parts: the fringing field associated with the x-direction field spreading from one gate to the next, and the self-induced field associated with the variation in charge concentration from point to point under the transfer gate. For the above case, when the voltage on phase 3 becomes equal to the voltage on phase 2, the charge begins to flow into the potential well under gate 3 due to self-induced drift; charge is now distributed under both gates 2 and 3. As long as the voltages on phases 2 and 3 are equal, no futher charge transfer will occur. When the voltage on phase 2 starts to fall below the voltage on phase 3, the fringing field due to the unequal voltages on the adjacent gates forces the charge under gate 2 into the well under gate 3. If the potential well under gate 2 collapses too quickly, the trailing edge of the charge packet will not have sufficient time to traverse the total gate length of the discharging well and will not be transferred. Consequently, the speed of collapse of the discharging potential well is much more important for the improvement of CTE than the speed of formation of the receiving potential well. Using an asymmetric clock could improve CTE by this mechanism, but generation of such asymmetric waveforms at higher frequencies may be problematic. These observations agree with previous silicon CCD investigations [26].

D. Output Structure

The output structure consists of an output gate (G_O), a MESFET with a floating n^+ source, a reset gate (G_R), and a drain biased to the dc voltage V_d. Fig. 6 shows the CCD

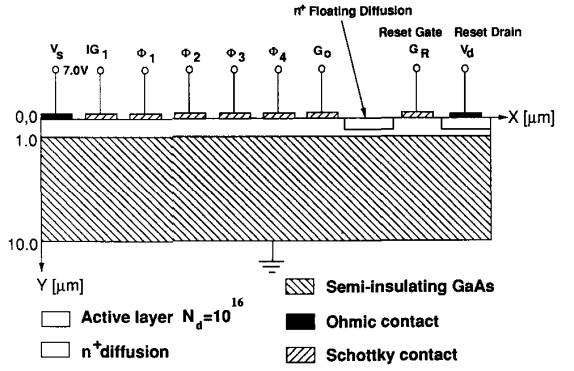


Fig. 6. The cross section of a 1.0-μm channel four-phase GaAs CGCCD including both input isolation, and output sensing and reset gates.

with the output charge sensing structure, without the amplifier stage. All of the gates, the floating diffusion, as well as source and drain regions are 1.0 μm long; the interelectrode gaps are 0.4 μm. A reset pulse, applied to G_R, resets the floating diffusion potential to V_d. Pulsing the output gate G_O, the signal charge is transferred to the floating diffusion.

Electrons that are clocked out of the CCD to the output node cause a voltage change according to the equation $\Delta V = qN/C_{fd}$, where q is the electron charge, N is the number of electrons transferred, and C_{fd} is the output node capacitance. In general, minimizing C_{fd} increases the output sensitivity and reduces the noise [27]. Normally the capacitance C includes the floating diffusion capacitance and the output amplifier MESFET gate capacitance. We modeled only the output charge-sensing structure, excluding the output amplifier. Beyond pinch-off of the channel, which is the case here, the gate-to-source and gate-to-drain capacitance is given by [28], [29].

$$C_{gs} = \epsilon\, w \tan^{-1} \sqrt{\frac{V_{bi} - V_{\text{th}}}{V_{\text{th}} - V_{gs}}} \tag{6}$$

where

- ϵ permitivity of the semiconductor
- w gate width
- V_{bi} built-in voltage
- V_{th} channel theshold voltage
- V_{gs} gate-to-source voltage.

For $V_{bi} = 0.85$ V, $V_{gs} = -7.0$ V, C_{gs} was calculated to be 8.06 fF/cm of gate width. Hence the capacitance of the floating source region and the output gate G_O plus the capacitance of the floating source and reset gate G_R is $C_{fd} = 16.12$ fF/cm of gate width. For a transferred charge packet of 74209 electrons, the expected change in floating diffusion potential is

$$\Delta V = \frac{Q}{C_{fd}} = \frac{74209 \times 1.6 \times 10^{-19}}{16.12 \times 10^{-15}}\ \text{V} = 0.73\ \text{V}$$

giving an output sensitivity of about 9.9 μV/e$^-$. Fig. 7(a) shows the CCD just before a charge packet of 74209 elec-

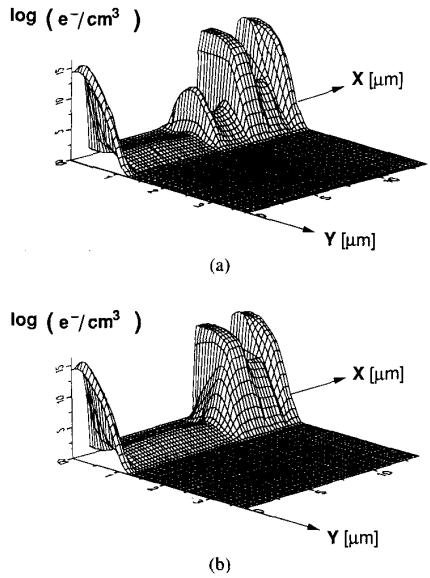


Fig. 7. The sensitivity of the output structure is determined by transferring a known number of electrons to the floating diffusion and measuring change in potential of the floating diffusion. (a) The electron packet immediately before transfer from the CCD to the floating diffusion via the output gate G_O. (b) After charge transfer, the floating diffusion surface potential is measured; the change in surface potential divided by the number of transferred electrons yields the output sensitivity.

trons is transferred to the floating source region. At this point the surface potential of the floating source is 5.98 V. After completion of the signal charge transfer to the floating source, Fig. 7(b), the surface potential of the floating source is 5.29 V. This ΔV of 0.69 V, which is fully sufficient for external amplification, corresponds to a sensitivity of about 9.3 μV/electron, assuming a 100% charge transfer between Φ_4 and the floating source.

To observe the effect of charge packet size on the sensitivity, a smaller charge packet of about 32040 electrons was transferred to the floating diffusion region, resulting in a $\Delta V = 0.32$ V. This corresponds to an output sensitivity of about 9.98 $\mu V/e^-$. Hence the output sensitivity variation with charge packet size is very small, but lower charge packet size may increase the output sensitivity.

E. Resistive-Gate CCD

Both CGCCD's and RGCCD's have been studied and built. For the case of the CGCCD, the minimum active layer thickness that could be simulated had to be greater than the gaps between the CCD gates because of electron trapping in the deeper interelectrode gap potential wells. The tendency of electron trapping is found to be more pronounced for a thinner layer than for thicker layers. In resistive-gate CCD's, a CERMET layer (in this case a thin film of resistive Cr/SiO oxide that forms Schottky contacts with the GaAs layer [30]–[32]) covers both the gates and the gap. This eliminates the interelectrode-gap potential well problem because of the distributed surface potential and also inhibits the charge packet broadening

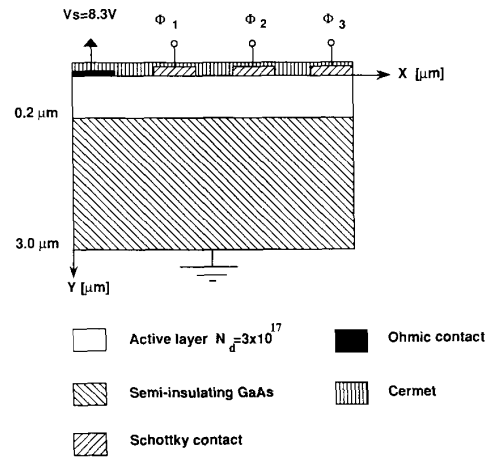


Fig. 8. The cross section of a 0.2-μm channel, three-phase GaAs RGCCD showing the simulation domain. The gates are 1.75 μm long, and the interelectrode gaps are 1.25 μm.

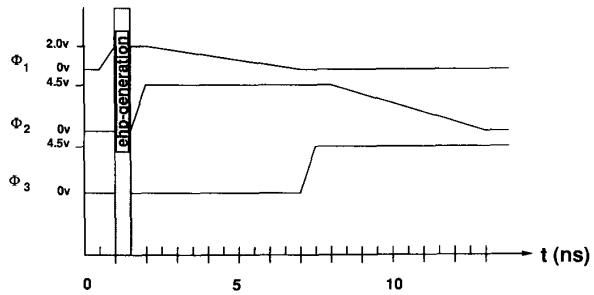


Fig. 9. Clocking sequence used for the 0.2-μm active layer, three-phase RGCCD. Excess carriers are generated between 1.0 and 1.5 ns.

[25]. Experimentally, the CERMET is deposited using RF sputtering and subsequently defined in proper areas using liftoff patterning. In our simulations, the CERMET layer is modeled using a series of gates having distributed potentials. An RGCCD having the same geometry as in Fig. 1, with a channel doping of 8×10^{15} cm^{-3}, is simulated for comparison with the CGCCD. For the RGCCD, the maximum transfer frequency, at a CTE of 0.999, improved to 1.7 GHz compared to 833 MHz for a comparable CGCCD.

Our simulations demonstrate the trends in RG and CGCCD's with different device parameters. In order to accommodate the support circuitry in the same chip as the CCD, an RGCCD compatible with existing MESFET technology was simulated. The device cross section of a three-phase, 0.2-μm active layer RGCCD is shown in Fig. 8. The clock sequence is shown in Fig. 9. These values are chosen to maximize compatibility with the MESFET integrated support circuitry. The simulation results showed no electron trapping in the interelectrode gaps when a CERMET layer was used. For our structure, the well capacity is approximately 4.4×10^8 electrons per centimeter of gate length. The simulated maximum transfer frequency at 0.999 CTE is about 33 MHz. This pen-

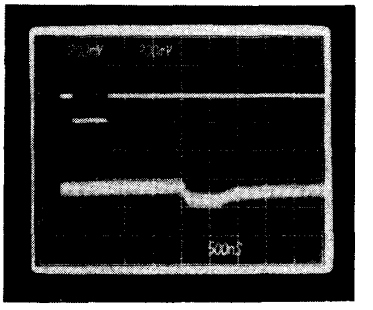
alty in performance is the direct result of using a thin film and higher doping level necessary for MESFET compatibility.

III. Experimental Results

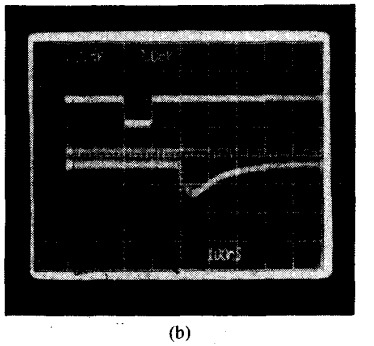
The modeling results of both CGCCD's and RGCCD's were compared with the measured performance of such devices fabricated at Lawrence Livermore National Laboratory. The experimental RGCCD has a 0.2-μm active layer thickness and a doping level of 3×10^{17} cm^{-3}. The gates are 1.75 μm by 20 μm. The interelectrode gap is 1.25 μm. A CERMET layer is deposited covering both the interelectrode gaps and the Cr/Au gate electrodes. The simulated maximum clocking speed at a CTE of 0.99 is about 100 MHz. The experimental measurements of the fabricated GaAs RGCCD generally agree with this value. Degradation of CTE is measured as the clock frequency is increased. This can be seen in Fig. 10(a) and (b), which shows measured input and output signals at 20 and 290 MHz, respectively. These CTE's are low compared to previously published results [33], [16]. In 1983, Sovero *et al.* reported a GaAs CCD with best measured CTE of 0.9999 and an average CTE of 0.997 at a clock frequency of 1 GHz. The geometry of the particular CCD or the doping level of the active channel are not known, hence, it is not possible to directly compare our results. In 1984, Sovero *et al.* reported a GaAs 3-μm cell CCD with an active layer thickness of 0.3 μm and channel doping of 1×10^{17}/cm^3 (the gate length was not mentioned). The maximum reported CTE was 0.99 at 2.5-GHz clock frequency.

For compatibility with our existing GaAs MESFET technology at the Livermore Laboratories (LLNL), our CCD was designed to have a thinner active layer and a higher doping level. The Rockwell [16] CCD's active layer was 50% thicker than the LLNL CCD, and the doping level of the LLNL CCD is 300% higher then the Rockwell CCD. As shown in our simulations, both thinner active layer and higher doping level drastically reduces the CTE of a CCD. Hence the lower CTE of the LLNL CCD is expected.

Most of the experimentation was done at lower frequencies (around 10 MHz). This allowed wafer probing of the CCD's; high-frequency testing requires individual device packaging. All devices were fabricated using MBE-grown epitaxial layers on semi-insulating substrates. The active CCD channel was isolated from the substrate by a low growth temperature ($\sim$200°C) layer of GaAs which has been shown to reduce backgating effects in GaAs MESFET circuits [34]. Although the details of how this layer impacts the performance of the CCD's have not been fully investigated, many devices demonstrated transfer of charge at frequencies as low as 1 MHz. This indicates that dark currents are very low. Collection of dark current, which fills the wells to capacity, is generally the source of the lower frequency limit on the operation of GaAs CCD's. The high-frequency limitation is the inability to transfer all of the charge from one cell to the next within one clock cycle. Many of our early CCD's utilized gate recess etching to adjust the pinch-off voltage of the CCD gates. Some of these CCD's do not exhibit any charge transfer. Our modeling suggests, in these cases, that the CTE frequency limit may be lower than the dark-current frequency limit due to the thermally generated dark current and gate leakage current, both thermionic emission and thermionic-field emission components. The thermionic emission component of the leakage current is important for lower doping level, and for a doping level of more than 10^{17}/cm^3 the thermionic-field emission component becomes dominant [18]. For our structure, the thermally generated component of the dark current is about (9.8×10^3 carriers/cm^2 · s) [35] and is orders of magnitude lower than the gate leakage current (3.13×10^{10} carriers/cm^2 · s) at room temperatures.



(a)



(b)

Fig. 10. Measured electrical input and delayed output signal for a 0.2-μm active layer 16-cell RGCCD. (a) At 20-MHz clock, the delayed output is a reasonable reproduction of the input pulse. (b) At 290 MHz, the output is distorted, showing degradation of CTE at higher operating frequencies.

In addition to the four-phase devices that are the primary subject of our modeling effort, we also fabricated a modified four-phase structure that operates with only two clocks, 180° out of phase with each other. The four-phase structure was modified by combining gates 1 and 2 together to form what is referred to here as a "phase-A gate." A permanent potential gradient is formed between what used to be gates 1 and 2 by slightly etching the GaAs under gate 1 before the phase-A metal is deposited over the gate 1–gate 2 combination, similar to the castellated

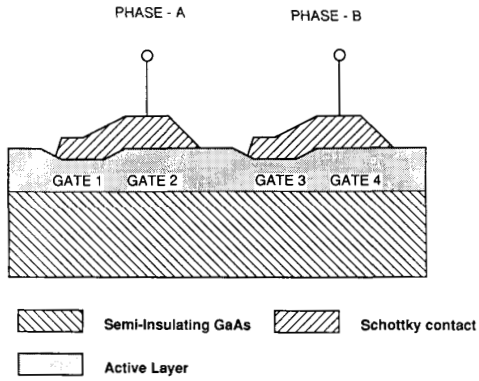


Fig. 11. Schematic cross section of a two-plase CCD. Gates 1 and 2 of the four-phase CCD are connected to form a single phase-A gate. The region under gate 1 is slightly etched to form a permanent potential gradient to collect electrons under the right half of each gate.

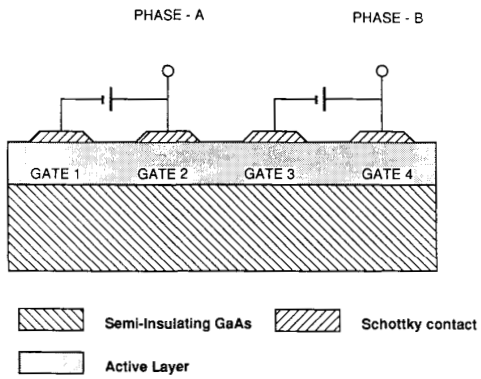


Fig. 12. Operation of a four-phase CCD in quasi-2-phase mode. A small fixed potential is appled between gates 1 and 2 to produce a potential gradient in the CCD channel that causes electrons to be collected under gates 2 and 4.

channel geometry reported by Kellner *et al.* [36], Kosel *et al.* [37], and LeNoble *et al.* [38]. A schematic cross section of this is shown in Fig. 11. This has the effect of making the region that is etched slightly more repulsive than the region next to it even though the two regions are under the same phase-A metallization. This is because the gate over the etched region is closed to the conducting CCD channel. Electrons that are injected under phase-A pass through the etched region and accumulate in the less repulsive potential well formed under the unetched side of phase-A. The probability of transport in the opposite direction is reduced substantially due to the fixed potential gradient between the two halves of the region. Analogous modifications are made to phase 3 and phase 4 to form phase-B. These devices have been demonstrated to transfer charge but the CTE is poor. We believe that the poor CTE is due to a spurious potential pocket that is formed at the edge of the etched region between phase-A and phase-B interfering with the electron transport from phase-A to phase-B. The effect that enhances the directional charge transport within one of the phases (i.e., the edge of the etched region) has a detrimental effect on transport between the phases.

The four-phase devices also operate in a "quasi-2-phase" mode. To do this, gate 1 is tied to gate 2 with a fixed negative dc voltage offset. Similarly, gate 3 is tied to gate 4, with an offset, as shown in Fig. 12. This has the same effect as the two-phase device in that the electrons injected under gate 1 are swept into the potential well under gate 2. This produces CTE comparable to four-phase operation without the problems associated with the CCD's that were physically modified for two-plate operation.

In general, both the four-phase and the quasi-2-phase CCD's show improvement in CTE when the CERMET layer is used. This improvement is due to 1) a reduction of surface potential variations due to the presence of Schottky metal covering the entire structure, particularly in the interelectrode gaps, and 2) the potential gradient between gates formed by the resistive CERMET which enhances electron transport through the CCD's.

IV. Conclusions

We have seen that both well capacity, and to a greater extent, CTE, decrease with decreasing active layer thickness. In general, thicker active layer CCD's have higher well capacity and higher operating frequencies, until the point at which the required pinch-off voltage becomes too high and approaches gate breakdown voltage. To the first order, the well capacity is directly proportional to the active layer thickness for a fixed doping level. Low-doped active layers have better CTE due to a higher electron mobility.

Compatibility with established GaAs MESFET technology requires higher doped, thinner active layers. The higher doping in the thinner active layer will compensate somewhat for the loss of well capacity in the thinner layer. The high doping and thin layer will, however, degrade the CTE. Such degradation of the CTE can be partially compensated for by using an RGCCD architecture.

The speed at which charge is transferred between two gates of a CCD cell is a function of not only clock speed, but also of clock shape. Keeping the clock frequency constant, an extended fall time improves the charge transfer. The CTE is less sensitive to the rise time of the clock as compared with the fall time. Using an asymmetric clock with a faster rising edge and slower falling edge improves the CTE for a given clock frequency.

The computer simulation of a complete GaAs CCD cell, including the output sensing and reset gates, provides insight into the operation of the CCD's. This provides a powerful means to optimize the architecture of the GaAs CCD cell for maximum performance.

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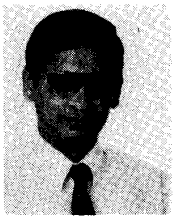

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