High-Efficiency Micromachined Sub-THz Channels for Low-Cost Interconnect for Planar Integrated Circuits

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***Abstract*—This paper presents for the first time the design, fabrication, and demonstration of a micromachined silicon dielectric waveguide based sub-THz interconnect channel for a high-efficiency, low-cost sub-THz interconnect, aiming to solve the long-standing intrachip/interchip interconnect problem. Careful studies of the loss mechanisms in the proposed sub-THz interconnect channel are carried out to optimize the design. Both theoretical and experimental results are provided with good agreement. To guide the channel design, a new figure of merit is also defined. The insertion loss of this first prototype with a 6-mm-long interconnect channel is about 8.4 dB at 209.7 GHz, with a 3-dB bandwidth of 12.6 GHz.**

***Index Terms*—Channel, dielectric waveguide, interconnect, micromachined, sub-THz, terahertz (THz).**

I. Introduction

THE input/output (I/O) bandwidth growth of intrachip/interchip communications doubles every two years over the past decade, and the trend is projected to continue in the future [1]. However, the number of I/O pins increases slowly over the time due to physical constraints. To overcome this increasing gap between the I/O bandwidth and pin numbers, the transmitting data bandwidth per I/O, defined as bandwidth density, should keep up with the interconnect bandwidth requirement. In addition, the energy used for data communications may potentially be orders of magnitude higher than the energy used for data processing and storage [2]. There are two scenarios for the interconnect: intrachip interconnect, which is the communication among CPU cores or among the high-speed processing components inside a chip, and interchip interconnect, which is the communication between chips. Therefore, to ultimately solve the problem of intrachip/interchip interconnect, both bandwidth density and energy efficiency should be boosted.

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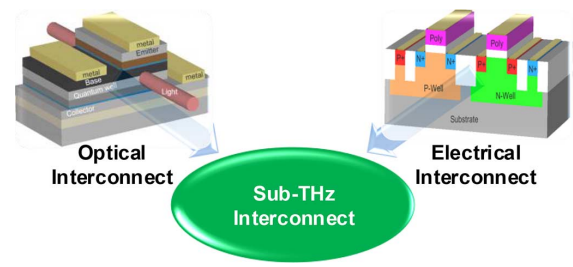

Fig. 1. Proposed sub-THz interconnect by leveraging optical interconnect [3] and electrical interconnect advantages.

Interconnect research has been active in two areas: optical interconnect [3]–[6] and electrical interconnect [7]–[11]. Optical interconnects have the advantages of low loss and high bandwidth, but it is still very challenging to integrate highly efficient light sources with current CMOS processes [4]. Electrical interconnect schemes are compatible and scalable with silicon processes. However, the transmission media, metal wires, has severe conduction loss with high data rates or operating at high frequencies, thus limiting the supported bandwidth. Therefore, both electrical and optical interconnect face big challenges to fill this gap individually.

The sub-THz interconnect, using the spectrum sandwiched between optical and microwave frequencies, holds high potentials to fill the interconnect gap with wide bandwidth density and high energy efficiency by leveraging advantages of both optical and electrical interconnect approaches: low-loss quasi optical channels as well as advanced high-speed semiconductor devices, illustrated in Fig. 1.

The comparison with the state of the art is shown in Table I. Wireless chip-to-chip communication, demonstrated in [7]–[10], suffers from large losses. For example, the path loss is greater than 40.9 dB with 40-mm distance at 260 GHz [7] and 66 dB with 1-m distance at 45 GHz [8]. The challenge of wireless chip-to-chip communications is that the path loss is inversely proportional to λ^2, which impedes high-frequency adoption in wireless scheme. Besides, the interference between channels is a big issue for wireless based schemes. Chang's group [11] demonstrates a design on wired interconnect based on-chip transmission line, which also faces the challenge of increasingly high losses versus frequencies.

In general, the interconnect can be classified into three types: transmission line (including microstrip line, coplanar waveguide (CPW), grounded CPW, etc.) [12], [13], metallic

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TABLE I
COMPARISON AMONG DIFFERENT TECHNOLOGIES OF CHIP-TO-CHIP COMMUNICATIONS

Design	Wired/ Wireless	Carrier Freq (GHz)	Distance (mm)	Path Loss (dB)	Normalized Path loss* (dB) with 10-mm l at 200 GHz
[7]	Wireless	260	40	40.9	26.6
[8]	Wireless	45	1000	66	38.9
[9]	Wireless	60	100	58	48.5
[10]	Wireless	43	100	45	38.4
[11]	Wired	60	3	6.6	N/A
This work	Wired	210	6	8.4	8.7

*The path loss normalization is calculated based on Friis equation for wireless type.

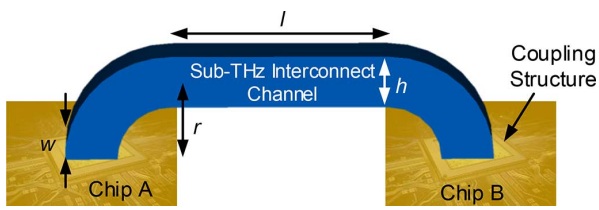

Fig. 2. Illustration of the proposed dielectric waveguide based sub-THz interconnect, which is adapted from [25].

waveguide [14]–[18], and dielectric waveguide [19], [20]. The dielectric waveguides with low-loss dielectric material have much less losses than transmission lines and metallic waveguides, since the conduction loss is avoided. For example, a metal-based transmission line has almost three orders higher loss than the loss of silicon ribbon at the THz frequency [21]. The loss for the CMOS transmission line is about 1 dB/mm at 100 GHz and 2 dB/mm at 150 GHz and increases fast with frequency [22], [23]. Moreover, from the process-compatible point of view, the dielectric waveguides are easier to fabricate and potentially compatible with integrated silicon circuits compared with metallic waveguides. Metallic waveguide poses a big challenge to integrate with ICs due to the waveguide flange connection. Therefore, to enable a sub-THz interconnect, the channel should have wide bandwidth and small size for large bandwidth density, low loss for high energy efficiency, and good compatibility with silicon processes for low cost as well as good isolation among channels.

To satisfy these requirements, dielectric waveguides [24] are employed by taking advantage of quasi optical channels. Low-loss THz channels have been investigated with loss of 0.1 dB/m [21]. However, till now, no investigations have been conducted on planar silicon process based compatible sub-THz channels for intrachips/interchips interconnects.

In this work, we demonstrate the feasibility of using a micromachined dielectric waveguide as a low-loss chip-to-chip interconnect channel that is compatible with conventional semiconductor and packaging processes. Fig. 2 illustrates the concept [25]. The signal, transmitting from chip A, propagates through the channel and reaches chip B. The bending structures at two ends of the channel are to establish the link for planar processes.

Compared with the authors' previous work [25], this paper presents a thorough analysis of the design tradesoffs for the silicon dielectric waveguide as well as the analysis of the bending loss, radiation loss, and mode conversion loss. We propose a figure of merit (FoM) to quantify channel design by incorporating bandwidth-area efficiency and channel loss. The first demonstration is presented at 210 GHz due to the constraint of the measurement equipment availability. The channel design methodology can be readily applied to higher frequencies in the THz range.

This paper is organized as follows. Section II reviews and presents the fundamental concept and design methods of the silicon dielectric waveguide-based sub-THz interconnect. Section III discusses the design and considerations of the coupling structure. Section IV presents the fabrication, the measurement, and discussions of the sub-THz interconnect.

II. SILICON DIELECTRIC WAVEGUIDES AS SUB-THZ INTERCONNECT MEDIUM

To enable a high data transmission rate, the proposed sub-THz dielectric interconnect channel must be optimized for both bandwidth and loss. The bandwidth of a dielectric waveguide is primarily determined by the dispersion characteristics of the chosen mode of the propagating wave and the orthogonality and/or separation from other modes. In this demonstration of the proposed concept, we choose to operate our waveguide in the lowest order mode (E_{y11}) to simplify the design and implementation. The loss of the waveguide is determined by many factors, including the dielectric loss of the material, the geometry of the waveguides, such as bending and discontinuity structures, and possibilities of mode conversions. The following subsections provide detail discussions of these factors for design guidance.

A. Material Loss

Material loss can be a critical contribution to the total channel loss. It is, therefore, desirable to use low-loss materials as the dielectric medium. Several materials have been studied at sub-THz frequencies, such as silicon [21], [26]–[30], quartz [21], and plastic [31], [32]. These works provides evidence that dielectric sub-THz interconnect channels can be designed with low loss. In particular, the loss of high-resistivity (HR) silicon has been reported to be as low as 0.1 dB/m at 200 GHz [21], which is one of the reasons that HR silicon is used in this work. A second reason to choose HR silicon is due to its relatively high dielectric constant $(\epsilon_r = 11.9)$, which helps to confine the electromagnetic (EM) wave inside the waveguide. A higher level of confinement can reduce cross-talk between adjacent channels, lower packaging parasitics, and facilitates wave guidance in nonstraight channels, such as bending structures.

B. Waveguide Geometry

Rectangular silicon waveguides with air surrounding are used in this work. Compared to the other geometries, such as circular waveguides, rectangular waveguides are easier to fabricate using microfabrication technologies, such as the deep reactive-ion etching (DRIE). Also, rectangular waveguides are not prone to have polarization mode dispersion issues [33], which minimize polarization mismatches and losses.

Fig. 3(a)–(c) shows the effective index n_{eff}, the wave confinement factor Γ, and the attenuation constant α of rectangular waveguides of various dimensions w of 100–500 μm, and h of 100–700 μm) based on full-wave simulation in an ANSYS high-frequency structure simulator (HFSS). Due to the

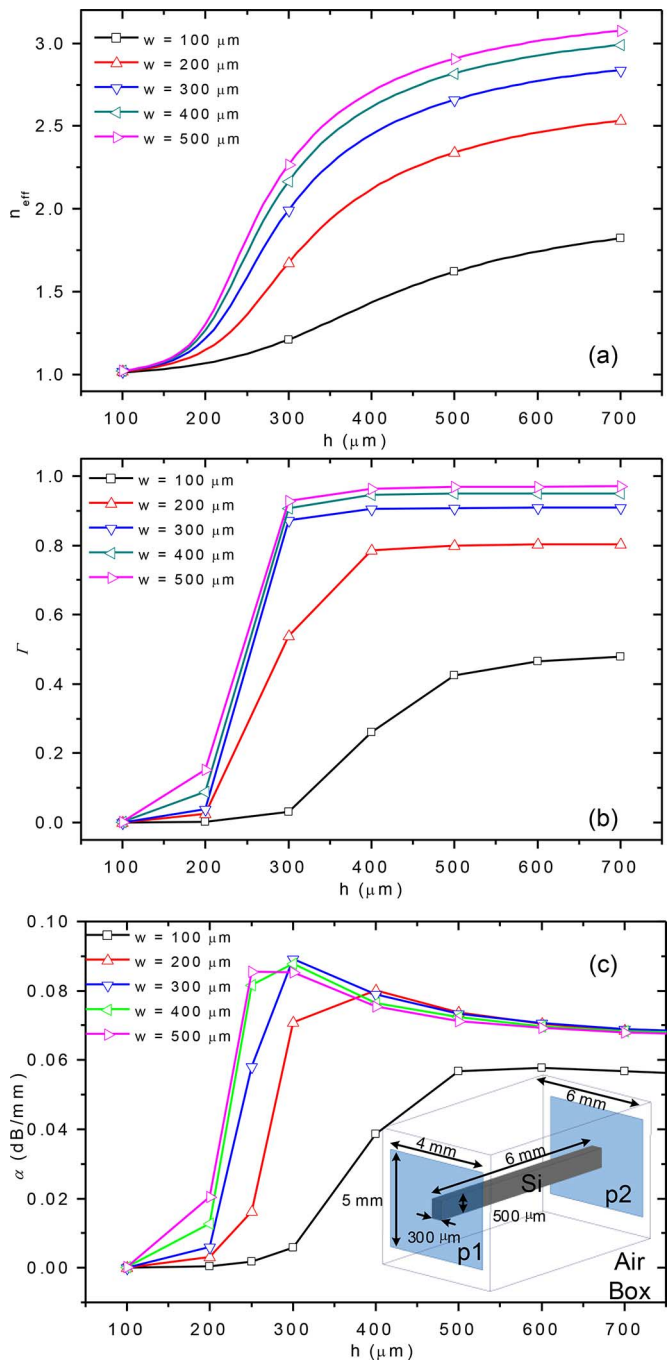

Fig. 3. (a) Calculated effective index, (b) simulated confinement factor, and (c) simulated attenuation constant 200 GHz with various h values. The inset of (c) shows the HFSS simulation setup labeled with waveguide dimensions (p1 and p2 are wave ports).

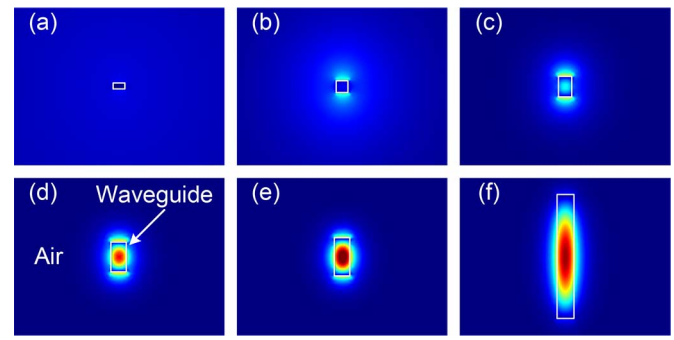

Fig. 4. Cross section views of magnitude of the E-field distribution with 200-μm w at 200 GHz with different channel height (a) $h = 100$ μm, (b) $h = 200$ μm, (c) $h = 300$ μm, (d) $h = 400$ μm, (e) $h = 500$ μm, and (f) $h = 1500$ μm.

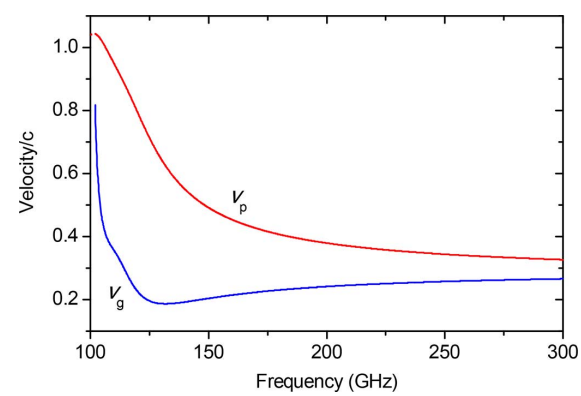

Fig. 5. Simulated phase velocity v_p and group velocity v_g as a ratio of the free-space value c for the channel with 6-mm l, 300-μm w, and 500-μm h.

unshielded characteristic, the size of the wave port in simulation is set significantly larger than the cross section. The channel is enclosed by an air box with radiation boundary. Γ is given by

$$\Gamma = \frac{P_{\text{in}}}{P_t} \tag{1}$$

where P_{in} is the power inside the waveguide, and P_t is the total cross section power. Γ represents how much EM wave energy is propagating inside the dielectric channel. It can be seen that at small w and h (compared to the propagation wavelength λ_g, which is about 1.3 mm at 200 GHz, the wave is weakly confined and has a large portion of wave propagating outside the channel. At large w and h (>300 μm), the wave is mostly confined inside the silicon channel, with n_{eff}, Γ, α values saturating with larger dimensions. The cross section views of electric field distribution with various h are plotted in Fig. 4. It is observed that larger portion of the electric field is confined within the waveguide as h increases. The attenuation constant α is a weak function of w due to the mode polarization along h direction.

The dispersion is another important aspect to optimize this channel. The phase and group velocity are utilized to check the dispersive characteristic as shown in Fig. 5. When the frequency is higher than 150 GHz, the dispersion decreases. Therefore, from a bandwidth point of view, it is desirable to operate at either the weakly or strongly confined states. However, from a loss point of view, we prefer to avoid the weakly confined region even though its straight channel loss is lower. This is due to the excessive radiation loss caused by the bending structures and large cross-talk among channels when waves are not confined. It is noted that the attenuation constant is still low (<0.09 dB/mm from simulation) for the highly confined case.

Isolation is also important with multiple channels, which is dependent on the channel space. The simulated isolation versus channel space is shown in Fig. 6. To achieve 30-dB isolation criteria, the minimum space s is 480 μm between two channels for $l = 6$ mm, $w = 300$ μm and $h = 500$ μm at 200 GHz. s will scale down with the increase of the operating frequency, since

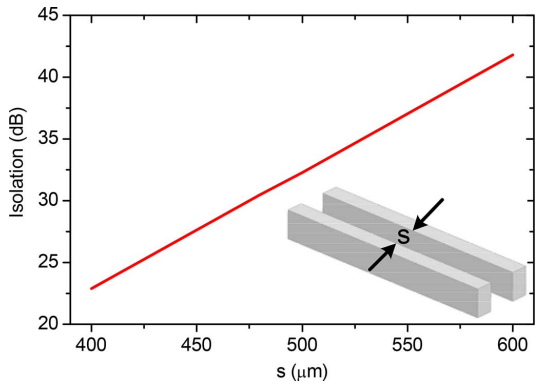

Fig. 6. Isolation between two identical 6-mm straight channels versus channel space s with 300-μm w and 500-μm h at 200 GHz.

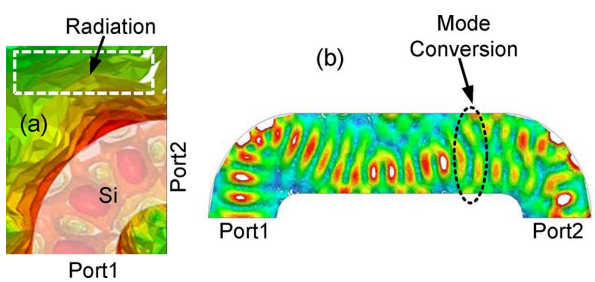

Fig. 7. (a) Simulated radiation loss and (b) mode conversion loss illustrated by HFSS simulations.

the dimensions of the channel are inversely proportional to the operating frequency.

C. Radiation Loss

To implement the intrachip/interchip interconnect for planar processes, the bending structure is the most intuitive and convenient approach. However, the bending structures may introduce additional loss due to radiation and mode conversion as shown in Fig. 7. Bending structure has been studied as early as the 1920's [33]. Researchers have reported very low bending loss designs [27], [28]. However, these works are for electrically large bending structures, such as [27] with about 113 wavelengths and [28] with about six wavelengths. Because the practical constraints of integrated circuit fabrication and packaging, a large bending structure is not feasible to integrate, and the investigation of a small bending structure is needed.

Radiation loss is caused because the portion of EM waves leaking into the air cannot preserve the phase front after the bending. As shown in Fig. 7(a), the portion of the waves propagating in air does not follow the curvature of the bend and results in the power loss. A method proposed in [34] can be used to analyze the radiation loss. The bending structure can be divided into infinitesimal sections as shown in Fig. 8. Considering each section as an array of point sources [35] and assuming that the power beyond the first null of the beam, that is, the power in minor lobes, will be lost after bending, the attenuation constant is defined as

$$\alpha_{\text{rad}} \approx \frac{1}{Z_c}\frac{P_l}{P_t} \tag{2}$$

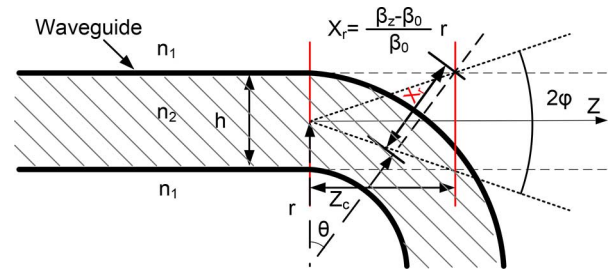

Fig. 8. Bending loss mechanism analysis diagram [34].

where P_l is the power loss through radiation, P_t is the total cross section power, and Z_c is the field propagation distance with a unit power loss [34]. Based on diffraction theory, Z_c is derived as

$$Z_c = \frac{h/2}{\tan\varphi} = \frac{h/2}{\tan\left[\sin^{-1}\left(\frac{\lambda_g}{h}\right)\right]} \approx \frac{h^2}{2\lambda_g} \tag{3}$$

where h is the channel height, φ is the half beam angle, and the λ_g is the guided wavelength in the channel. P_l and P_t can be obtained from

$$P_l = \int_{X_r}^{\infty} H^2(x), \tag{4}$$

$$P_t = \int_{-\infty}^{\infty} H^2(x)dx \tag{5}$$

where $H(x)$ is the magnetic field distribution, and X_r is the distance from the waveguide center to the position of the first null. Beyond the radius $(r + X_r)$, the waves phase velocity would have to exceed the velocity of unguided waves, which results in the loss of the corresponding wave power. To preserve the phase front [34], X_r has the relationship of

$$(r + X_r)\frac{d\theta}{dt} = \frac{\omega}{\beta_0}. \tag{6}$$

In addition, $H(x)$ is given by

$$H(x) = \begin{cases} H_0\cos(mx), & -\frac{h}{2} \le x \le \frac{h}{2} \\ H_0\cos\left(m\frac{h}{2}\right)e^{-C_0(|x|-\frac{h}{2})}, & \text{else} \end{cases} \tag{7}$$

where H_0 is the amplitude of $H(x)$, C_0 is the decay rate along the h direction, and m is the mode number. Substituting (3), (4), and (5) into (2) yields

$$\alpha_{\text{rad}} = \frac{\frac{1}{2C_0}\cos^2\left(m\frac{h}{2}\right)e^{-2C_0\frac{\beta_z-\beta_0}{\beta_0}r}2\lambda_g e^{C_0 h}}{\left[\frac{h}{2} + \frac{1}{2m}\sin(mh) + \frac{1}{C_0}\cos^2\left(m\frac{h}{2}\right)\right]h^2} \tag{8}$$

where r is the channel radius, β_z is the guided propagation constant, and β_0 is the propagation constant in free space. By multiplying the EM waves propagation distance l, the arc length of a quarter circle, the radiation loss for a bend is given by

$$\text{Loss} = \alpha_{\text{rad}}l = \alpha_{\text{rad}}\frac{\pi r}{2}. \tag{9}$$

Note that although (9) shows a linear relationship between *Loss* and r, the α_{rad} term is also dependent on r with an e^{-r} re-

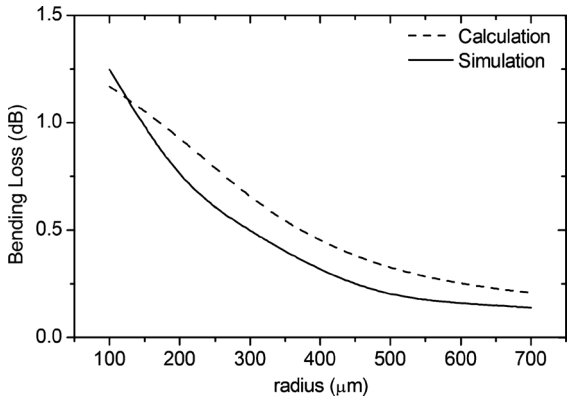

Fig. 9. Calculated and simulated bending loss with respect to r at 200 GHz with 200-μm w and 500-μm h.

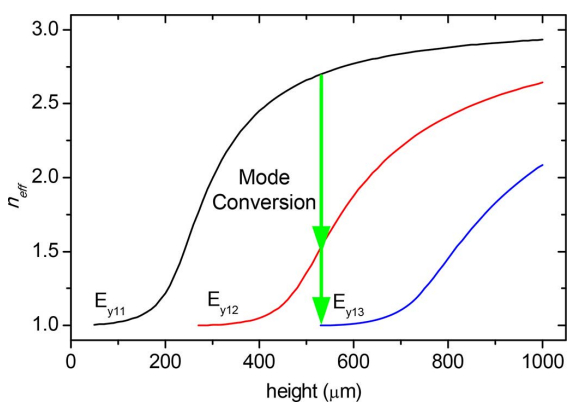

Fig. 10. Calculated n_{eff} versus frequency for the first three modes at 200 GHz with 300-μm w.

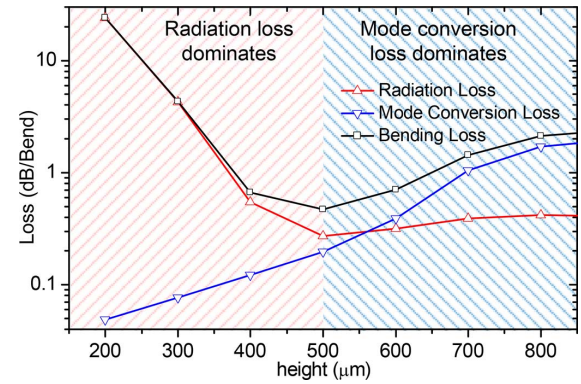

Fig. 11. Simulated total bending loss versus h at 200 GHz with 300-μm w and 300-μm r.

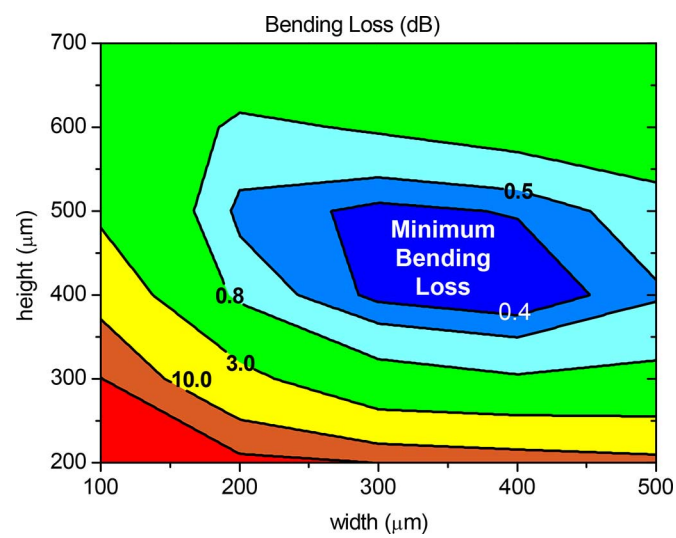

Fig. 12. Simulated total bending loss versus h and w at 200 GHz with 300-μm r.

lationship, which decays much faster. Therefore, the radiation loss is lower for a larger r, which is verified in Fig. 9 with both analytical and full-wave simulation results. The theoretical radiation loss analysis at the bend is based on Fig. 8 by assuming the bending structure has infinite width in the w direction. In a real case, the width is finite. Hence, the field distributions are not exactly same, which is responsible for the major discrepancy between theoretical and simulated results in Fig. 9.

D. Mode Conversion Loss

The discussions so far seem leading to a conclusion that a waveguide with large w, h, and r has smaller bending loss. However, the large waveguide dimensions may introduce a competing loss mechanism by introducing mode conversion as shown in Fig. 7(b).

Mode conversion can lead to additional loss when w and h of the waveguide are large enough to allow multiple modes to exist at the operating frequency. The issue is exacerbated by the bending structure of the proposed interconnect scheme. Fig. 10 shows n_{eff} of several possible modes for a channel of $w = 300$ μm at various h values. For example, the E_{y11} mode may be converted to E_{y12} mode when h is larger 260 μm after bending.

Fig. 11 shows the bending loss, consisting of radiation loss and mode conversion loss, versus h with a fixed r of 300 μm and a fixed w of 300 μm at 200 GHz. Multi-mode wave ports are used in HFSS to extract the power conversion among the lowest three modes. When h is less than 500 μm, radiation loss dominates. Smaller height leads to a larger portion of the waves leaking into the air and causes larger radiation loss as shown by the curve with up triangles. When h is larger than 500 μm, higher order modes may be excited and propagate, causing increasing mode conversion loss as shown by the curve with down triangles. The total loss is plotted as the curve with squares. The minimum loss of 0.3 dB occurs around 500 μm.

A contour map of the bending loss versus w and h is plotted in Fig. 12. The minimum bending loss occurs for $h = 500$ μm and $w = 400$ μm.

E. Figure of Merit

As discussed in Section I, the performance of chip-to-chip interconnect is determined by the bandwidth density and energy efficiency. The bandwidth density is defined as bandwidth per cross section area

$$\rho_{\text{BW}} = \frac{\text{BW}}{\text{Area}}. \tag{10}$$

A larger bandwidth density means a higher spatial utilization efficiency to enable a higher data rate transmission per unit space.

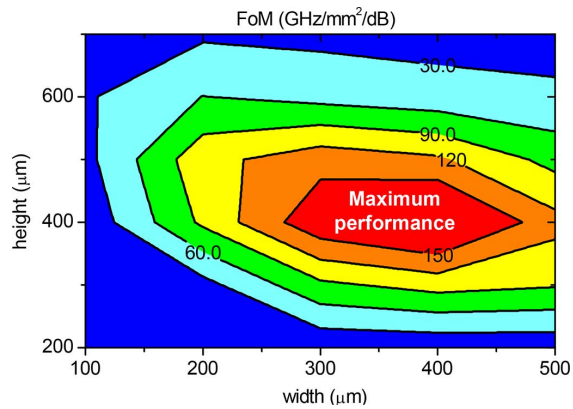

Fig. 13. FoM for sub-THz interconnect versus h and w at 200 GHz with 300-μm radius.

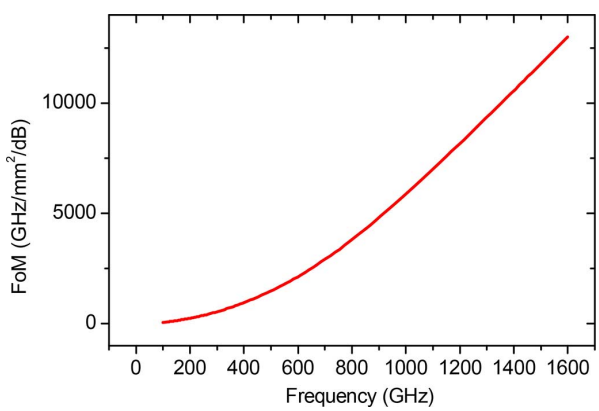

Fig. 14. FoM versus frequency for sub-THz interconnect with 6-mm l.

To evaluate the performance of sub-THz interconnect channel, we propose a figure of merit, defined as

$$\mathrm{FoM} = \frac{\rho_{\mathrm{BW}}}{\text{Channel Loss}} = \frac{\mathrm{BW/Area}}{\text{Channel Loss}(r, h, w)} \tag{11}$$

where channel loss depends on the r, h, and w of the channels. Note that the dominant loss mechanism depends on the communication distance. The total channel loss is dominated by bending loss for short distance communications ($l < 10$ mm) while material loss is the dominant factor for the longer ones. Assuming that the data bandwidth is 10% of the carrier frequency, the contour map of FoM versus h and w is plotted in Fig. 13. The highest FoM occurs around $h = 400$ μm and $w = 400$ μm.

Higher operating frequency leads to better FoM. This is because at higher operating frequencies, the optimal waveguide dimensions, h, w, and s, are all inversely proportional to the operating frequency. Assuming a constant fractional bandwidth, higher operating frequency leads to the significant increasing of FoM as shown in Fig. 14.

III. Coupling Structure

To transmit signals between IC chips and channels, coupling structures are needed with the requirements of high directivity, high radiation efficiency, and with the broadside radiation pattern. High directivity and high coupling efficiency aim to maximize the power transfer to the receiver through the interconnect channel. The reasons to choose broadside radiation patterns compared to end-fire radiation patterns are: a) better isolation due to nondirect interference from the reflected waves to the circuits in surrounding places and b) flexible channel location because the coupling structure can be located in the whole chip instead of just on the chip peripherals otherwise in end-fire radiation pattern cases.

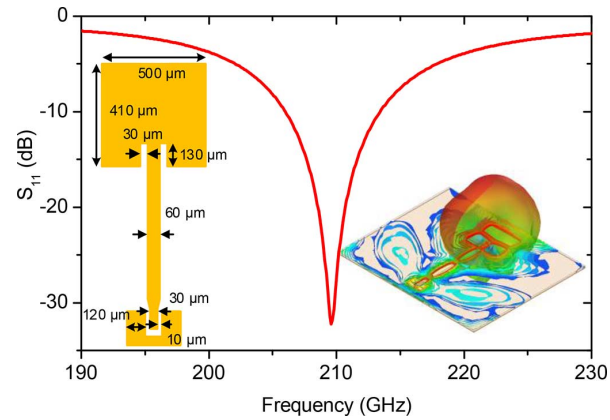

Fig. 15. Simulated S_{11} for the patch-antenna-based channel coupling structure with insets of schematic, and field distribution at 210 GHz.

In this work, a patch-antenna-based coupling structure is chosen due to the mature design method [33]. Fig. 15(a) illustrates the coupling structure. The signal is excited through a coplanar waveguide (CPW), and transitioned to a microstrip line before feeding the coupling structure Rogers 3850, with 25.4-μm thickness and dielectric constant of 2.9, is chosen as the coupling structure substrate. To simplify the fabrication, a vialess CPW to microstrip line transition is adopted [36]. In order to prevent the energy leakage through the substrate, choosing the ground plane width smaller than half wavelength of the signal avoids the generation of parallel plate modes and high order modes [37]–[39]. The dimensions of the coupling structure are labeled with EM simulation results in Fig. 15. Also, both near-field and far-field patterns are presented. From these patterns, it can be seen that the signal effectively propagates upward to the perpendicular direction from the antenna.

Noted that the coupling structure exhibits a limited bandwidth whereas the bandwidth of the dielectric waveguide is very large as shown in Fig. 17. Future demonstrations of the sub-THz interconnect concept will focus on improving the bandwidth of the coupling structures.

IV. Experimental Demonstration

A. Design of the Demonstration Setup

The simulation results of the complete sub-THz interconnect channel with a pair of patch antenna coupling structures and feeding structures are shown in Fig. 16. The waves are radiated by the coupling structure A, and then coupled to the waveguide. Propagating through the waveguide, the waves are collected by the coupling structure B. Fig. 16(a) also shows partial portions of EM waves leaking into air due to the bending structure causes coupling loss. Besides, a larger beam width compared with waveguides cross section size also results in a finite power collection capability. The simulated S_{21} as shown in

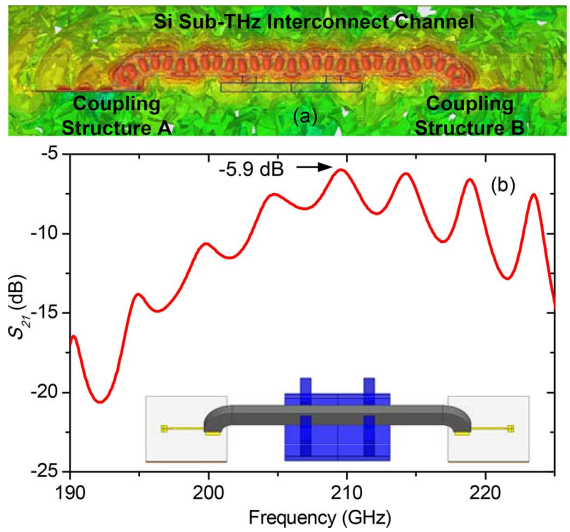

Fig. 16. (a) Simulated magnitude of E-field distribution of a complete sub-THz interconnect channel with a pair of channel feeding structures at 210 GHz and (b) simulated S_{21} with 300-μm w, 500-μm h, and 300-μm r.

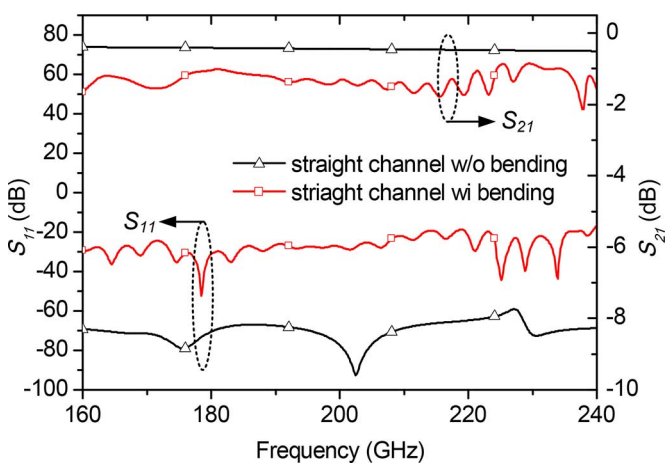

Fig. 17. Simulated S-parameters versus frequency for the straight silicon channel waveguides without or with bending structure with 6-mm l, 300-μm w, 500-μm h, and 300-μm r.

Fig. 16(b) indicates the minimum insertion loss of 5.9 dB of the complete interconnect structure. The bandlimited behavior S_{21} is due to the limited bandwidth of the patch antenna; the silicon channel waveguide itself is very wideband as shown in Fig. 17.

B. Fabrication

The fabrication processes of the sub-THz interconnect channel are summarized in Fig. 18. A 500-μm-thick HR silicon wafer (resistivity of 10 000 Ω·cm) is first patterned with a thick ($\sim$17 μm) photoresist (AZ9260) to define the waveguide geometries: h and r. Then, the HR silicon wafer is attached to a carrier substrate and etched through in a DRIE process. The individual channels are isolated after etching. Fig. 19(a) shows the photographs of the channel from a different perspectives. Note that the silicon waveguide is etching from the side view to simplify the fabrication complexity as shown in Fig. 18(a)(3).

The coupling structure is fabricated on a Rogers 3850 substrate. Photolithographic thin-film patterning is used to achieve a fine feature definition. One side of the copper laminate is

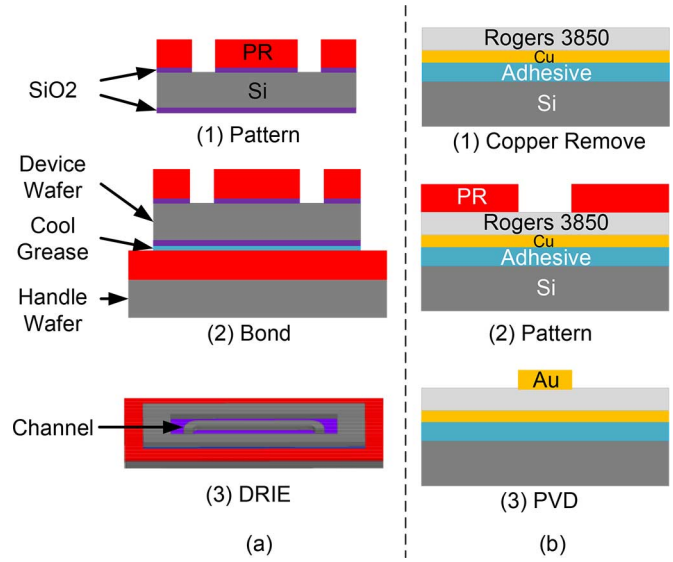

Fig. 18. Fabrication procedure of (a) the silicon channel and (b) the patch antenna.

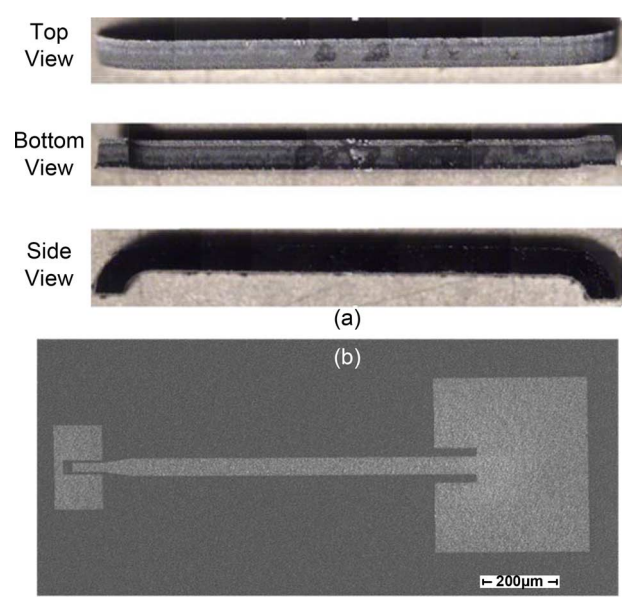

Fig. 19. (a) Photographs of the channel from different perspective and (b) SEM photograph of the patch antenna.

completely removed first. The antenna structure is then patterned with a Ti/Au thin film of thickness 50/300 nm by a lift-off process. Fig. 19(b) shows the fabricated scanning electron microscope (SEM) photograph of the antenna coupling structure.

A 3-D-printed holder with a low dielectric constant material (Acrylate-based polymer, $\varepsilon_r \approx 2.7$) is used to support the channel. According to the full-wave simulations, the holder introduces negligible effects on the signal propagation. The alignment of the channel and two coupling structures is very critical. To ensure good alignment, the channel holder and alignment marks are introduced. The channel holder is first attached to the two alignment marks, which should be put exactly between alignment marks; the holder's slot, where the channel is to insert, is then in the center of alignment marks and holds the channel.

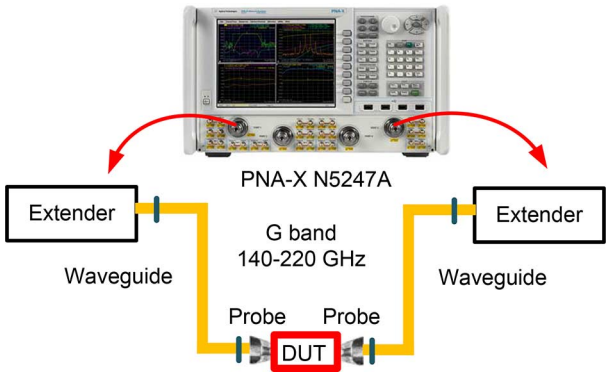

Fig. 20. Schematic of the test bench.

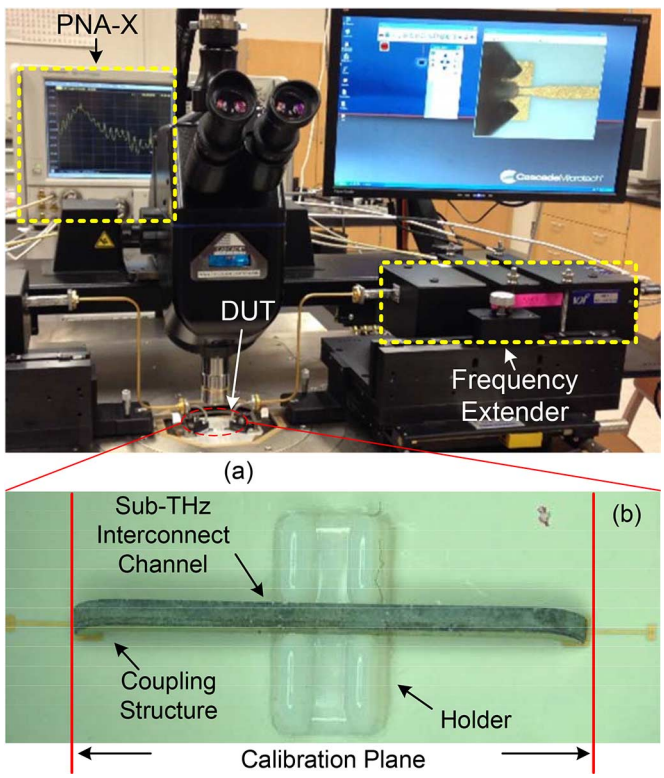

Fig. 21. (a) Photograph of the test bench and (b) the zoom-in picture of the channel with the holder.

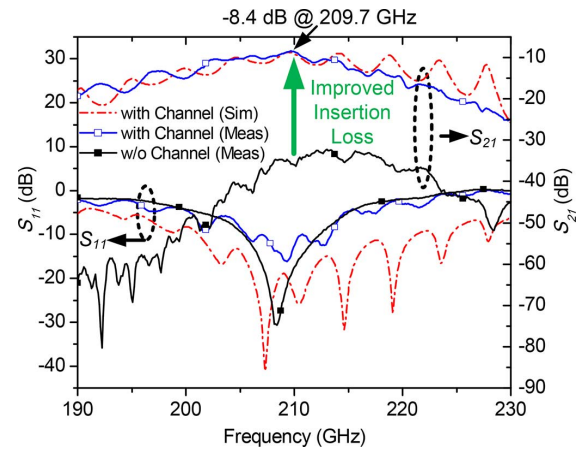

Fig. 22. Comparison of measured and simulated S-parameters (with extracted material parameters) with 6-mm l, 500-μm h, 500-μm w, and 300-μm r and the case without the sub-THz interconnect channel.

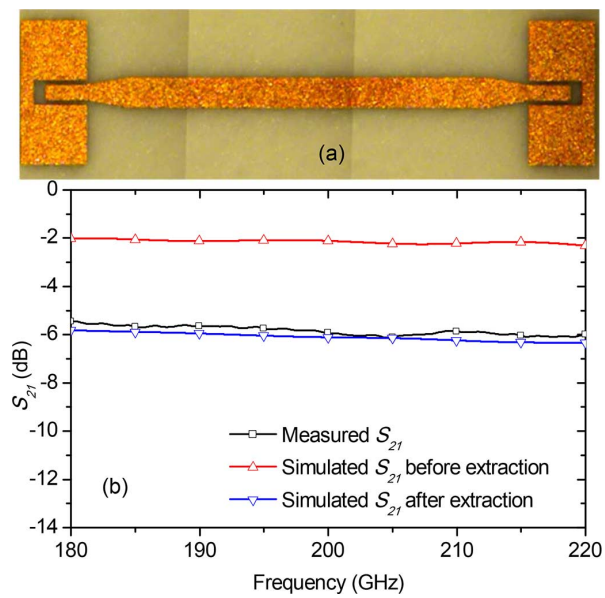

Fig. 23. Measured and simulated S_{21} of the fabricated transmission line before and after extraction of loss tangent of a Rogers 3850 board and metal conductivity by including titanium and gold together. The length of the transmission line is 5.1 mm.

C. Measurement Results and Discussions

Figs. 20 and 21 illustrate the measurement setup, which is based on an Agilent network analyzer (PNA-X N5247A). A pair of Virginia Diodes frequency extension modules (VDI WR5.1-VNAX) up-converts the signal frequency to G band (140–220 GHz). WR-5 waveguides are used to guide the wave toward the tip of the probes. The Short, Open, Load, Thru (SOLT) calibration method is employed to set the reference plane at the edge of the patch antenna for each side. The measured interconnect path includes two patch-antenna-based coupling structures and the sub-THz interconnect channel.

Fig. 22 shows the comparison of measurement results between the cases with and without the sub-THz interconnect channel, which indicates the insertion loss is significantly improved. Fig. 23 also shows the measured S-parameters comparing with the simulation results after using extracted material parameters, specifically the substrate loss tangent and metal effective conductivity. The minimum insertion loss is 8.4 dB, which is about 2.5 dB higher than the simulation result in Fig. 16(b) due to two major reasons. First, the real loss tangent of the substrate for the coupling structure is larger than their typical values at such high frequencies, with the extraction method described in the next paragraph. Second, titanium is used as an adhesion layer under the gold thin film. Because the skin depth of gold and titanium at 210 GHz are 172 and 807 nm, separately, the underlying titanium layer with 50-nm thickness can be penetrated completely. The effective conductivity of the Ti/Au thin-film is extracted to be 2.92×10^7 S/m.

The substrate loss tangent is extracted through fabricated transmission lines as shown in Fig. 23(a). After comparing the S_{21} between measurement and simulation results, the extracted loss tangent is 0.053, as compared to 0.0067 at 98.5 GHz [40].

Fig. 23(b) shows the comparison among measured S_{21} and simulated S_{21} before and after extraction. By using the extracted material parameters, the updated simulated S-parameters have a good agreement with measurement results as shown in Fig. 22.

V. Conclusion

This paper for the first time presents the design, analysis, and demonstration of a micromachined silicon dielectric waveguide-based sub-THz interconnect channel for silicon planar integrated circuits. A detailed analysis of channel losses, including radiation loss and mode conversion loss, channel size optimization for the bending, fabrication procedure, and the measurement setup have been conducted. To quantify the design optimization, an FoM is also defined. The analytical, simulated, and measured results agree well, demonstrating much lower loss than other electrical interconnect methods while maintaining better process compatibility than optical interconnect. In addition, this technique can be readily scaled up to THz frequencies due to a better FoM at higher frequencies. Therefore, the authors envision that THz interconnect has the potential to eventually solve the long-standing interconnect problems of intrachip/interchip communications.

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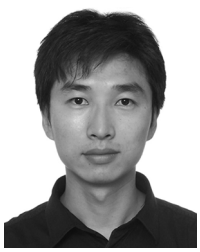

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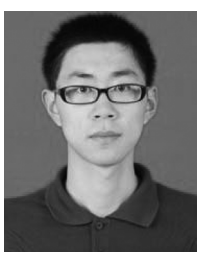

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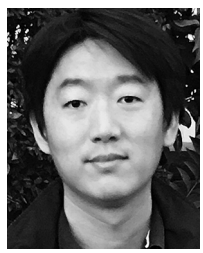

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