THz Interconnect: The Last Centimeter Communication

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ABSTRACT

Terahertz, sandwiched between conventional microwave and optical frequencies, has inspired increasing interest due to its uniqueness and high potential applications, such as imaging, sensing, and communications. This article, on the other hand, focuses on one emerging application of the terahertz spectrum: THz interconnect. Intra-/inter-chip communication has doubled every two years over recent decades, and the trend is projected to continue in the future. However, the bandwidth supportable by chip I/O pins cannot keep up with the requirement, which forms the increasing gap between the bandwidth requirement and support capability, or the interconnect gap. To ultimately solve the problem and close the gap, both bandwidth density and energy efficiency should be boosted. THz interconnect holds high potential to boost key performance by leveraging the advantages of both high-speed electronics devices and low-loss quasi-optical channels. This article discusses THz interconnect from different aspects: system architecture, circuit specifications, design challenges, and non-ideality effects. Particularly, this article exemplifies both active and passive circuit design techniques for THz interconnect, a 140 GHz transceiver and a terahertz generator in 65 nm CMOS technology, and a low-loss and process-compatible silicon waveguide channel. THz interconnect opens high potential new revenue to solve the long-standing interconnect issue.

INTRODUCTION AND MOTIVATION

Continuous scaling of semiconductor devices allows more processor cores and integrated functionalities into a single chip to support the growing computation demands of scientific and commercial workloads in both speed and volume [1, 2]. This trend mandates an ever increasing inter-/intra-chip communication bandwidth, which has been a big challenge over recent decades. This challenge has motivated active research to improve interconnect capacities, characterized by two key specs: bandwidth density, defined as gigabits per second per square millimeter, determining the aggregate throughput; and energy efficiency, defined as Joules per bit, indicating the overall power consumption. The required off-chip I/O bandwidth doubles about every two years, significantly exceeding the growth rate of the number of pins due to packaging/assembly limitations [3]. The gap between the interconnect requirement and the capability forms the "interconnect gap." Given state-of-art (SOA) performance of energy efficiency and bandwidth density, the power consumption and chip size to support interconnect only will be overwhelming for most computers and embedded systems [4]. In addition, cost, defined as dollars per gigabit per second, needs to scale down over the increasing interconnect bandwidth. To sustain the continuous demands for system performance unmet by the current intra- interconnect capabilities, the interconnect gap must be filled.

There are two major research areas in the interconnect: electrical interconnect (EI) [5] and optical interconnect (OI) [4, 6]. The existing SOA has demonstrated a bandwidth density of about 37 Gb/s/mm^2 for OI [4] and 8 Gb/s/pin for EI [5] with energy efficiency of about 4 pJ/bit [5, 6]. However, it is challenging for both EI and OI to completely address the interconnect issues individually. The major limitation of EI is the low bandwidth-distance product of the metallic medium. Therefore, its energy efficiency drops significantly when transmitting large throughput over a > 1 mm distance due to the prohibitive channel losses. The fiber has unpreceded bandwidth-distance product, which makes it ubiquitous for long distance communication, such as wide area networks (WANs) and metropolitan area networks (MANs). However, OI faces the issues of system integration complexity and overhead, such as electronic-to-optical and optical-to-electronic (EO/OE) conversion, environment sensitivity, and high cost of short-distance communications (e.g., < 10 cm). All of these render the *last centimeter* dilemma, which falls into the distance range for inter-/intra- chip communications.

THz Interconnect (TI), utilizing the frequency spectrum sandwiched between microwave and optical frequencies, has high potential to complement EI and OI by leveraging the advantages of both electronics and optics as shown in Fig. 1a. Continuous scaling of mainstream silicon technologies enables terahertz electronics in silicon, such as a terahertz oscillator [7–9] and detector [10, 11], making terahertz signal generation/detection possible and suitable in silicon

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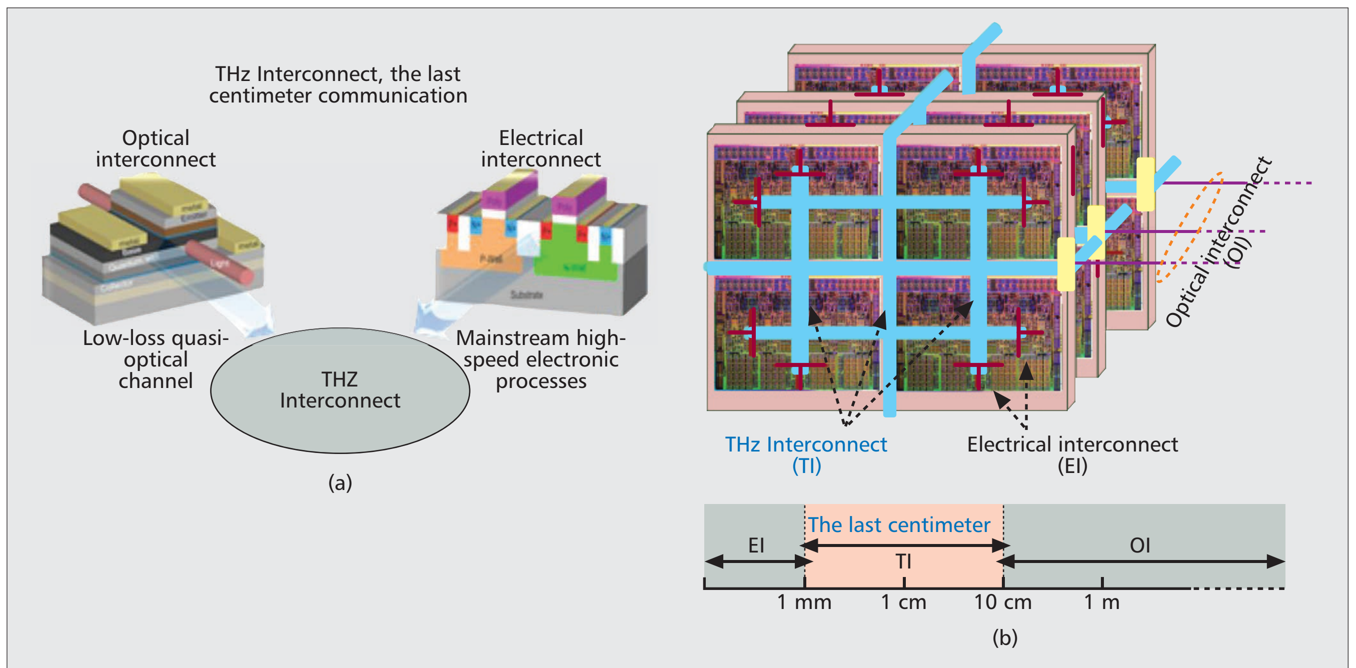
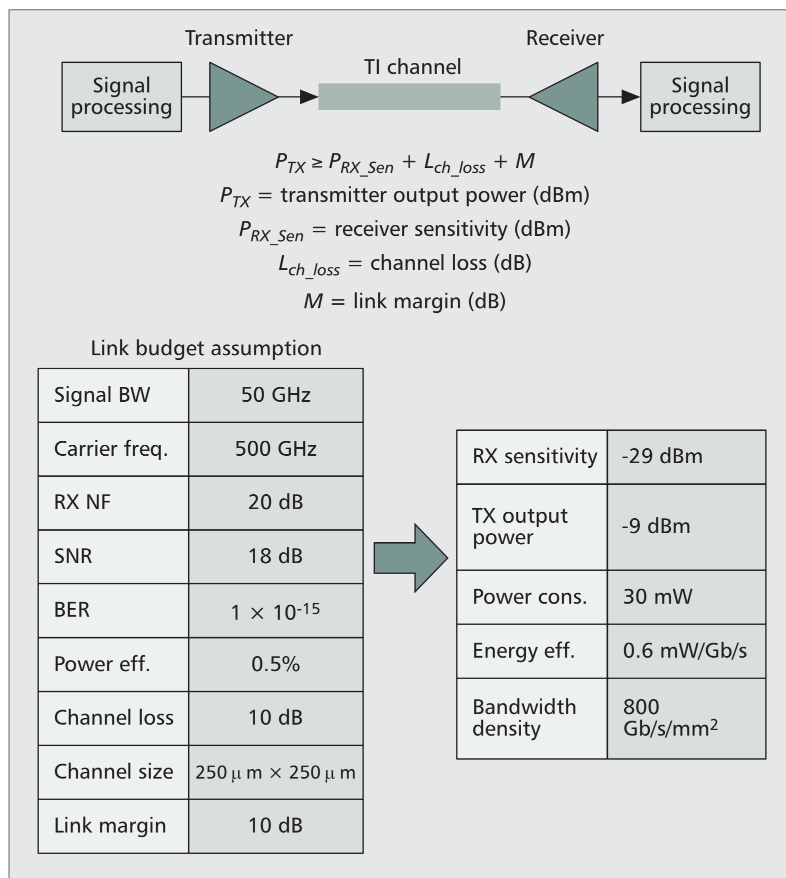


Figure 1. a) THz Interconnect leverages the advantages of both electrical interconnect and optical interconnect; b) THz Interconnect complements EI and OI to serve as the last centimeter data link.

processes. On the other hand, terahertz waveguides, similar to their optical counterparts, have small dimensions and present low loss with an attenuation factor < 0.04/cm [12, 13]. The ultra-low-loss feature alleviates the TI link budget to allow low transmission output power and improves TI energy efficiency. In addition, TI favors technology scaling because the increasing frequency supports higher communication data rates and reduces channel dimensions, thus resulting in a larger bandwidth density. These unique features of TI enable it to complement EI and OI, with one optimum architecture shown in Fig. 1b for high energy efficiency, high bandwidth density, low cost, and high resilience. As shown in Fig. 1, the TI aims to address the last centimeter dilemma between 1 mm and 10 cm, while EI and OI address the issues in their most effective operation regions to ultimately fill the interconnect gap.

THz Interconnect Link Budget Analysis

One stringent requirement of interconnect is an ultra-low bit error rate (BER), demanding high signal-to-noise ratio (SNR). To realize high-efficiency systems, simple modulation schemes, such as binary phase shift keying (BPSK) or amplitude shift keying (ASK), are preferred. Figure 2 analyzes the link budget suggested by simulation and measurement results from a 65 nm complementary metal oxide semiconductor (CMOS) technology. With the ASK scheme, a data rate of 50 Gb/s requires 50 GHz bandwidth due to the 1 b/Hz bandwidth efficiency. The assumption of 10 percent fractional bandwidth leads to 500 GHz carrier frequency. To achieve BER < 1×10^{-15}, the SNR must be > 18 dB. With a 20 dB noise figure, the receiver sensitivity is about –29 dBm. The loss from the channel, including the signal coupling from/to the transceiver and channel itself with 10 mm length, is assumed to be 10 dB. The loss is mostly dominated by the channel coupler with the loss from the channel itself < 0.08 dB/mm, based on the discussion below. Therefore, the loss does not change much with long channel length. With the link budget margin of 10 dB, the output power from the transmitter is therefore about –9 dBm. With 0.5 percent efficiency at the transmitter side, the DC power consumption is about 25 mW from the transmitter. The receiver consumes less power than the transmitter. Here, 5 mW power budget is allocated to the receiver, which leads to total power consumption of 30 mW for the entire transceiver, and the resulting energy efficiency is 0.6 mW/Gb/s or 0.6 pJ/b. With regard to the bandwidth density, the interconnect size needs to be evaluated, which is mostly constrained by the channel dimension and is about 0.25×0.25 mm^2 in Fig. 2's system assumption. Therefore, the bandwidth density can be estimated to 50 Gb/s/(0.25*0.25) = 800 Gb/s/mm^2. This link budget analysis is based on 65 nm CMOS technology speed and capabilities. The device f_T in 65 nm CMOS technologies is about 200 GHz. To support 500 GHz operation, novel circuit architecture and design techniques are required. This is exemplified below. With more advanced technologies, such as 40 nm and 28 nm processes, the increasing carrier frequency is able to support a larger signal bandwidth and higher data rate while using a smaller channel size. Therefore, the bandwidth density can increase quadratically with the carrier frequency. In addition, a higher device speed supports better DC-to-RF conversion efficiency for a better interconnect energy efficiency. Moreover, all the active circuits are based on standard mainstream processes, which provides the most cost-effective



Link budget assumption	
Signal BW	50 GHz
Carrier freq.	500 GHz
RX NF	20 dB
SNR	18 dB
BER	1×10^{-15}
Power eff.	0.5%
Channel loss	10 dB
Channel size	250 μm × 250 μm
Link margin	10 dB

RX sensitivity	-29 dBm
TX output power	-9 dBm
Power cons.	30 mW
Energy eff.	0.6 mW/Gb/s
Bandwidth density	800 Gb/s/mm^2

Figure 2. THz Interconnect link budget analysis, and the corresponding energy efficiency and bandwidth density based on 65 nm CMOS technology.

implementation and high resilience. Therefore, TI scales well with processes to be able to ultimately close the interconnect gap by providing scalable interconnect capabilities.

Active Circuit Design Challenges and Example

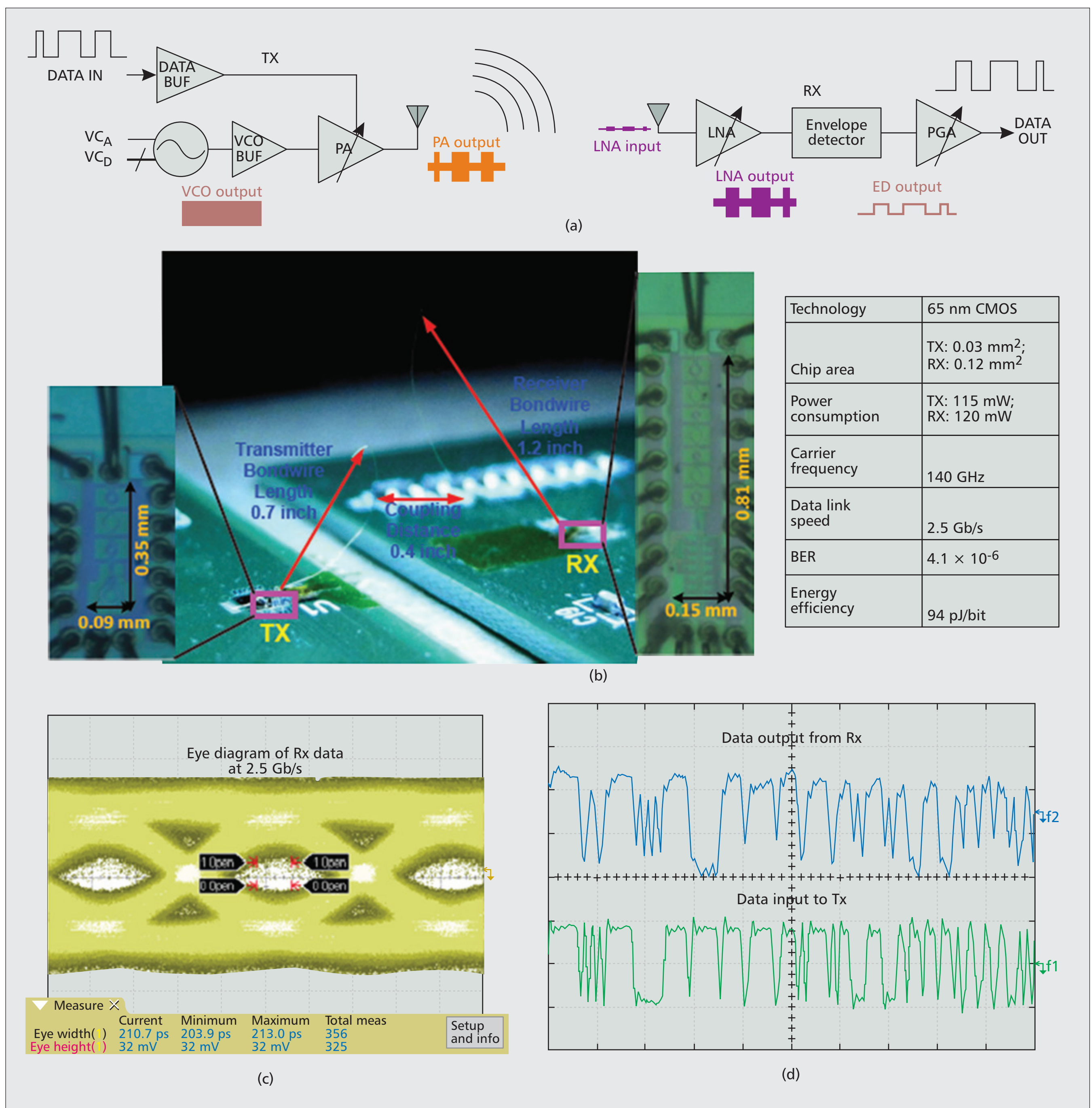
As shown in Fig. 2, active transceivers supporting high data rate with small power consumption are the key to TI. In such high frequency spectrum, spectrum usage efficiency is not as a serious concern as in the lower gigahertz range. Therefore, simple modulation schemes, such as ASK and BPSK, can be adopted to reduce hardware complexity and power consumption while still offering high communication data rates by leveraging the wide bandwidth. Among them, on-off keying (OOK) modulation, the simplest form of ASK, represents the data as the presence or absence of a high-frequency carrier through binary amplitude modulation.

To demonstrate the feasibility, we have developed a non-coherent OOK-based transmitter/receiver for short-distance communications, such as inter-/intra-chip interconnect [14]. Figure 3a sketches the system architecture. In the transmitter, a voltage-controlled oscillator (VCO) generates a high-frequency signal running at 140 GHz as the carrier, and a VCO buffer isolates the VCO core from the OOK modulated power amplifier (PA) to stabilize the carrier frequency and support a large carrier signal. The data modulates the PA input and intermediate nodes together to achieve high modulation depth, > 90 percent. The differential switching configuration by crossing the differential signals is equivalent to reduce the channel resistance to increase modulation speed. In the receiver, the low-noise amplifier (LNA) provides over 20 dB power gain with more than 20 GHz bandwidth centered at 142 GHz. An envelope detector directly demodulates the incoming OOK RF signal into a low-frequency baseband signal, which is then amplified by the following PGA before sending it off-chip.

The 140 GHz TX and RX are fabricated in a 65 nm CMOS technology. To characterize the data link, the TX and RX chips are placed in close proximity (~1 cm) and coupled with bonding wires, as shown in Fig. 3b with chip photos shown as insets. The performance is summarized in the table. The tested data rate is 2.5 Gb/s with a pattern of 2^{15}–1 pseudo-random binary sequence (PRBS). Figure 3c shows the receiver output signal eye diagram with the eye height about 32 mV and eye width about 210 ps. Figure 3d presents the comparison of the data sequence between the input data to the TX and output data from the RX, which clearly indicates a successful link. The measured BER is 4.1×10^{-6}. In this design, the 2.5 Gb/s data rate is mainly limited by the baseband VGA speed, which needs to drive off-chip 50 ohm and only provides 1.2 GHz bandwidth. In practical interconnect scenarios, driving 50 ohm may not be necessary. Therefore, the baseband speed can be designed higher to support larger throughput. In addition, due to the inefficient bonding wire coupling, which indicates > 40 dB loss from simulation, the SNR significantly drops, which degrades BER. With a better coupler design, such as patch antenna or dipolar antenna based couplers, the energy efficiency and communication distance can be improved.

One of the key issues of this transceiver is that the 140 GHz carrier frequency is not high enough to efficiently support data rate higher than 50 Gb/s. In addition, the corresponding passive component size is also large to considerably constrain the bandwidth density. For example, an on-chip patch antenna at 140 GHz occupies about 1 mm^2 chip area.

To boost the energy efficiency and bandwidth density, the carrier frequency needs to be increased to be able to support wide bandwidth and high data rates as well as reduce the passive device sizes. Traditional transit-time-based electronic devices are typically limited by their low cutoff frequencies (i.e., f_T and f_{MAX}). Despite a continuous increase in the device cutoff frequencies, deep-scaled CMOS technologies still suffer major drawbacks in realizing terahertz circuits and systems. First, external parasitics limit circuit operating speed to much lower than device-intrinsic speed due to charging/discharging parasitic capacitance. This scenario becomes even worse with technology scaling due to a larger ratio of external parasitics over intrinsic device loading. Second, a CMOS device demonstrates large losses with a combination ohmic losses



Technology	65 nm CMOS
Chip area	TX: 0.03 mm^2; RX: 0.12 mm^2
Power consumption	TX: 115 mW; RX: 120 mW
Carrier frequency	140 GHz
Data link speed	2.5 Gb/s
BER	4.1×10^{-6}
Energy efficiency	94 pJ/bit

Figure 3. a) OOK-based 140 GHz transceiver for short distance communications; b) the measurement configuration coupled by bonding wires with the chip photos shown in insets and performance summary; c) measured receiver output eye diagram; d) the data sequences of transmitter input and receiver output.

from contacts and metal resistance, and dielectric losses from substrate coupling. These losses degrade circuit quality factor and reduce signal gain, which are particularly severe in terahertz operations and result in the challenge of generate terahertz signals. Third, ultra-high-frequency generation faces big challenges due to small available gain. This is because ultra-high-frequency operation requires small active and passive components, resulting in insufficient signal gain. Increasing signal gain can possibly be achieved by increasing active device size or passive device size. Increasing active device size boosts signal gain, but at the cost of larger capacitance loading, which then shifts down the operating frequency. Increasing passive device size, on the other hand, demands size reduction of the active components, which then reduces the transconductance and drops the overall signal gain. These are active terahertz circuit design dilemmas.

To overcome the above design issues, we have invented a new signal generation architecture, composed by a frequency-selective negative resistance (FSNR) tank, to generate the oscillation frequency higher than device cutoff fre-

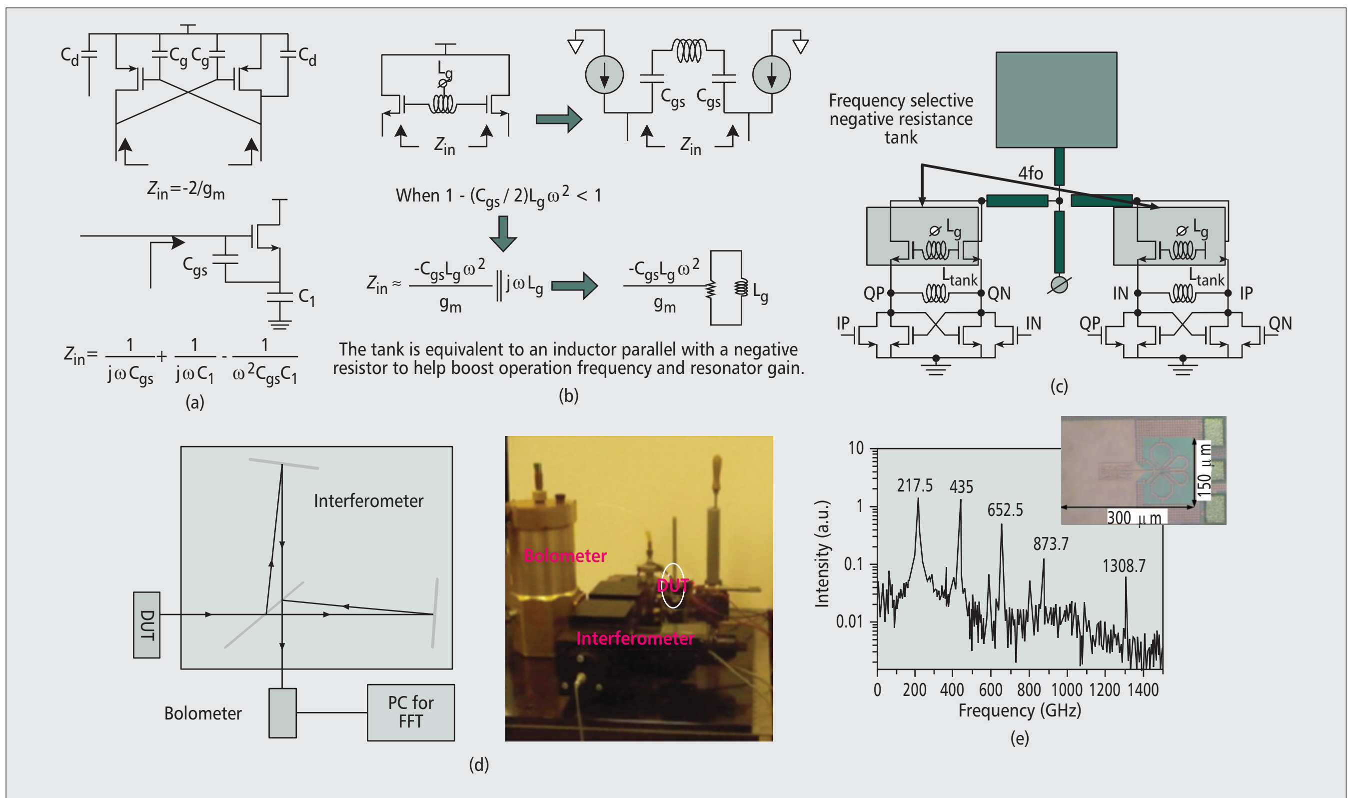


Figure 4. a) Conventional negative resistance generation mechanisms that introduce extra capacitance; b) the working mechanism of the proposed frequency-selective negative resistance tank; c) the complete terahertz generation circuit with fourth order harmonic enhancement by double push-pull scheme; d) the Michaelson interferometer measurement setup; e) the measured output spectrum with die photo shown in inset.

quency [7]. The key challenges in conventional signal generation are the small signal gain due to low quality factor Q passives and low operating frequency due to parasitic loading. To boost the signal, an extra negative resistance can be used to compensate for the tank loss. However, the well-known negative resistance generation circuits introduce extra capacitance loading. For example, Fig. 4a shows two negative resistance generation circuits: cross-coupled pairs with negative resistance of $-1/(2g_m)$, and the gate input impedance with source capacitor degeneration producing negative resistance of $-1/(\omega^2 C_{gs}C_1)$. The extra capacitance (e.g., C_g, C_d, C_{gs}, and C_1) lowers the overall operating frequency and defeats the purpose of ultra-high-frequency generation.

Therefore, the goal is to identify a circuit that can generate a negative resistance while not presenting extra capacitance. Figure 4b is the circuit configuration that satisfies this requirement. The input impedance looking into the source, Z_{in} presented in Fig. 4b, demonstrates negative resistance in a selected frequency range. When the operating frequency is high enough to satisfy $1 - (C_{gs}/2)L_g\omega^2 < 1$, the equivalent circuit can be presented as an inductor L_g parallel with a negative resistance of $-C_{gs}L_g\omega^2/g_m$, as shown in Fig. 4b. This feature exactly satisfies the requirement of generating negative resistance without adding extra loading capacitance. Moreover, this scheme provides extra inductance, which further boosts operating frequency when parallel with a tank. Because this situation only holds for a certain frequency range, it is called frequency-selective negative resistance (FSNR) tank. With the discovery of this resonant tank, a terahertz signal generator circuit can be formed by combining this tank with a conventional cross-coupled pair, shown in Fig. 4c. The fundamental resonant frequency increases to

$$1\Big/\sqrt{C(L_g // L_{tank})},$$

which is higher than the original resonant frequency from the cross-coupled pair,

$$1\Big/\sqrt{CL_{tank}}.$$

To further boost the operating frequency, a double push-pull structure to generate the 4th order harmonic is adopted as shown in Fig. 4c. There are a few unique features of this architecture. First, combining an FSNR tank with the primary tank boosts the resonant frequency higher than either of the individual tank resonant frequencies. This allows for larger inductance values of L_{tank} and L_g, which not only generate a larger tank impedance for higher gain, but also render on-chip inductor design more flexible and reproducible than typical super-small inductors in the terahertz frequency regime. Second, the FSNR tank provides negative resistance at the desired high resonant frequency, which ensures a high operating frequency. The additional negative resistance also relaxes a high transconductance g_m requirement of the core circuit device, which allows a

smaller device size to further boost the operation frequency and reduce the power consumption. Third, a vertical stacking structure allows a higher supply voltage without reliability concerns and increasing signal swing.

Conventional electronic apparatus is not suitable for identifying high order harmonic frequencies in the terahertz frequency range. To overcome this obstacle, a Michelson interferometer based quasi-optical measurement approach is adopted. As shown in Fig. 4d, the output signal, radiating from the vertically mounted CMOS oscillator with an on-chip patch antenna, is detected through an interferometer followed by a bolometer. The signal spectrum is then recovered through fast Fourier transform (FFT), as shown in Fig. 4e. The fundamental frequency is about 217 GHz, which is larger than 65 nm CMOS cutoff frequency, the unit current gain frequency f_T, which is about 200 GHz. The inset shows the chip photo, occupying a 0.045 mm^2 area.

The wireless communication feature of 140 GHz transceiver-based short-distance communications, shown in Fig. 3, naturally suffers from large path losses and channel interferences. In addition, the loss increases quadratically vs. the operating frequency, and is thus not favorable for frequency up-scaling. Moreover, the severe interference caused by channel crosstalk constrains simultaneous multiple channel communications and is hard to adopt in dense interconnect channel scenarios. Therefore, a wired communication channel with low loss is desired for interconnect, especially TI.

Passive Channel Design Challenges and Example

Low-loss terahertz channels have been studied extensively based on a variety of materials [15], including silicon ribbons [12], plastic ribbons and fibers [13], and so on. The silicon ribbon has demonstrated < 1 dB/m loss at frequencies up to 1 THz [12]. To reduce channel size, a subwavelength plastic fiber, with 200 mm diameter at 0.3 THz, has been demonstrated with an attenuation factor of < 0.01 cm^{-1} [13]. These low-loss channels alleviate link budget to reduce the requirements of transmitter output power and receiver noise performances to enable TI in silicon processes. However, planar silicon process compatible terahertz channels and couplers have not been investigated in previous literature. To further investigate the feasibility of terahertz channels compatible with planar silicon processes, we have designed a micro-machined dielectric waveguide-based terahertz channel.

One key specification of the TI channel is the loss. There are three major loss categories: material loss, radiation loss, and mode conversion loss. All these losses must be minimized to achieve overall low-loss performance. Material loss reduction is straightforward, which means the use of low-loss materials such as silicon [12], quartz [15], and plastic [13]. We have used high resistivity (HR) silicon as the channel material for low material loss and compatibility with mainstream silicon processes [16]. To implement the inter-/intra-chip interconnect for planar processes, a bending structure is the most intuitive and convenient approach. However, the bending structure may introduce additional losses due to radiation and mode conversion. The two losses are determined not only by the material, but also by the channel dimensions, and therefore present design trade-offs when optimizing the two loss mechanisms.

To support small form factor and package footprint, small bending structure is preferred. When the bending radius is smaller than the signal wavelength, radiation loss may exist because the portion of electromagnetic (EM) waves leaking into the air cannot preserve the phase front after bending. To minimize the radiation loss, the wave must satisfy two requirements:

- Total internal reflection (TIR) to reduce the radiation loss
- Transverse resonance condition to ensure constructive interference with itself [17]

Figure 5a illustrates the analysis of EM wave propagating in a planar slab dielectric waveguide, where n_1 and n_2 are the refractive indices, and k_1 and k_2 are the wave numbers of the dielectric waveguide material and the surrounding material, respectively. The waveguide has finite size along the x axis within the $\pm d$ region and is infinite along the y axis. The electromagnetic wave propagates along the z axis. When the incident angle θ is larger than the critical angle $\theta_c = \sin^{-1}(n_2/n_1)$ to satisfy the TIR requirement, the boundary condition determines the electrical fields on the three regions: upper, down, and inside the slab, can be represented as [17]

$$\begin{aligned} E &= E_o exp(a_x(x+d))cos(\beta z - \omega t) \quad x < -d \\ E &= E_o exp(-a_x(x-d))cos(\beta z - \omega t) \quad x > d \qquad (1) \\ E &= E_o cos(\beta z - \omega t) \quad -d \le x \le d \end{aligned}$$

where $a_x = (k_1^2 \sin^2\theta - k_2^2)^{0.5}$. Therefore, the waves outside the central waveguide area ($-d < x < d$) are evanescent waves with attenuation factor a_x. Besides the TIR requirement with the incident angle larger than the critical angle θ_C, transverse resonance needs to form constructive interference for low loss propagation. To achieve that, the phase difference needs to be an integer number of 2π after two reflections, expressed as

$$\begin{aligned} &2k_1 d cos\theta - 2\phi_r = 2\pi m \\ &tan(\phi_r/2) = (n_1^2 sin\theta^2 - n_2^2)^{0.5} / (n_1 cos\theta) \\ &\text{Therefore}: tan\left(\frac{dk_1 cos\theta}{2} - \frac{\pi}{2} m\right) \\ &\qquad = (n_1^2 sin\theta^2 - n_2^2)^{0.5} / (n_1 cos\theta) \end{aligned} \qquad (2)$$

where m is the mode number starting from 0 for the fundamental mode, ϕ_r is the phase difference generated for each reflection, determined by the incident angle and dielectric constants of the two interfacing materials. Equation 2 determines the possible propagation modes supportable by the slab dielectric waveguide. FigThe graphic at the top of Fig. 5b illustrates the EM distribution along a bending dielectric waveguide channel,

The severe interference caused by channel crosstalk constrains simultaneous multiple channel communications, and it is hard to adopt in dense interconnect channel scenarios. Therefore, a wired communication channel with low loss is desired for interconnect, especially TI.

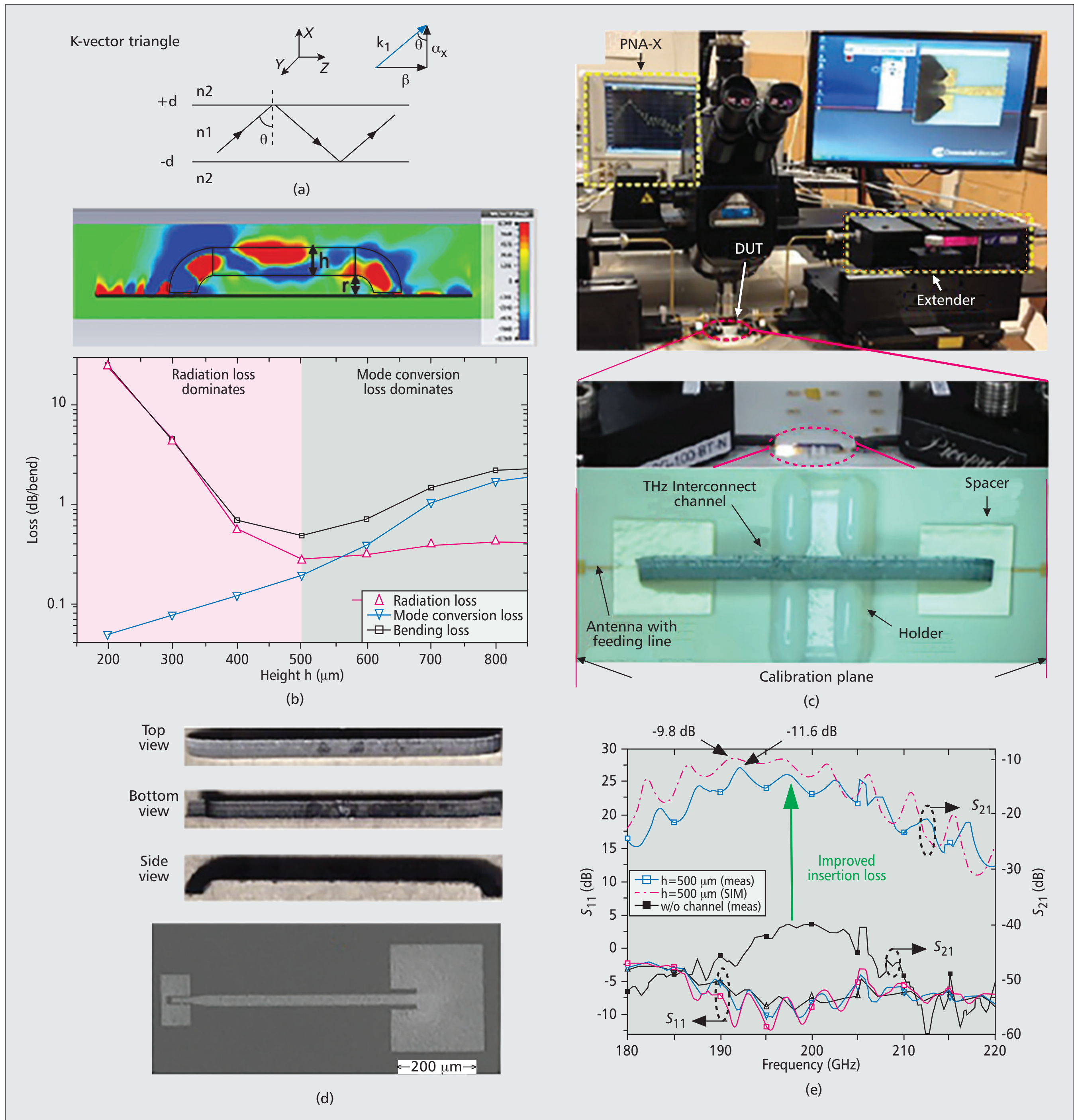


Figure 5. a) Analysis with total internal reflection and electrical field distribution in different media regions of a slab dielectric waveguide; b) simulated electrical fields and propagation waves along the channel and the simulated loss vs. different channel height; c) photograph of the test bench and a zoomed-in picture of the channel sitting in the spacer; d) photographs of the channel from different perspectives and the SEM photograph of the patch antenna based channel coupler; e) the measured and simulated S-parameters of the design silicon dielectric waveguide channel.

which indicates two major loss mechanisms: radiation loss and mode conversion loss. Increasing the channel dimension helps to confine the electrical field inside the waveguide channel to reduce the radiation loss. However, when the channel dimension becomes large enough to allow multiple modes to exist at the operating frequency, mode conversion loss will be induced. The issue is exacerbated by the bending structure. Figure 5b presents the bending loss, consisting of both radiation loss and mode conversion loss, vs. channel height h with a fixed radius r of 300 μ and a fixed width w of 300 μm at 200 GHz of a designed silicon dielectric waveguide [16]. When h is less than 500 μm, radiation loss dominates. Smaller height leads to a larger portion of the waves leaking into the air and causes larger radiation loss as shown by the curve with up triangles. When h is larger than 500 μm, higher order modes may be excited and propa-

gate, causing increasing mode conversion loss as shown by the curve with down triangles. The total loss is plotted as the curve with squares. The minimum loss of 0.3 dB occurs with h around 500 μm. To realize the signal coupling between the transceiver and the channel, this prototype adopts patch-antenna-based coupler structure to utilize its broadside radiation pattern.

Figure 5c illustrates the measurement setup and zoomed-in figure of the silicon dielectric channel [16]. Figure 5d presents the pictures of the fabricated channel and coupler. Figure 5e shows the comparison of measurement results between the cases with and without TI, which indicates dramatically improved insertion loss. The simulation results are also included for comparison, which confirms the consistency. The minimum insertion loss for h of 500 μm is about 11.6 dB. This loss can be significantly reduced due to the usage of low conductivity titanium on the feeding line and coupler to increase the fabrication stiffness, which is not needed in real interconnect scenarios. Without low-conductivity titanium, the insertion loss improves about 5 dB. Although the channel is only measured around 200 GHz due to equipment limitations, the design methodology and structure are ready to apply into the terahertz frequency range due to the benefits at higher operating frequencies. First, higher operating frequency increases signal bandwidth to support higher throughput; second, higher operating frequency reduces the device and channel size to further increase bandwidth density; third, higher frequency introduces better coupler efficiency for patch structure due to the small gaps between the top plane and the bottom ground plane in CMOS processes.

Circuit and System Non-Ideality Effects

TI performance is affected by practical circuit and system parameters and non-idealities, such as channel dispersion, circuit nonlinearity, noise, and system bandwidth. Large bandwidth facilitates high data rates. However, increasing bandwidth has realistic concerns; even the carrier frequency, channel bandwidth, and circuit bandwidth have sufficient capabilities. This is mainly because wide bandwidth results in a large integrated noise and is vulnerable to channel dispersion and circuit nonlinearity, thus degrading system SNR. When the bandwidth exceeds 100 GHz, it is extremely challenging to support the required SNR for ultra-low BER (e.g., 1×10^{-15}). Therefore, to support wide bandwidth, logically shared multi-channels through the same physical link, with relatively small bandwidth for each channel, should be adopted. The schemes to support multiple channels can be achieved through frequency-division multiplexing or other multiplexing approaches. When there are multiple channels, the interference due to channel crosstalk also degrades SNR. In addition, for all inter-/intra-chip communications, multiple parallel physical links are required to satisfy the overall extremely large aggregate data rate, such as petabyte or exabyte.

The scenario of multiple physical links and multiple logical channels sharing physical links is illustrated in Fig. 6. Due to the physically and logically adjacent channels, there is interference through channel coupling and crosstalk. A simplified scenario of channel coupling and crosstalk is illustrated in Fig. 6a. Assume a target channel, N, is coupled by eight adjacent channels. Two physically collocated channels, $N - 1$ and $N + 1$, generate interference. On the two adjacent physical links, there are also three corresponding channels close to the target channel with interference generation. Two factors — filtering, the suppression between adjacent logical channels, and crosstalk, the coupling between adjacent physical links — are critical to TI performance with multiple channel links. The coupling between adjacent channels and the target channel is illustrated in Fig. 6a. Figure 6b presents the normalized energy efficiency vs. physical link crosstalk given the filtering suppression is fixed at 40 dB. The target SNR is 18 dB to achieve a BER of 1×10^{-15}. The energy efficiency gets worse with a larger crosstalk. This is due to the fact that more crosstalk results in more interference, which therefore requires a larger signal power to maintain the same SNR, thus degrading the energy efficiency. Figure 6c illustrates the EVM and BER vs. physical link crosstalk given the same assumption of 40 dB filtering suppression. Assume initial EVM without crosstalk and channel coupling of –46 dB. The crosstalk degrades both the EVM and BER. When the crosstalk is worse than –20 dB, EVM degrades to –16.9 dB, which can no longer satisfy the BER requirement of 1×10^{-15}.

This analysis is a simplified scenario. In practical systems, there are more effects to consider, such as out-of-band intermodulation and adjacent channel spectrum regrowth. Therefore, the overall SNR and BER with practical circuit and system specifications can be presented as

$$\frac{S}{N} = \frac{P_S}{N_n \times BW + P_{nl_self} + P_{CC}};$$
$$BER = \frac{1}{2} erfc\left(\sqrt{\frac{SNR}{2}}\right) \quad (3)$$

where N_n is the noise spectrum density of a channel, P_{nl_self} is the interference from the target channel itself, such as dispersion and circuit nonlinearity, and P_{cc} is the interference from the adjacent channels, including channel crosstalk, out-of-band intermodulation, and spectrum regrowth due to nonlinearity. Good SNR and BER demand high suppression of all the non-idealities.

The development of THz Interconnect requires advancements from a large variety of research fields, including low-power and high-frequency active circuits and systems; low-loss, small-size, and low-dispersion channels; low-loss coupling between actives and passives; small crosstalk multiplexing techniques; and novel ideas in active and passive co-design to further boost energy efficiency.

Conclusions

This article proposes and presents a new application for the terahertz spectrum, THz Interconnect, to potentially address inter-/intra-chip interconnect issues by leveraging the advantages from both the electronics and optics sides. TI complements electrical interconnect and optical interconnect to focus on the communication dis-

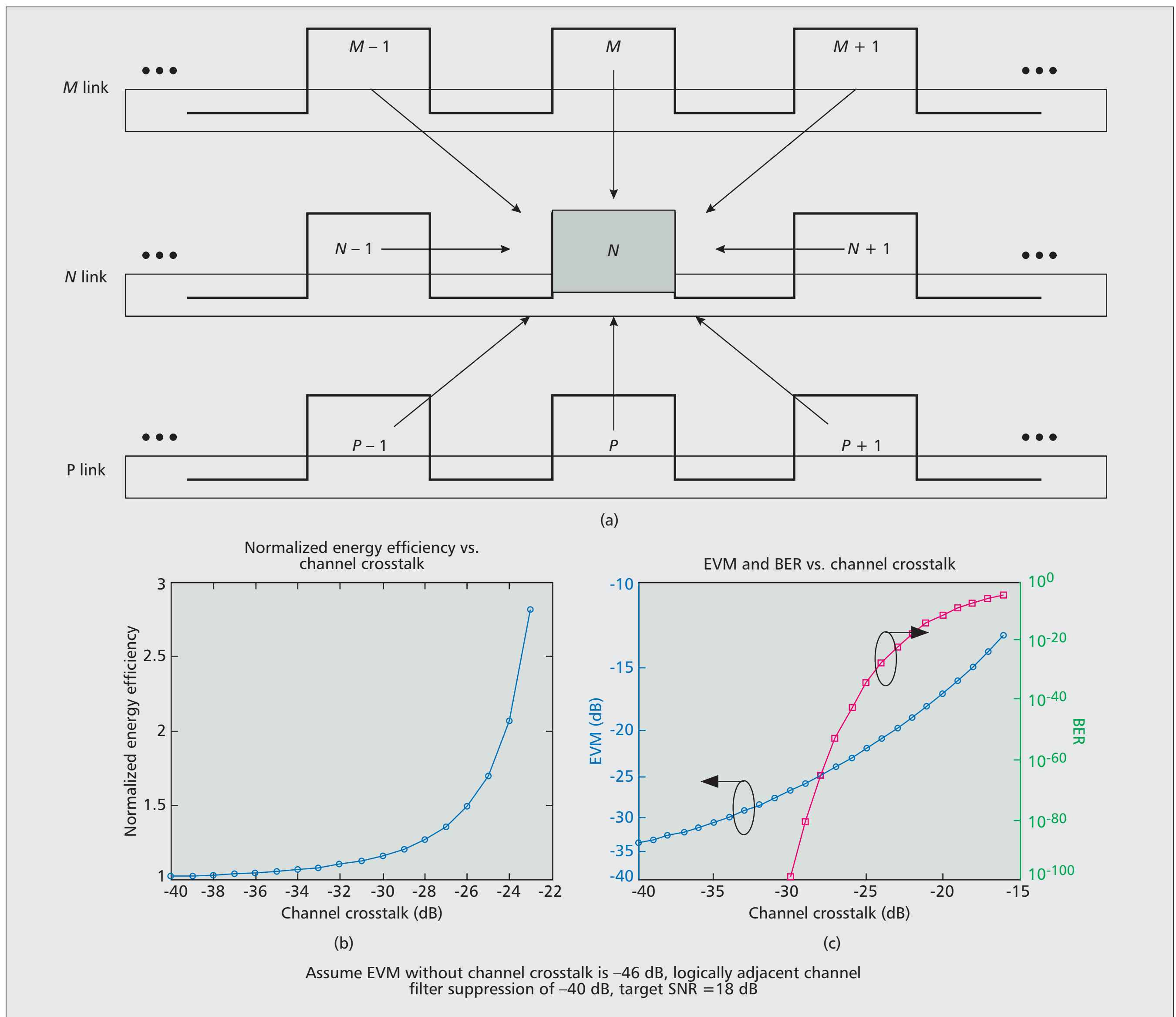


Figure 6. a) The scenario to analyze crosstalk effect among physically and logically adjacent channels; b) normalized energy efficiency; c) EVM and BER vs. channel crosstalk.

tance between 1 mm and 10 cm, which is the "last centimeter" region for inter-/intra-chip communications. The development of TI requires advancements in a large variety of research fields, including low-power and high-frequency active circuits and systems; low-loss, small-size, and low-dispersion channel; low-loss coupling between actives and passives; small crosstalk multiplexing techniques; and novel ideas in active and passive co-design to further boost energy efficiency. With the developments of the corresponding fields, we are optimistic to witness the long-standing interconnect gap to be closed.

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