# A Wideband and Low Power Dual-Band ASK Transceiver for Intra/Inter-Chip Communication

Shunli Ma[1], Junyan Ren[1*], Ning Li[1], Fan Ye[1]and Qun Jane Gu[2]

[1]State Key Lab of ASIC and System, Fudan University, Shanghai 200433, China; [2]Electrical and Computer Engineering Department, University of California Davis, Davis, CA 95616, USA

**Abstract- An energy-efficient dual-band ASK transceiver for intra/inter-chip communication is proposed in this paper. The transmitter is implemented with two coupled VCOs which have two modes and generate two carrier frequencies (75GHz/85GHz) with low power consumption. Meanwhile, the receiver consists of a wideband LNA, an envelope detector and output buffer. The LNA has a peak gain of 27dB at 86GHz, a bandwidth of 28GHz from 65GHz to 93GHz and a power consumption of 7mW. Intra-chip communication channels are implemented by on-chip transmission lines. Prototype ASK transceiver is fabricated in TSMC 65nm CMOS process with an area of 0.42mm$^2$. A spectrum and transient measurements show the bandwidth achieves up to 8GHz with a power consumption of 13mW.**

**Index Terms- RF-interconnect, dual-mode VCOs, wideband low noise amplifier (LNA), ASK transceiver, intra/inter-chip communication.**

## I. Introduction

The short-range communications have been increasingly important because they can satisfy the aggregated bandwidth requirements of multi-processors, memories, and networks-on-chip (NoCs) [1]-[2]. Various short-range communication methods have been proposed [3]-[5], and the short-range communication by RF-interconnection has already been demonstrated its advantages in bandwidth, latency, scalability, re-configurability and power efficiency [6]-[8]. For example, through-silicon-via (TSV) or through-silicon-interposer (TSI) [9]-[10] which are used as RF-interconnections for inter-chip communication has much high energy efficiency.

ASK transceivers can be used in RF-interconnected short-range communication system due to its simple modulation, demodulation and low power consumption because the complex mixed-signal modules such as ADCs, DACs and power-hungry digital block are eliminated [3]-[4]. On-chip transmission line (TL) used as RF-interconnect channels can achieve data rate of 5Gb/s with high power efficiency [7]. In order to further improve the data rate, a two-band receiver is proposed in [8], but it consumes large power and areas because two narrowband LNAs are needed and two ASK modulators are required in transmitter. Thus, this paper proposes an energy-efficient ASK transceiver solution. The transmitter has two capacitor-coupled VCOs providing two carriers to modulate the data. The receiver has a wideband LNA to cover the two bands. As a result, the proposed transceiver is power efficiency and can double the data rate with almost the same power of one band ASK transceiver compared to previous designs [8].

The transceiver is analyzed in time-domain and frequency-domain. The input data is modulated with by the carriers generated by the proposed dual-band VCO in transmitter. The modulated signal is sent to the receiver through on-chip RF-I channels. At the receiver side, the RF signal is amplified by the LNA and output to the following envelope detector for data recovery as shown in Fig.1(a). The data can be modulated to high band and low band in proposed design. As a result, the bandwidth is doubled as shown in Fig.1(b). Based on the different applications, RF-I channels can be implemented by TSV or TSI for inter-chip communication and on-chip TL for intra-chip communication as shown in Fig.1 (c).

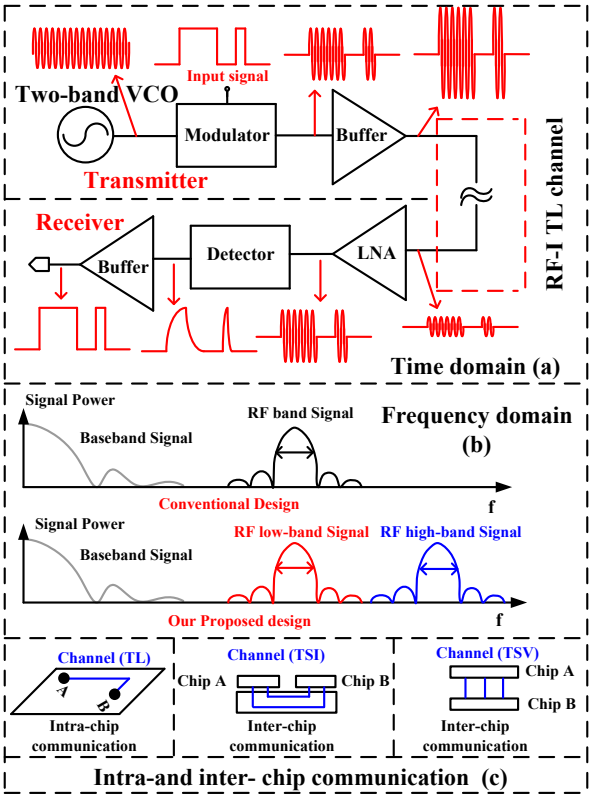



Fig.1 (a) ASK modulation in time-domain analysis. (b) ASK modulation in frequency domain for the proposed transceiver. (c) Channels for short range intra-and-inter chip communication

In this paper, on chip TL is used as RF-I and the transceiver was fabricated in TSMC 65nm CMOS process. Measurements show that the transceiver can achieve communication bandwidth up to 8 GHz with a higher energy efficiency compared to the previous designs [6]-[8].The paper is organized as follows. Section II presents the transmitter design and the receiver design including coupled VCOs, the high gain wideband LNA, RF-I channels, envelope detector and output buffer. The measurements results are given in Section III and the design is concluded in Section IV.

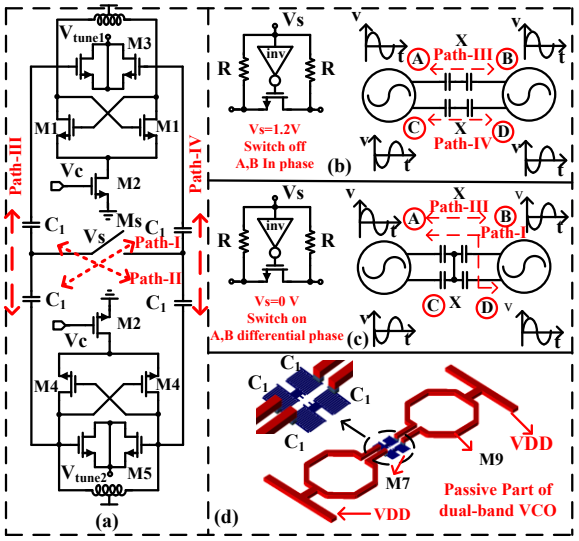



Fig.2 Circuit diagram of coupled VCOs and its passive device part

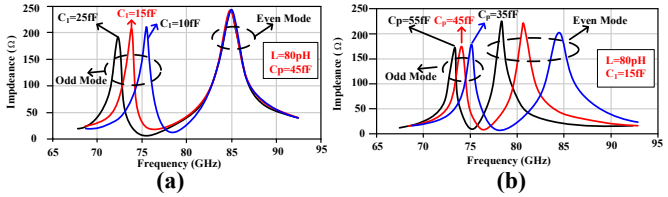



Fig.3 (a) Resonant frequency and impedance of LC tanks in the two modes with different values of the coupled capacitor $C_1$. (b) Resonant frequency changing with different values of the $C_P$

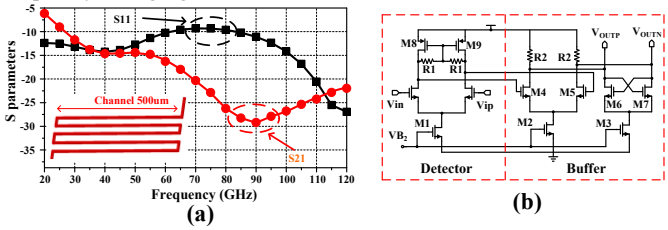



Fig.4 (a) the S-parameter of the on-chip TL and (c) circuit of the envelope detector and the output buffer

## II. The Proposed Transmitter

The proposed transmitter consists of coupled VCOs which are modulated by input data as shown in Fig.2 (a). The coupled VCO is implemented by two VCOs coupled with capacitor $C_1$ and a band-selected switch Ms. The gate of $M_2$ is modulated by input data.

### *A. The Proposed Dual-Band VCO Design*

Two modes of the proposed VCO are selected by the switch Ms which consists of two resistors and one inverter as shown in Fig.2(b)-(c). A small varactor in each VCO is used to compensate the free running frequency differences between the two VCOs, which are caused by asymmetry layout and process variation. The passive part was simulated in ADS as shown in Fig2(d).

The even mode and odd mode exist in the coupled VCO [11]-[12]. In the even mode, the two VCOs resonate in phase as shown in Fig.2(b). The coupling capacitors $C_1$ have no voltage drop and do not carry current. As a result, the $C_1$ only synchronizes the two VCOs in phase and have no effect on the resonant frequency as shown in Fig.3(a). The even mode resonant frequency $\omega_h$ can be expressed as

$$\omega_h = \frac{1}{\sqrt{LC_p}} \quad (1)$$

where $C_p$ is the capacitor of the LC tank.

In the odd mode, the output of the two VCOs is out of phase as shown in Fig2(c). Then the coupling capacitor $C_1$ has voltage drop and current flow. As a result, the resonator frequency $\omega_l$ will depend on the value of capacitors $C_1$ shown in Fig.3(b) which can be expressed as

$$\omega_l = \frac{1}{\sqrt{L(C_p+C_1)}} \quad (2)$$

The two modes are switched by controlling the coupling strength between the two VCOs, which is realized by the switch Ms. Strong coupling and larger impedance will stimulate the VCO resonating at higher frequency (even mode), while the weak coupling and smaller impedance leads lower resonant frequency (odd mode).

When the switch is off, Path-I and path-II are cut off which causes strong coupling due to output of the two VCOs injecting into each tank directly by path-III and path-IV as shown in Fig.2(b). Moreover, and even mode has higher impedance as shown in Fig3(a)-(b). As a result, the VCO resonates at high frequency in even mode. When the switch is on, the coupling is weaker because most parts of injection strength by path-I and path-III is cancelled due to the differential output characteristic of the VCO such as outputs at point (B,D) and point (A,C) as shown in Fig.2(c). Meanwhile, the impedance is lower as shown in Fig.3 (a)-(b). As a result, the VCO resonates at low frequency in odd mode.

### *B. The Proposed Receiver design and Channel Simulation*

The RF-I channel is implemented by metal-9 in 65nm CMOS process with length of 2.5mm and width of 10um. The loss of the channel is around 25dB at the two modes as shown in Fig.4(a). This on-chip TL channel can be replaced with TSI and TSV for inter-chip communication.

The proposed receiver consists of the high gain LNA, detector, and output buffer. The envelope detector and buffer are shown in Fig.4(b). The In order to achieve high gain, the LNA has three stages and adjacent stages are coupled by transformer which is shown in Fig.5(a).

This structure can achieve wideband and high gain within compact area. Moreover, the bias circuits are easily implemented. Meanwhile, the adjacent stages eliminate the bulk and loss capacitor used for blocking DC due to transformer coupled methods [13]. In this design, the target is high gain and wideband, not high power compared to conventional PA design because the LNA drives the small

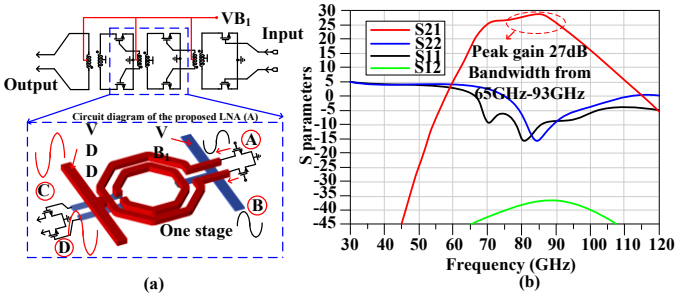
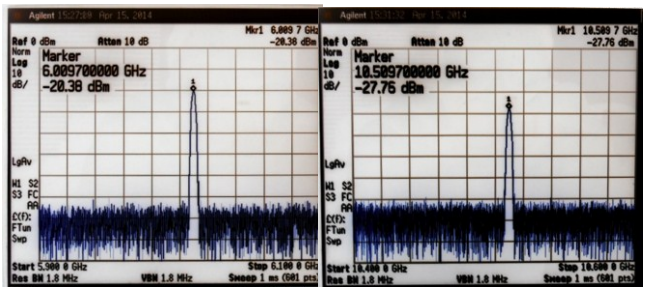



Fig.5 (a) Circuit diagram of the LNA and its passive part of one stage(b) S-parameter of the LNA.




(a) (b)

Fig.6The spectrum output of receiver when input modulation signals are 6GHz (a) and 10GHz (b)

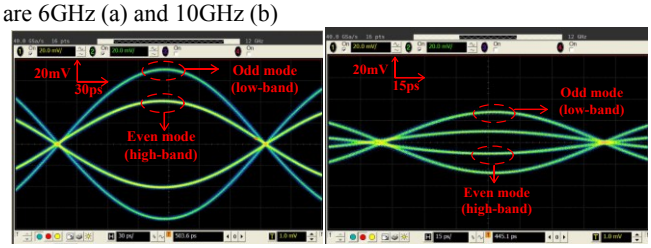



Fig.7 The transient output of receiver at two modes when modulation signals are 2.5GHz and 5GHz

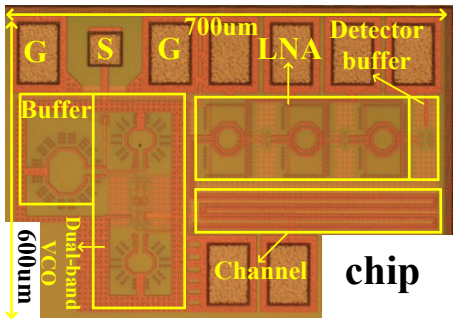



Fig.8 die-photo of the proposed transceiver;

load from the detector. As a result, the output power can be traded to high gain and wideband during design. What is more, by appropriate sizes of the transistors (20u/65nm) and the bias voltage, the low power consumption within 7mW was achieved.

The passive part of one stage is shown in Fig5.(a). The loss of the transformer is around 0.8dB at interested frequency, and the gain of each stage is around 9 dB. The post-layout simulations by ADS shows the LNA can achieve 27dB gain and 28GHz bandwidth from 65GHz-93GHz as shown in Fig.5(b). The outputs of the LNA are connected to envelope detector which recover the baseband data from ASK signal because its low frequency part is amplified due to higher gain, while high-frequency carrier is filtered.

## III. Measurement Results

The prototype ASK transceiver is fabricated in 65nm TSMC CMOS 1P9M RF process. Firstly, the bandwidth of the transceiver is measured. The input modulation signal frequency at transmitter side is swept from low frequency to 10GHz with constant -3dBm power. The output of the receiver is connected to E4440A spectrum analyzer and its spectrum is shown in Fig.6 (a)-(b). The output power of 6GHz is -20 dBm and 10.5GHz is -27dBm. The bandwidth of the transceiver is about 8GHz at 1V supply voltage.

TABLE I: COMPARISON TABLE

| | ISSCC 2011[1] | JSSC 2010[2] | VLSI 2012[3] | CICC 2012[7] | **This work** |
|---|---|---|---|---|---|
| Technology | 65nm CMOS | 40nm CMOS | 40nm CMOS | 65nm CMOS | 65nm CMOS |
| *fc*(GHz) | 23.3 | Baseband | 135 | 60 | **75/85** |
| Modulation | ASK | ASK | ASK | ASK | **ASK** |
| Bandwidth*(GHz) | 4.2 | 2.15 | 5 | 2.5 | **8** |
| Power(mW) | 21 | 11 | 98 | 14.4 | **12/13** |
| Channel | wireline | wireline | Wireless | wireline | **wireline** |
| Channel loss | 12dB | 10dB | NA | 27dB | **25dB** |
| FoM (GHz/mW) | 5 | 5.11 | 19.6 | 5.76 | **1.5/1.625** |

*the bandwidth is calculated by the data rate in these references

Secondly, the transient outputs of receiver at two modes are measured by Agilent 40GS/s oscilloscope with 13GHz bandwidth. The modulation signals frequencies are 2.5GHz and 5GHz. The measurements results show that amplitudes of the two modes have small differences due the larger channel loss at high-band.

The die photo is in an area of 0.42mm$^2$ as shown in Fig.8, Table I shows the comparison table of recently publish papers. The proposed dual-band transceiver can achieve wide bandwidth and low power consumption.

## IV. Conclusion

This paper proposed high energy efficiency ASK dual-band transceiver consisting of dual-band transmitter and wideband receiver with RF-interconnect. The dual-band transmitter is realized by coupled VCOs whose modes can be selected by a switch. The wideband and high gain LNA is used in the receiver. Meanwhile, the channel is implemented by on-chip TL with 20-25 dB loss which can be replaced by TSV or TSI for inter-chip communication. The testing chip was fabricated in TSMC 65nm CMOS 1P9M process within an area of 0.42mm$^2$ and measurements show bandwidth is up to 8GHz with power consumption of 12mW for low band and 13mW for high band.

## References


[1] G.S. Byunet al., "A 8.4 Gb/s 2.5 pJ/b mobile memory I/O interface using simultaneous bidirectional dual (Base+RF) band signaling," *IEEE ISSCC Dig. Tech. Papers*, pp. 488–489, Feb. 2011

[2] B. Leibowitz et al., "A 4.3 GB/s mobile memory interface with power efficient bandwidth scaling,"*IEEE JSSC*, vol. 45, no.4, pp. 889–898, Apr. 2010.

[3] N. Ono et al., "135 GHz 98 mW 10 Gbps ASK Transmitter and eceiver Chipset in 40 nm CMOS,"*IEEE VLSI*, pp50-51, Jun.2012

[4] A. Oncu et al., "19.2mW 2Gbps CMOS Pulse Receiver for 60GHz and Wireless Communication," *IEEE VLSI*, pp158-159, Jun.2008

[5] M. F. Chang et al, "Power reduction of CMP communication networks via RF Interconnect," *IEEE/ACM Sym. Micro.*, pp.376-387, Nov. 2008.

[6] S.-W. Tam et al "A simultaneous tri-band on-chip RF-Interconnect for future Network-on-Chip", *VLSI Sym.*, pp. 90-91, Jun. 2009.

[7] H.Wu et al., "A 60GHz On-Chip RF-Interconnect with λ/4 Coupler for 5Gbps Bi-Directional Communication and MultiDrop Arbitration," *IEEE CICC*, pp. 1-4, Sep. 2012.

[8] R. Fujimoto et al., "A 120 GHz / 140 GHz dual-channel ASK receiver using standard 65 nm CMOS technology" *IEEE EuMC*,pp 1189 - 1192 Oct. 2011

[9] P.D. Sai Manoj et al. "Reliable 3D Clock-tree Synthesis Considering Nonlinear Capacitive TSV Model with Electrical-thermal-mechanical Coupling", *IEEE TCAD*, vol.32, no.11, pp1734-1747, Nov. 2013

[10] J.C. Wang et al., “High-Speed and Low-Power 2.5D I/O Circuits for Memory-logic-integration by Through-Silicon Interposer,” *IEEE 3DIC*, pp.1-4 Oct. 2013.

[11] G. S.Li et al , “A Distributed Dual-Band LC Oscillator Based on Mode Switching,” *IEEE TMTT*, vol. 59, no.1, pp. 99–107, Jan. 2011.

[12] Z. Deng, “A 4-port inductor-based VCO coupling method for phase noise reduction,” *IEEE JSSC*, vol. 46, no.8, pp. 1772–1781, Aug. 2011.

[13] W. L.Chan et al, "A 60GHz-band I V 11.5dBm Power Amplifier with 11% PAE in 65nm CMOS," *IEEE ISSCC Dig. Tech. Papers* ,pp. 380-381, Feb. 2009.