A Ultra-Wideband CMOS PA with Dummy Filling for Reliability

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***Abstract* — This paper presents a V-band power amplifier in a bulk 65 nm CMOS technology with the peak gain 14.5 dB and 3-dB bandwidth of 28.8 GHz (50.8 GHz to 79.6 GHz). The PA has demonstrated 15.1 dBm P_{sat} and 18.9 % peak PAE. The PA features three stage transformer coupled differential architecture with integrated input and output baluns. The entire PA core occupies 0.31 mm^2 chip area and dissipates about 150 mW.**

***Index Terms* — CMOS, power amplifier, transformer, V-band.**

I. Introduction

The unlicensed multi-gigahertz bandwidth around 60 GHz is a good candidate for high data rate wireless communication systems. CMOS technology is attractive for the advantages of low power consumption, low cost, and intimate integration with baseband circuitries. A CMOS-based 60 GHz power amplifier is still a challenging block mainly due to two design aspects: low output power/power added efficiency (PAE) and narrow bandwidth. Power combining techniques are typically used to achieve higher output power, albeit at the cost of reduced efficiency. Further improvement continues to challenge the designers. Recently, a number of 60 GHz PAs were reported [1-12]. However, trade-offs are still challenging between key specifications, such as gain, power efficiency, and bandwidth.

This paper presents a broadband, high efficiency power amplifier for the 60 GHz low-power applications. The PA exhibits a small signal gain greater than 13.5 dB from 53.5 GHz to 71 GHz and 3-dB bandwidth of 28.8 GHz, 50.8 GHz to 79.6 GHz. With 1.25 V power supply, the PA achieves peak PAE of 18.9 % at 65 GHz.

II. Wideband PA Design

CMOS technologies' fast advancements over the past decades support increasing speed circuits, making mm-wave CMOS circuits widely adopted today. Although intrinsic CMOS device speed keeps increasing, the inherent drawbacks impede high performance mm-wave circuits, particularly for the challenging PAs. First, the shrinking power supply voltages challenge high power delivery from each channel. Second, lossy substrates and high contact resistance degrade the quality factor of passive components and drop power efficiency. Third, a larger portion of parasitic capacitance versus inner capacitance erodes achievable operating frequency and further wastes power through the additional charging/discharging current to the parasitics. In addition, the main drive for CMOS technologies for integration with analog and digital sub-systems for SOC, on the other hand imposes large coupling and interferences among circuit blocks. In addition, deep-scaled technologies have very tight DRC requirements, including local and global density requirements to ensure the reliability. This requirement therefore imposes a significant challenge to high frequency design with the need of passive components, such as inductors, capacitors, and transformers. To overcome these challenges in deep-scaled CMOS technologies, we adopted a transformer based differential PA architecture with metal dummy filling to achieve high output power and PAE while maintaining high reliability.

A. Transformer based PA Architecture

Fig.1 shows the simplified schematic of a transformer-coupled three-stage differential PA with integrated input

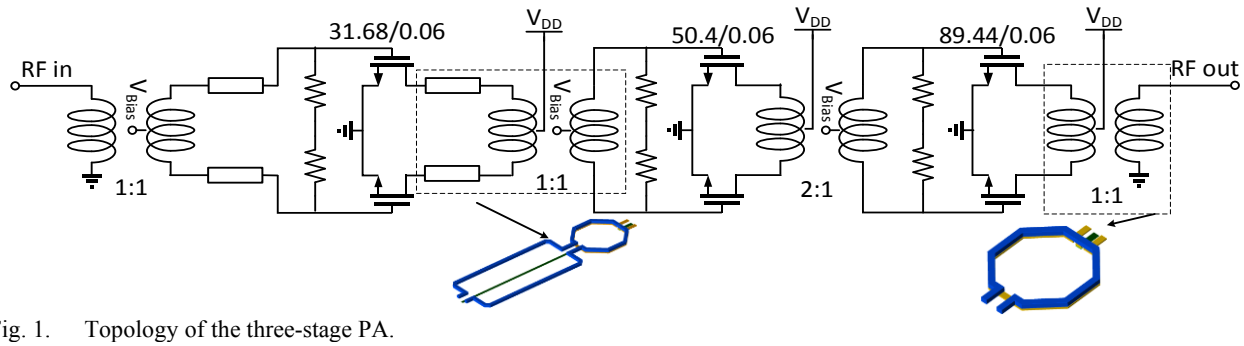


Fig. 1. Topology of the three-stage PA.

and output baluns. Each stage is a differential NMOS common-source amplifier to achieve larger headroom and higher linearity.

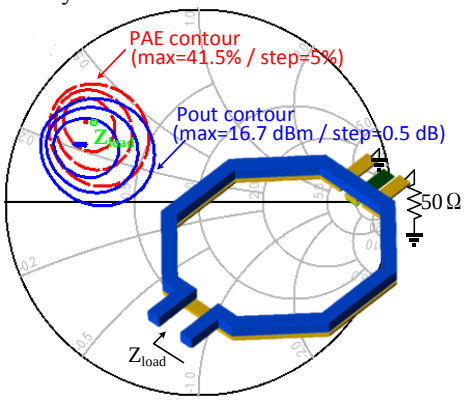


Fig. 2. Output load-pull power contours and PAE contours at 65 GHz for differential pair transistors and output balun impedance.

Transformer based inter-stage matching and tuning is adopted due to its advantages of compactness, differential configuration, individual stage biasing, good isolation between input and output for better stability. The input and output transformers server as baluns to convert between single-ended I/O signals and differential on-chip signals. To maximize magnetic coupling coefficient and quality factor, the primary and secondary windings are stacked directly above each other and realized using the top two thick layers, which are 3.4 µm and 0.9 µm, respectively. The simulated coupling coefficient is 0.7. The vertical stacking structure will also block the signal coupling from the top layer to the substrate to reduce the dielectric coupling loss, resulting in a quality factor of about 13. The diameter of the output balun is optimized to efficiently transform the 50 Ω output load impedance to the chosen value Z_{opt} for the last stage transistors as shown in Fig.2. Due to the large mismatch between the output conductance of stage 1 and the input conductance of stage 2, an additional matching network is required. Therefore, transmission lines are inserted between stage 1 drain load and transformer as shown in Fig.3. A similar conductance mismatch at the input of the PA is also solved by adding transmission line to the transformer.

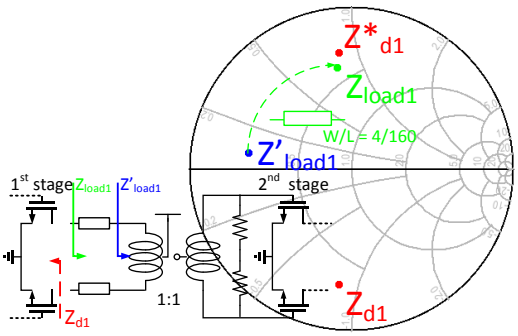


Fig. 3. The inter-stage matching network using 1:1 transformer with a pair of differential microstrip transmission lines.

B. *Broad Band Amplifier*

Fig.4 presents the simulated gain curves for each stage. A wide bandwidth of the PA is achieved by 3-stage amplifier offset tuning frequency scheme. Since transistors' size increase from the first to last stage, their G_{max} and f_{max} decline toward the output side. Therefore, the resonant frequency of the first stage is designed to be higher than that of the second stage, which is further higher than the third stage resonant frequency so that the overall gain response can be maintained over a wide bandwidth. This method facilitates a flat gain response as shown in Fig.4 and maintain high output power over the entire frequency range.

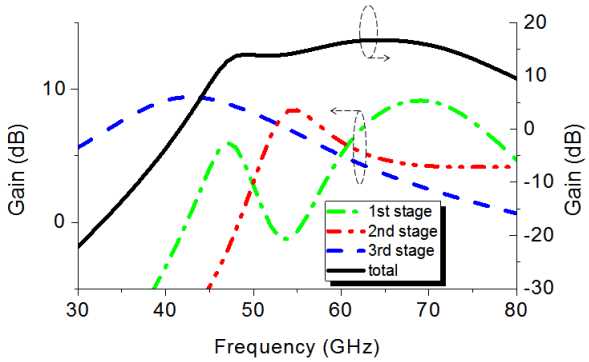


Fig. 4. Simulated power gain for each stage and the overall PA gain versus frequency.

The transformer based matching network also helps to further boost operating bandwidth. Fig.5 shows the comparison of traditional transmission line and transformer based matching network from 50 to 80 GHz. The traditional transmission line matching can achieves perfect conjugate matching at a single frequency, but the matching become worse as frequency deviates from the center frequency. In contrast, the transformer achieves wide bandwidth matching to assist wideband amplification.

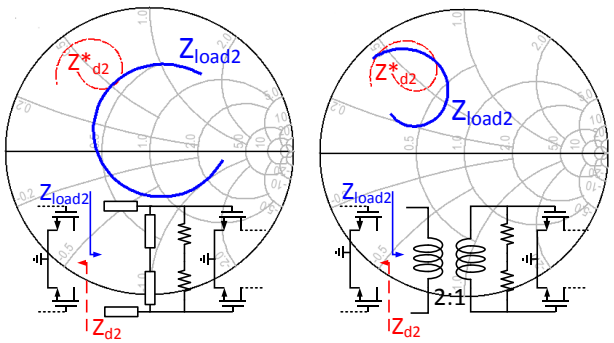


Fig. 5. Comparison of inter-stage matching using transmission line and transformer from 50 GHz to 80 GHz.

C. *Dummy Filling for Reliability*

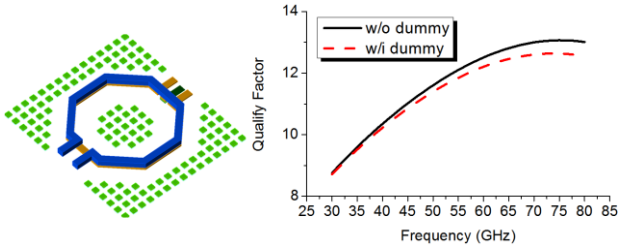
Deep-scaled processes require metal density not only in the global chip area, but also in local chip areas. Conventionally, to avoid the EM coupling effects, high frequency passive components are often exempted from

TABLE I PERFORMANCE COMPARISONS WITH SOAS IN 65 NM BULK CMOS

Ref.	*B.W.* [GHz]	*OP1dB* [dBm]	*Psat* [dBm]	Peak Gain [dB]	Peak PAE [%]	Supply Voltage [V]	P_{dc} [mW]	Size [mm^2]
[1]	43-65	9	12.3	7.7	8.8	1	N/A	0.251
[2]	56.5-65	5	11.5	16	15.2	1	50	0.696
[3]	55-67	N/A	9.6	18.2	13.6	1.2	62.4	0.319
[4]	54-63 *	10	14.6	23.2	16.3	1.2	135	0.6
[5]	57-66	9.3	12.9	16.7	23.4	1.2	61.2	0.11**
[6]	49-58	8.5	12.3	17.1	20.4	1	N/A	0.036**
[7]	55.5 - 62.5	13.7	14.85	9.4	16.2	1	N/A	0.357
[8]	N/A	N/A	9.6	29	17.3	1.2	N/A	0.1**
[9]	54-66	15.5	16.6	17.7	14.5	1.2	378	0.32**
This work	50.8-79.6	12.9	15.1	14.5	18.9	1.25	150	0.31

* estimated from the presented figures, **the size without the pads.

the metal density requirements. However, this layout style may degrade chip reliability in the long term. Therefore, metal dummy filling is required to satisfy all the density requirements, both locally and globally. Fig. 6(a) shows a transformer with dummy filling. To avoid eddy current, the dummy fillings need to be isolated small metal pieces. The most important region is the area surrounding the transformer metal trace due to the strongest EM field. Therefore, the dummy metal should be placed as far as possible from the transformer metal conductor. Fig. 6(b) compares the EM simulated results of the transformers with and without metal dummies. The quality factor drops by 2.7% due to the dummies.



(a) (b)

Fig. 6. (a) Topology of transformer with dummy filling and (b) simulated EM results with the comparison of the transformer without dummy filling.

III. MEASUREMENT RESULTS

Fig.7 shows the chip photograph of the fabricated V-band PA. The chip was implemented on TSMC 65 nm CMOS process with dimensions of 0.43×0.73 mm^2 including all the testing pads. An Agilent N5247A PNA-X vector network analyzer with Agilent N5260-60004 waveguide T/R module (frequency extenders) are used for small signal measurements. The large signal measurement results are obtained by driving the PA with a mm-wave signal generator and measuring the output power by a mm-wave power meter. The losses of probes, adaptors, and cables were all calibrated.

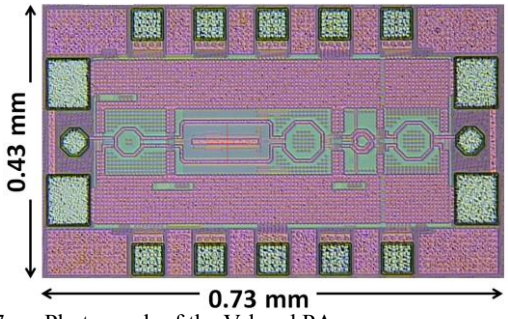


Fig. 7. Photograph of the V-band PA.

Fig. 8 shows the measured S-parameters from 30 GHz to 80 GHz at 1.25 V drain bias. The PA exhibits a peak gain of 14.5 dB at 60 GHz with 1-dB bandwidth of 17.5 GHz from 53.5 to 71 GHz and 3-dB bandwidth of 28.8 GHz from 50.8 to 79.6 GHz. The input return losses are better than 5 dB from 45 GHz to 80 GHz.

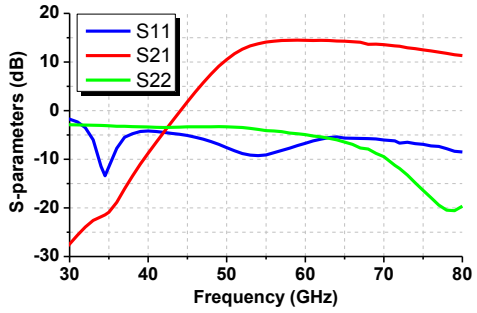


Fig. 8. The measured S-parameters results.

Fig. 9 shows the measured output power, power gain, and PAE versus input power at 65 GHz. The PA achieves a saturated output power (P_{sat}) of 15.1 dBm at 65 GHz with a power supply of 1.25 V. The output 1dB compression point (OP_{1dB}) is 12.9 dBm and the peak PAE is 18.9 %.

Fig.10 shows the broadband characteristics of this PA. Measured OP_{1dB} and P_{sat} with their PAE at 1.25 V bias from 55 GHz to 69 GHz are plotted in Fig.10. Within the

frequency range from 57 GHz to 69 GHz, the OP_{1dB} variation is 1.2 dB with PAE from 10% to 12.8%. The measured P_{sat} variation is 1 dB and the peak PAE is greater than 14% over 57 to 69 GHz. Both high output power performance and high efficiency are obtained from 57 GHz to 69 GHz, suggesting that the PA achieves an ultra-wide operation frequency range.

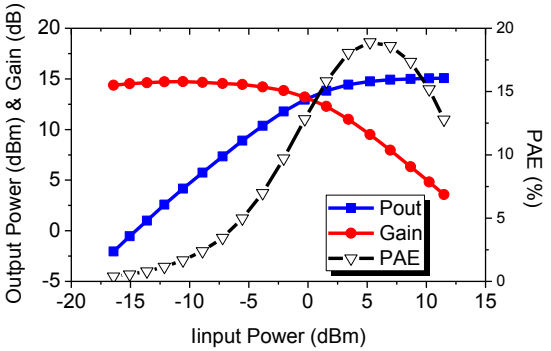


Fig. 9. Measured output power, power gain and PAE versus input power at 65GHz.

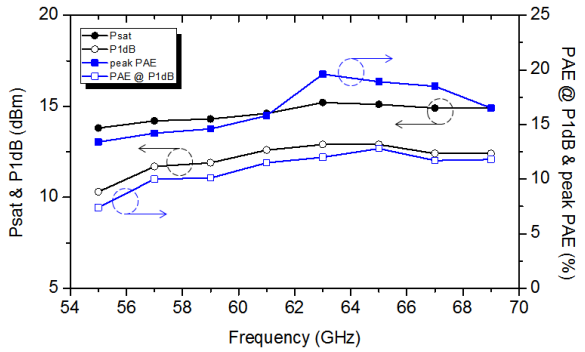


Fig. 10. Measured P_{out}, peak PAE, and PAE at P_{1dB} as a function of frequency.

Table I summarizes the recently reported V-band PAs units in 65 nm bulk CMOS processes [1-9]. This design achieves widest 3-dB bandwidth.

IV. Conclusion

This paper presents a broadband high efficiency power amplifier for 60 GHz low-power applications. The PA exhibits a small signal gain of 14.5 dB and a saturated output power of 15.1 dBm, which demonstrates a to-date the widest 3-dB bandwidth of 28.8 GHz in 60 GHz band without capacitor tuning. With 1.25 V power supply, the PA achieves peak PAE of 18.9 % at 65 GHz.

Acknowledgement

The authors wish to acknowledge the assistance and support of the IWS Organizing Committee. This work was partially supported by the U.S. Department of Energy Grant DE-FG02-99ER54531.

References

[1] D. Chowdhury, P. Reynaert, A. Niknejad, "A 60GHz 1V +12.3dBm Transformer-Coupled Wideband PA in 90nm CMOS", ISSCC Dig. Tech. Papers, pp. 560-635, Feb.2008

[2] W. Chan and J. Long, "A 58 GHz–65 Hz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," IEEE J. Solid-State Circuits, vol. 45, no. 3, pp. 554–564, 2010

[3] T. Wang, T, Mitomo, N. Ono, and O. Watanabe, "A 55-67GHz Power Amplifier with 13.6% PAE in 65 nm standard CMOS " IEEE RFIC Symp., pp. 1-4, June 2011.

[4] H. Asada, K. Matsushita, K. Bunsen, K. Okada, A. Matsuzawa, "A 60GHz CMOS power amplifier using capacitive cross-coupling neutralization with 16 % PAE", EuMIC, Manchester, pp. 1115- 1118, Oct. 2011

[5] W.-H. Lin, T.-W. Huang, H. Wang, and J. Wang, "A 57-66 GHz 12.9-dBm Miniature Power Amplifier with 23.4% PAE in 65-nm CMOS," EuMIC, Amsterdam, pp. 12-15, Oct. 2012

[6] X. Bi, Y. Guo, J. Brinkhoff, L. Jia, L. Wang, Y. Xiong, M. S. Leong, and F. Lin, "A 60-GHz 1-V supply band-tunable power amplifier in65-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no.11, pp. 719–723, Nov. 2011.

[7] J. Y.-C. Liu, R. Berenguer, and M. F. Chang, "Millimeter-wave self-healing power amplifier with adaptive amplitude and phase linearization in 65-nm CMOS," IEEE Trans. Microw. Theory Tech., vol. 60, no. 5, pp. 1342–1352, May 2012

[8] J. Lin, C.C Boon, X. Yi, W. M. Lim, "A Compact Single Stage V-Band CMOS Injection-Locked Power Amplifier With 17.3% Efficiency," IEEE Microwave and Wireless Components Letters, col. 24, no. 3, pp.182-184, 2014

[9] P. M. Farahabadi, and K. Moez, "A dual-mode highly efficient 60 GHz power amplifier in 65 nm CMOS," IEEE RFIC Symp., pp. 155 – 158, Jun. 2014

[10] T. LaRocca and M. C. F. Chang, "60GHz CMOS differential and transformer-coupled power amplifier for compact design," IEEE RFIC Symp. pp. 65-68, 2008

[11] N. Kurita and H. Kondoh, "60 GHz and 80 GHz wide band power amplifier MMICs in 90 nm CMOS technology RFIC Symp. Dig., Jun. 2009, pp. 39–42.

[12] M. Abbasi, T. Kjellberg, A. de Graauw, E. van der Heijden, R. Roovers, and H. Zirath, "A broadband differential cascode power amplifier in 45nm CMOS for high-speed 60 GHz system-on-chip," IEEE in RFIC Symp., pp. 533–536, May 2010