A 54-84 GHz CMOS SPST Switch with 35 dB Isolation

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***Abstract*—This paper presents a hybrid design based, CMOS millimeter-wave (mm-wave) single-polar single-throw (SPST) switch. The circuit design starts from the analysis and optimization of a distributed structure, while implemented using coupled lump elements for performance improvement and area-efficient layout. Moreover, a specific bias scheme is used to further decrease insertion loss by more than 0.5 dB. This SPST switch achieves higher than 35 dB isolation over an ultra-wide frequency range, from 54 GHz to 84 GHz, a minimum 1.7 dB insertion loss, and <-10 dB return loss with 0.012 mm^2 chip area in 65 nm CMOS. This design achieves more than 10 dB enhancement of isolation by comparing with state-of-the-arts while maintaining similar insertion loss.**

***Index Terms*—SPST switch, high isolation, millimeter-wave, 65 nm CMOS.**

I. Introduction

For mm-wave applications including passive imaging, short-range communication and sensing, switches [1]–[3] are essential components for transmitting-receiving functions, signal-routing and modulation. The important specifications include insertion loss, isolation, return loss as well as power handling ability.

Different from the traditional series-shunt switch architecture in RF frequency ranges, most of the published mm-wave switches remove the series switch to reduce insertion loss [1][2]. However, isolation performance degrades without series switches.

This work starts from a detailed analysis of switch insertion loss and isolation, optimization and their trade-offs, and then devises a simplified design for optimum performance that is verified by a hybrid mm-wave SPST design in 65 nm CMOS technology. The paper organizes as follows. First, the architecture of mm-wave SPST switches is analysed, followed by the design details of an E-band switch design. The measurement results are then presented with conclusions at the end.

II. Circuit Analysis and Design

A. Architecture Analysis

Dur to removing the series transistor in switches, the design of a shunt transistor based switch faces direct trade-offs between insertion loss and isolation. A shunt transistor can be modelled as a channel resistor R_{on} at on-state and a combination of resistor R_{off} and capacitor C_{off} at off-state. The on-state resistance R_{on} determines the isolation performance, a smaller R_{on} leads to a higher isolation by using a larger device size. On the other hand, a larger device size increases C_{off}, resulting in higher insertion loss and a narrower bandwidth.

A few approaches have been reported to improve switch performances. For example, a transmission-line (TL) stub can be added parallel with the shunt switch to compensate C_{off}, effectively broadening the operating bandwidth [1]. A π-type network based mm-wave SPST switch improves the isolation [4]. To further improve isolation, more stages may be added, as shown in Fig. 1, which leads to a distributed structure [2][5]. However, there is no prior art elaborating the optimum number of stages for both insertion loss and isolation.

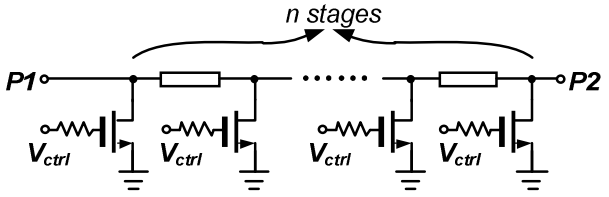

Fig. 1 Distributed SPST switch structure

With the help of ABCD-parameters, the S_{21} and S_{12} of the two-port network in Fig. 1 can be concluded as [5]

$$S_{21} = S_{12} = \frac{2}{2 + Z_o n Y} \tag{1}$$

where Z_o is the characteristic impedance of the system, n is the number of stages, while Y represents the Y-parameter of each shunt transistor. The isolation and insertion loss of the switch can be calculated as

$$\mathrm{ISO} = |S_{21-on}| = \frac{2}{2 + Z_o n Y_{on}} = \frac{2}{2 + \frac{Z_o n}{R_{on}}} \approx \frac{2R_{on}}{Z_o n} \tag{2}$$

$$\mathrm{IL} = |S_{21-off}| = \left|\frac{2}{2 + Z_o n Y_{off}}\right| = \frac{2}{\sqrt{\left(2 + \frac{Z_o n}{R_{off}}\right)^2 + Z_o^2 n^2 \omega^2 C_{off}^2}} \tag{3}$$

Eq. (2) shows high isolation need be achieved by either increasing n or enlarging the transistor size to reduce R_{on}. The approach to increase transistor size for better isolation is limited when the size becomes large. The reason is that the transistor includes not only an on-resistor R_{on}, but also

parasitic capacitance in on-state. The parasitic capacitance eventually degrades the isolation when the device is too big. Therefore increasing number n becomes more effective. As shown in Eq. (2), the isolation performance has a comparatively linear relationship with n. Therefore, it is preferred to design a multi-stage distributed architecture when targeting high isolation performance, while keep each stage transistor at a relatively small size, which results in a high R_{off} and small C_{off}. However, the caveat of this approach is the negligence of TLs losses. When too many stages are incorporated, insertion loss from TLs becomes an issue, which leads to an optimum n to balance insertion loss and isolation.

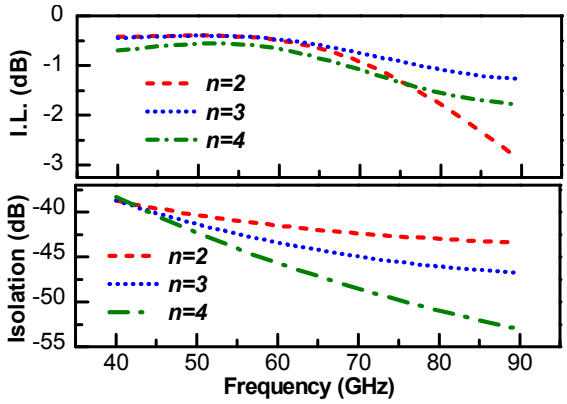

Fig. 2 simulated insertion loss (I.L.) and isolation of distributed SPST switch versus different stage number n

Fig. 2 compares the simulated insertion loss and isolation of three distributed SPST switches versus different stage number n. In this simulation, standard transistor model and microstrip TLs are used. The transistor size and TLs length are optimized for low insertion loss and high isolation. The pass-band is centred at around 60 GHz. As expected, the isolation is continuously increased with a larger number of stages. The degradation of insertion loss between 2-stage and 3-stage architecture is negligible. In addition, thanks to the distributed architecture, the 3-stage SPST switch offers a larger bandwidth than its 2-stage counterpart. However, when n increases to 4, insertion loss suffers from a remarkable degradation, although a higher isolation can be realized. Therefore, 3-stage SPST switch structure is adopted in this design.

B. Circuit design

The schematic of the designed SPST switch is shown in Fig. 3 (a). According to above analysis, the SPST switch employs three shunt transistors for the optimum 3-stage structure. Unlike the conventional distributed structure, the SPST switch is implemented using lump devices to save chip area as shown in Fig. 3 (b). A symmetrical inductor is employed to represent two TLs with the second stage transistor M_2 connected to its centre-tap. The other two shunt transistors M_1 and M_3 are connected to the two terminals of the inductor respectively. The invented hybrid design results in an area-efficient layout by replacing two individual TLs.

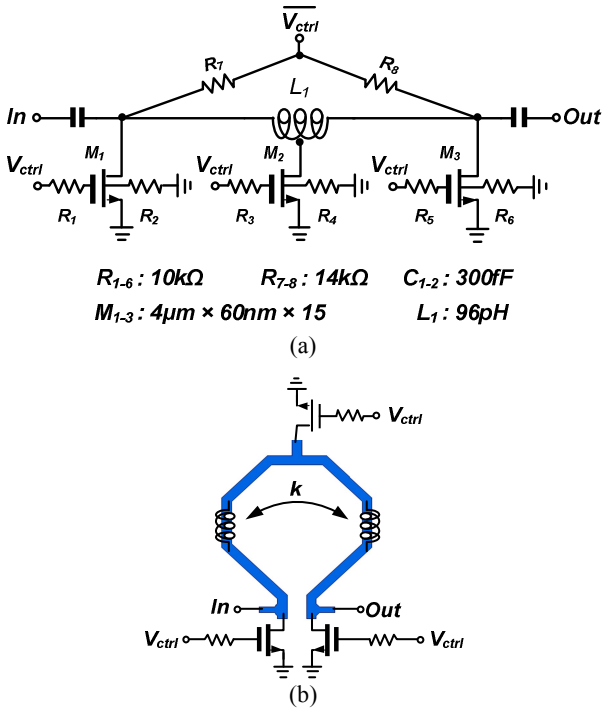

Fig. 3 (a) SPST switch schematic and (b) hybrid implementation of the SPST switch

Furthermore, the hybrid layout induce coupling between two half inductors, which is utilized to improve the performance. Its effect is investigated in simulation using ideal inductors with different inductance and coupling coefficient, to keep the centre frequency at 67 GHz. As shown in Fig. 4, insertion loss shows a strong dependence on the coupling coefficient k in the entire band, a larger k resulting in less insertion loss. This coupling has a negative influence on the isolation. A large k reduces isolation, but this effect is more prone to occur in the frequency range higher than the centre frequency. For the designed switch in E-band, an optimum k around 0.3 is chosen, which could reduce insertion loss and maintain the isolation around centre frequency. Above 0.5 dB improvement of insertion loss is accomplished due to this coupling. When it comes to a real inductor design, the inductor size is shrunk artificially due to the mutual inductance generated by this coupling. Accordingly, smaller inductor size results in higher quality-factor and less coupling to the substrate, especially in mm-wave band. These advantages eventually benefit both the insertion loss and isolation. The inductor is EM-simulated in ADS momentum to attain accurate model for circuit simulation.

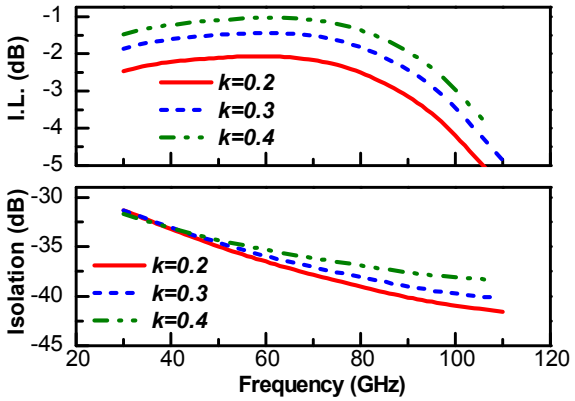

Fig. 4 Simulated insertion loss (I.L.) and isolation with different coupling coefficient *k*

Using this distributed architecture, the transistor size must be optimized for a balanced performance. With 60 µm/60 nm size, the switch transistor provides a R_{on}= 5.8 Ω, R_{off} = 1.5 kΩ and C_{off} = 28 fF. Although this size cannot offer a very small R_{on}, the switch is still able to realize a >30 dB isolation in simulation, due to the optimized distributed structure and hybrid layout. The transistor is designed in a triple-well as described in Fig. 5 (a). The transistor's gate, bulk and deep-Nwell (DNW) are all ac-floated by 10 kΩ large resistors to reduce signal leakage under large signal condition [6]. On the other hand, bulk and DNW are both biased to make sure the diodes shown in Fig. 5 (a) are reverse-biased. Consequently, the signal at the S/D sees extremely large impedance to the substrate, resulting in lower insertion loss.

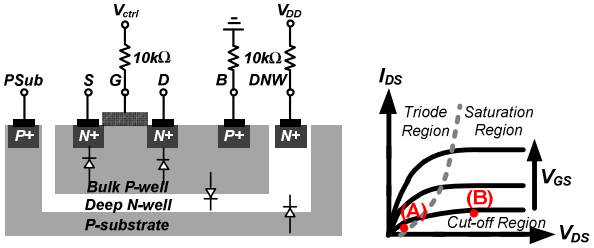

Fig. 5 (a) Cross-section view of NMOS transistor in triple-well process, (b) I/V characteristics of NMOS transistor

A special bias scheme is used to improve the insertion loss. Unlike other mm-wave switch design which leaves the D of transistors unbiased, D is biased to the reversed voltage of V_{ctrl} through a 14 kΩ large resistor. A larger resistor is used here than the body-floating, because the signal at D sees a smaller impedance to the bias voltage than to the substrate. From the transistor's I/V characteristics shown in Fig. 5 (b), the off-state resistance R_{off} increases from point A (D unbiased) to point B (D reverse biased from V_{ctrl}). The transistor operates in cut-off region. Fig. 6 shows the simulated insertion loss comparison between these two cases, which presents more than 0.5 dB improvement due to the new bias scheme.

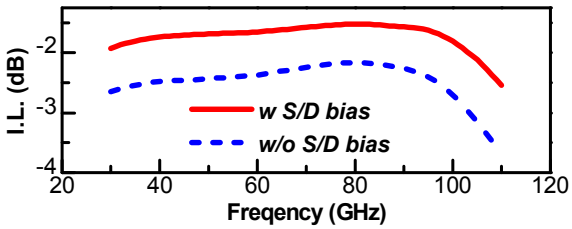

Fig. 6 Simulated insertion loss with proposed bias scheme

III. MEASUREMENT AND DISCUSSION

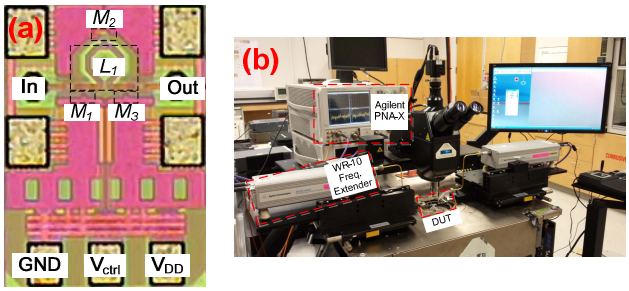

Fig. 7 (a) Die photo, (b) S-parameter measurement setup

The switch was fabricated in a standard bulk 65 nm CMOS technology with a 6-metal back-end. The switch core circuit occupies only 100×120 µm^2 area. The on-wafer S-parameter measurement is conducted with the setup shown in Fig. 7. The system is calibrated to probe tip using SLOT approach. Therefore, the pads loss is included in the measurement results.

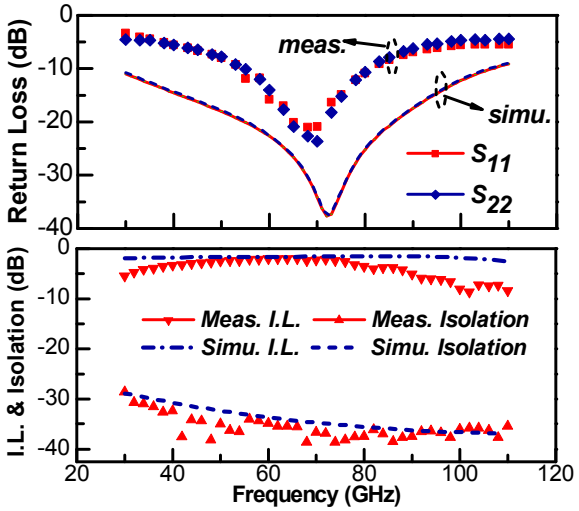

Fig. 8 Simulated and measured small-signal performance

The measured and simulated small-signal performances are compared in Fig. 8 with good agreement. In the pass-mode, the operating bandwidth is centered at 70GHz. The SPST switch achieves <-10 dB return loss from 54 GHz to

84 GHz. The minimum insertion loss is 1.7 dB at 65 GHz. It has less than 4 dB insertion losses between 35 GHz and 85 GHz, which can satisfy our application requirement.

When shunt switches are all in on-state, the SPST switch provides a very high isolation, >35 dB from 54 GHz to 84 GHz. The highest isolation is 39 dB, at around 75 GHz. The switch structure shows resilience to a low supply voltage. The isolation maintains well down to 0.9 V. Even with 0.6 V supply voltage, isolation can still be higher than 20 dB. The insertion loss is independent to supply voltage.

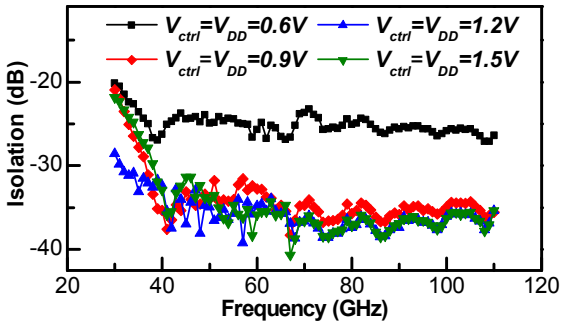

Fig. 9 Isolation performance with different supply voltage

The large signal measurement is plotted in Fig. 10 at 60 GHz. The loss of connection and probes has been calibrated. It shows a 10.5 dBm input-referred P1dB compression-point.

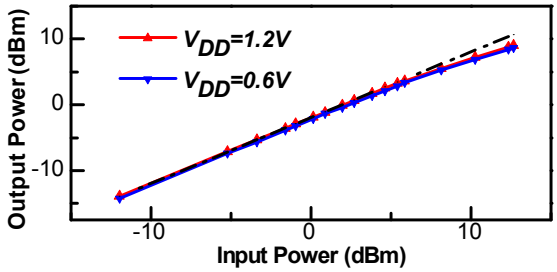

Fig. 10 Measured large-signal performance at 60 GHz

A performance comparison is presented in Table 1. The switch advances the state-of-the-art performance by achieving isolation >35 dB, bandwidth about 30 GHz, while maintaining good matching and low insertion loss. If a single-polar double-throw (SPDT) switch is implemented by incorporating this SPST switch, a higher isolation can be attained, since the impedance transformation network in SPDT switch will further increase isolation.

IV. Conclusion

A 54 GHz-84 GHz SPST switch is presented with optimized distributed structure while implementing with lumped components by leveraging coupling coefficient. It demonstrates 1.7 dB minimum insertion loss and <-10 dB return loss over an ultra-wide operating range from 54 GHz to 84 GHz. Furthermore, a larger than 35 dB isolation is achieved in the entire band. With the invented hybrid implementation composed of a distributed structure and coupled lump elements, more than 10 dB isolation improvement is realized with similar low insertion loss, by comparing with state-of-the-art reports.

Table 1
Performance comparison with SOAs in silicon

Ref.	[1]	[3]	[4]	[7]	[8]	This work
Type	SPDT	SPDT	SPDT	SPST	SPST	SPST
BW (GHz)	50-70	57-66	94-110	42-70	44-54	54-84
Min I.L. (dB)	1.5	2	4	1.25	1.9	1.7
R. L. (dB)	<-8	<-10	<-10	<-5	<-10	<-10
ISO. (dB)	>25	>21	>25	>18	18	>35
IP1dB (dBm)	13.5	13.8*	N/A	2	21*	10.5
Tech	90 nm CMOS	130 nm CMOS	65 nm CMOS	0.35μm SiGe	0.18μm SiGe	65 nm CMOS

*simulation results

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