A 10 GHz Delay Line Frequency Discriminator and PD/CP based CMOS Phase Noise Measurement Circuit with -138.6 dBc/Hz Sensitivity at 1 MHz Offset

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***Abstract*—This paper presents a delay line frequency discriminator (FD) and phase detector (PD)/charge pump (CP) based phase noise measurement (PNM) circuit to achieve wide bandwidth, great sensitivity and reliable integration at 10 GHz. PD/CP based phase noise detection makes it insensitive to environment and coupling noises. A delay-locked loop (DLL) is designed to align the PD input phases and a DC offset cancellation circuit is embedded to overcome circuit mismatches, which make the PNM self-calibrated. This PNM demonstrates -61/-81 dBc single tone sensitivity and -110.35/-138.60 dBc/Hz phase noise sensitivity at 100 kHz/1 MHz offset, respectively. The phase noise measurement bandwidth is 200 MHz, which is determined by the off-chip SAW filter bandwidth. This proof-of-concept design is fabricated in a 65 nm CMOS technology with the chip area of 1.5 mm × 1.3 mm. The core circuit consumes 15.2 mW power.**

***Index Terms*—Delay line (DL), phase detector (PD), charge pump (CP), frequency discriminator (FD), phase noise measurement (PNM).**

I. Introduction

Phase noise is the performance limitation to many microsystems, such as communications, imaging, sensing and radar. To suppress phase noise, feedback and feed forward noise cancellation have been investigated [1-2]. The capability of these phase noise cancellation systems is limited by the phase noise measurement (PNM) circuit noise floor, which determines the best achievable phase noise performance. Delay line with large delay time and low phase noise is the key component in PNM. Ref. [1] adopts high-Q FBAR filter as delay line to extract phase noise, which demonstrates superior noise sensitivity of -162 dBc/Hz at 1 MHz offset. But the operational bandwidth is limited by the high-Q filter, which is very small. Ref. [2] and [3] utilized an active delay line chain to extract the phase noise, which is constrained by the high noise contribution from the active delay line itself.

The existing PNM circuits are based on mixer type phase noise extraction scheme [1-3], which cannot differentiate phase noise from amplitude noise. Therefore, the PNM accuracy is vulnerable to environment noises, such as cross-talk and coupling noise. This drawback impedes the integration of the PNM into systems, where other circuits/sub-systems produce a variety of coupling spurs and noises.

To overcome the issues of existing PNMs and achieve wideband, reliable and integratable approaches, we present a new passive delay line frequency discriminator (FD) and PD/CP based PNM circuit. Although, this proof-of-concept has used off-chip SAW filter as the delay line, the research shows that SAW filter can be realized as silicon-in-package (SiP) [4], or even systems-on-chip (SoC) solutions to minimize the form factor [5].

II. Proposed Phase Noise Measurement System

The delay line frequency discriminator (FD), shown in Fig. 1, is the core of the PNM. It consists of delay line (DL) and phase detector (PD). DL transforms the absolute phase noise into relative timing jitter; PD detects the relative timing jitter and converts it to a voltage signal.

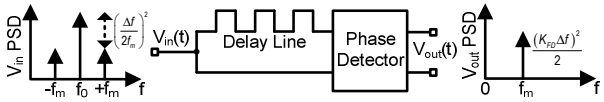

Fig. 1. Delay line frequency discriminator (FD)

The input signal with phase noise can be represented by a narrow-band FM signal without losing generality:

$$V_{in}(t) = V_{amp}\cos\left(2\pi f_c t + \frac{\Delta f}{f_m}\cos(2\pi f_m t)\right) \quad (1)$$

where V_{amp} is the input signal amplitude, f_c is the carrier signal frequency, f_m is the modulation frequency or the offset frequency of the target phase noise measurement, and $\Delta f / f_m$ is the index of the FM signal, which indicates the phase noise level.

The phase difference between the input signal and its delayed one represents the phase noise information which can be expressed as

$$\Delta\phi = \frac{\Delta f}{f_m}\left|\cos(2\pi f_m t) - \cos\left(2\pi f_m (t-\tau)\right)\right| \quad (2)$$

where τ is the delay time of the delay line.

By converting the phase noise modulated on the carrier frequency to the baseband, the baseband signal processor,

such as amplifier, can magnify the extracted phase noise as

$$V_{out}(t) \approx K_{FD} \cdot \Delta f \cdot \sin\left(2\pi f_m (t - \tau/2)\right) \quad (3)$$

where K_{FD} is the frequency discriminator gain in V/Hz. The output voltage is proportional to sideband amplitude Δf, which represents the phase noise level.

There are a few design concerns and challenges in PNM design:

1) One critical requirement is to tolerate coupling noise and differentiate phase noise from amplitude noise. To achieve this, PD/CP based phase noise extraction scheme is adopted.

2) With PD/CP based PNM, the phase of PD inputs should be in-phase. To achieve this, an embedded delay-locked loop (DLL) is designed to guarantee that the delay time is integer times of signal period, i.e. $\tau = nT$.

3) Due to the very small phase noise level, any circuit mismatch will desensitize the circuit. To overcome this issue, on-chip DC offset cancellation circuit is leveraged.

To address these concerns, the new PNM is designed, illustrated in Fig. 2. The PNM mainly consists of divider, on-chip passive voltage controlled delay line (VCDL), off-chip SAW filter, PD, CP and analog baseband (ABB), which includes a variable gain amplifier (VGA) and a low pass filter (LPF).

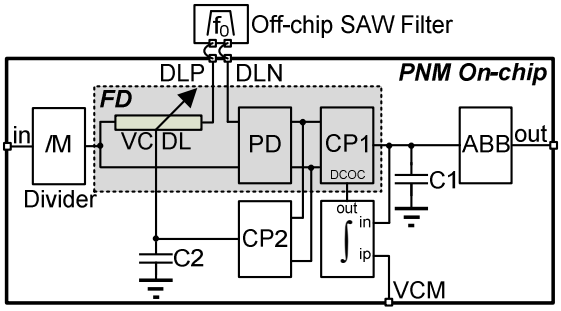

Fig. 2. Block diagram of the delay line and PD/CP based PNM

One of the key performances of PNM is the phase noise sensitivity, which is determined by the circuit noise floor, and can be calculated as:

$$PN_{sensitivity} = 20\log_{10}\left(\frac{V_{n,out}(f_m)}{TF(f_m)}\right) \quad (4)$$

where $V_{n,out}(f_m)$ is the output noise and $TF(f_m)$ is the transfer function of PNM, which can be represented as

$$TF = (2\pi\tau \cdot K_{PDCP} \cdot G/M) \cdot f_m \quad (5)$$

where K_{PDCP} is PD/CP gain, G is VGA gain and M is divider ratio. The part in bracket is the K_{FD} of this design.

Eqs. (4) and (5) show that large delay time delay line with small phase noise is preferable for better phase noise sensitivity. In addition, large K_{PDCP} also improves phase noise sensitivity.

III. Mixer Based FD vs. PD/CP Based FD

There are two types of phase noise extraction methods: mixer based and PD/CP based methods. We chose PD/CP based phase noise extraction scheme due to two key advantages: in-phase relationship requirement and insensitivity to amplitude noise.

A. Requirement of Phase Relationship for PD Inputs

The mixer based FD requires the two input signals to be quadrature phase relationship, which has large harmonics. [3] adopts a calibration loop to ensure the quadrature. The loop includes a comparator, a state machine and a programmable LDO. But the implementation is sensitive to environment and coupling noises due to their different transient states.

In contrast, the PD/CP based FD requires the input signal to be in-phase, which leverages the same transient state of the two inputs and suppresses the coupling noise by converting them into common mode noises. As to the phase alignment, DLL based approach ensures the in-phase relationship, as shown in Fig. 2, which is a more effective implementation scheme.

B. Amplitude Noise Sensitivity

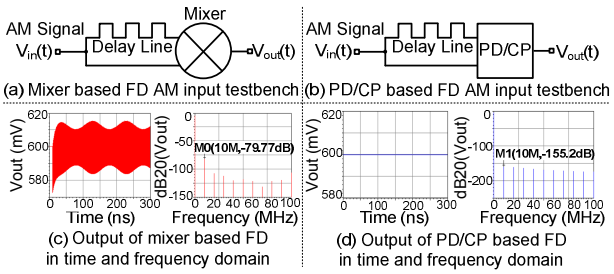

Fig. 3. Comparison of mixer based FD and PD/CP based FD with AM input signal

The mixer based phase extraction scheme is responsive to both amplitude and phase information of the input signals, therefore it is sensitive to environment variations. However, PD mainly extracts the phase information of the inputs. Therefore, it is more reliable in integrated circuits and systems.

To verify this understanding, two test benches are set up as shown in Fig. 3(a) and (b) for mixer based and PD/CP based FD. Input is 1.25 GHz AM signal with 10 MHz modulation frequency, and index is 0.1. Fig. 3(c) shows the time and frequency domain output of mixer based FD, which does respond to the AM input signal. In contrast, Fig. 3(d) shows the output of PD/CP based FD in both time and frequency domain. The amplitude of 10 MHz output signal is 75.43 dB smaller than mixer based FD output, which indicates no response to AM input signal. Therefore, PD/CP based FD is insensitive to amplitude noise.

IV. Circuit Implementation

A. Delay-Locked Loop

The DLL, consisting of VCDL, SAW filter, PD, CP2 and C2, is shown in Fig. 4(a). To ensure the in-phase relationship, DLL controls the varactor of the on-chip VCDL to adjust the input phase relationship. DLL is a one-pole system to ensure the stability [6].

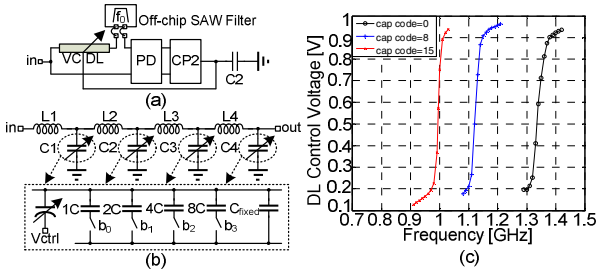

Fig. 4. (a) Block diagram of DLL, (b) schematic of VCDL, and (c) simulated DLL frequency locking range versus delay line control voltage at three switching cap codes: 0, 8 and 15

The on-chip VCDL consists of 4 cascaded stages LC type transmission line (TL) as shown in Fig. 4(b). The tunable capacitor includes one fixed capacitor, a 4-bit switchable cap array for discrete delay adjustment and a varactor for continuous delay adjustment. The phase noise of the combination of VCDL and SAW filter is superior due to their passive natures, which are -182/-185 dBc/Hz at 100 kHz/1 MHz offset, respectively. The SAW filter has 24 MHz bandwidth at 1.25 GHz center frequency. The in-band group delay is about 20 ns.

Fig. 4(c) shows the simulated DLL (without SAW filter) frequency locking range versus delay line control voltage at three different switching cap codes: 0, 8 and 15. The frequency locking range is continuously covered over the range of 0.95-1.4 GHz, which corresponds to 0.71-1.05 ns delay time.

B. DC Offset Cancellation Circuit for PD&CP

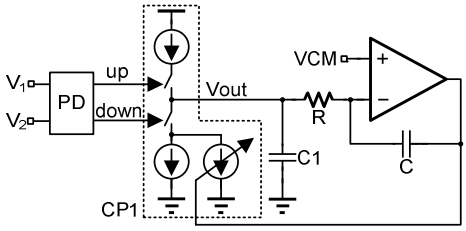

Fig. 5. Schematic of DC offset cancellation circuit

To remove the DC offset due to mismatches of PD/CP, the DC offset cancellation circuit is proposed as shown in Fig. 5. The output voltage of CP1 is extracted by the integrator and compares with the VCM. The output of the integrator changes the discharging current until the CP1 output common node voltage equals to VCM to cancel the DC offset introduced by mismatches. This DC offset cancellation circuit can compensate DC offset caused by CP charging and discharging current mismatch, PD input phase mismatch, up and down pulse rising and falling time difference.

The resistor and capacitor of the integrator must be large to prevent the desired signal from affecting the discharging current, which are: R=12.4 MOhm and C=54 pF. They form 237.7 Hz corner frequency.

V. Experimental Results

The proposed 10 GHz PNM circuit is fabricated in a 65 nm CMOS technology and occupies 1.5 mm × 1.3 mm area including PADs. Fig. 6(a) shows the die photo. The fabricated chip was mounted to a double-sided FR4 PCB for test. The core circuit consumes 15.2 mW power.

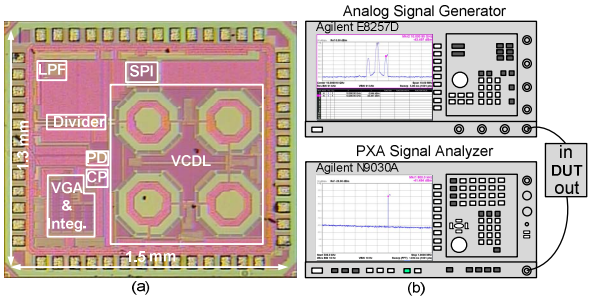

Fig. 6. (a) PNM die photo and (b) test setup for the PNM circuit

Fig. 6(b) shows the test setup for the PNM circuit. Single-tone (ST) FM signal is used to evaluate the linearity and sensitivity of the PNM [3]. Agilent E8257D analog signal generator is used to generate a 10 GHz FM signal as the PNM input. The output is monitored by Agilent N9030A signal analyzer with very low displayed average noise level (DANL) to improve test accuracy.

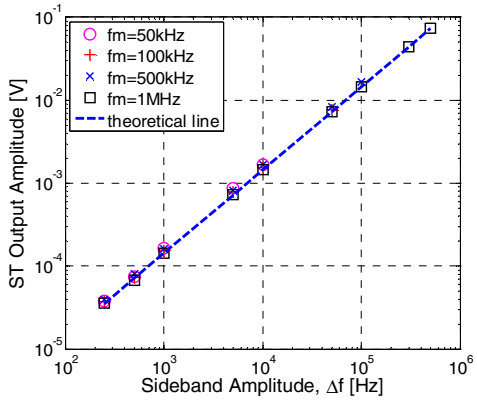

Fig. 7. ST linearity measurement results

Fig. 7 shows the ST output amplitude versus sideband amplitude with different modulation frequency, which

verifies the good linearity predicted by Eq. (3) with less than 1 dB error.

The ST sensitivity is measured using FM signal. When the sideband amplitude of the FM signal reduces, the output eventually deviates away from the linear response due to the circuit's own noise contribution. The 1 dB deviation point corresponds to the phase noise measurement ST sensitivity. Fig. 8 shows the ST sensitivity versus offset frequency. Measurement result shows that system's ST sensitivity is -61/-81 dBc at 100 kHz/1 MHz offset, respectively. The equivalent phase noise sensitivity is calculated from the ST results by averaging a window of three adjacent offset frequencies over the corresponding bandwidth [3]. The equivalent phase noise sensitivity is plotted in Fig. 8. At 100 kHz/1 MHz offset frequency, the equivalent phase noise sensitivity is -110.35/-138.60 dBc/Hz, which is better than the requirements of most applications.

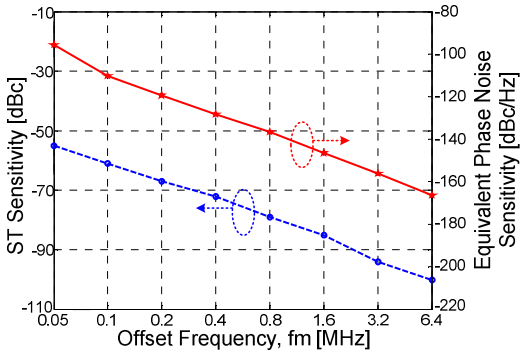

Fig. 8. Measured ST sensitivity (left) and equivalent phase noise sensitivity (right) versus offset frequency

This PNM can support wide working bandwidth. For this demonstration, it is limited by the SAW filter's 24 MHz bandwidth. Therefore, the input frequency range is 8 times of it due to the divide-by-8 circuit in the front. The actual measured frequency range is 9.896-10.096 GHz.

Tab. I summarizes the performances and shows the comparison with state-of-arts (SOAs). This design is insensitive to amplitude and environment noise to facilitate integration. The phase noise sensitivity can be improved by more than 10 dB when the CP current is increased from 0.64 mA to a few mA. The working bandwidth can also be boosted by using wideband SAW filter or an array of filters.

VI. Conclusions

This paper presents a new 10 GHz phase noise measurement circuit enabled by passive delay line frequency discriminator and PD/CP phase extractor. It has the advantages of wide bandwidth, great sensitivity, and immunity to amplitude and coupling noises, thus is suitable to be integrated. This circuit achieves -61/-81 dBc ST sensitivity at 100 kHz/1 MHz offset, which is equivalent to phase noise sensitivity of -110.35/-138.60 dBc/Hz. The phase noise sensitivity can be further improved by more than 10 dB when CP current is increased. This PNM provides a high potential solution for ultra-sensitive high-reliability on-chip phase noise measurement.

TABLE I
Performance Summary and Comparison with SOAs

	This Design	Ref. [1]	Ref. [3]
Carrier Frequency	10 GHz	1.5GHz	1 GHz
Bandwidth	200 MHz	narrow	2 GHz
Phase Detector Type	PD/CP	Mixer	Mixer
Sensitive to Amp. Noise	NO	YES	YES
On-chip self-calibration	YES	NO	YES
PN @ 100kHz (dBc/Hz)	-110.35 (equivalent to -130.35 for 1GHz)*	-142	-124
PN @ 1MHz (dBc/Hz)	-138.60 (equivalent to -158.60 for 1GHz)*	-162	-152
Power Consumption	15.2 mW**	26 mW	N/A
CMOS Process	65 nm	130 nm	250 nm

* PN sensitivity is converted to 1 GHz by using 20 dB/dec trend for comparison.

** There is additional 82.5 mW buffer power consumption to drive the off-chip 50 Ohm SAW filter, which is not needed when the filter is integrated.

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