Tunable N-Path RF Front-end Filter with an Adaptive Integrated Notch for FDD/Co-Existence

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***Abstract*— In this paper an RF front-end filter with an adaptive integrated notch is presented. The proposed filter consists of a N-path bandpass filter and a notch filter. The outputs of the bandpass filter and the notch filter are subtracted to create the integrated notch. The third and fifth harmonics are also suppressed due to the subtraction. The filter can handle strong transmitter frequency in the receive band by creating a notch at that particular frequency. The notch frequency can also be adjusted in a certain frequency range and as a result, the proposed filter can block strong out-of-band blockers close to the transmitting frequency. The passband of the filter is tunable from 0.6 GHz to 1.8 GHz. The gain of the filter is 20.3 dB. The NF is 3 dB, which only degrades to 3.68 dB in presence of a 0-dBm blocker at 50 MHz offset. The channel bandwidth is 8.7 MHz and the out-of-band IIP3 ($\Delta f = 50$ MHz) is 18.97 dBm.**

I. Introduction

The demand of highly integrated multiband receivers to cover different frequency bands has driven the development of blocker-tolerant software defined radios. Replacement of multiple dedicated narrowband radios by one widely tunable radio will reduce the cost and size of the transceiver due to the removal of multiple off-chip bulky SAW (surface acoustic wave) filters. Wideband receivers passes both the desired signal as well as the undesired blockers or out-of-band interference. The elimination of RF filtering is challenging due to gain compression and reciprocal mixing. A conventional narrowband design utilize an off-chip, high-Q SAW filter to suppress any out-of-band blockers. On the other hand, a wideband design has no selectivity and the low noise amplifier (LNA) amplifies both the wanted signal as well as blockers. High gain is expected from the LNA to achieve a low NF. A 0-dBm blocker will cause the LNA to clip due to low supply voltage used in modern CMOS process. As a result both the noise and distortion will increase in the receiver. An on-chip bandpass filter (BPF) will minimize the effect. However, it is hard to design an on chip bandpass filter with high-Q.

In a frequency division duplexing (FDD) system, the transmitter and receiver operate at different carrier frequencies and the transmitting frequency is the most dominant blocker for the receiver. Several architectures have been proposed with an integrated notch for multi standard applications. In [1], a bandpass filter with integrated notch is independently presented. However, the power consumption (74 mW$\sim$146 mW) is extremely high and complicated baseband processing is required to create the notch. The notch is moved by changing the LO frequency. In [2], the notch filter block is moved in front of the LNA. The in-band attenuation is high for large blocker power and also the blocker attenuation is only 20 dB at 40 MHz offset which is not adequate. The receiver is only designed for a specific frequency and the notch frequency is not tunable. A blocker resilient wideband receiver is proposed in [3] with two point cancellation of TX leakage and TX noise in receive band. The receiver uses a current mode architecture with a common gate (CG)-common source (CS) noise cancelling low noise transconductance amplifier (LNTA). The receiver is designed for a specific transmitter (TX) leakage cancellation and as a result, the receiver may still be desensitized by other strong out-of-band interference. The leakage cancellation is also dependent on process corners. N-path filters are exploited in RF transceivers to address blocker tolerance and high RF selectivity [4]. However, there are several drawbacks: (1) the low noise amplifier (LNA) must withstand strong blockers at its input and (2)low order filter transfer function does not provide sufficient selectivity in narrow band applications. To increase the selectivity of the receiver, a notch filter in the feedback path of an LNA is introduced [5]. However, this architecture suffers from TX leakage in the receive band.

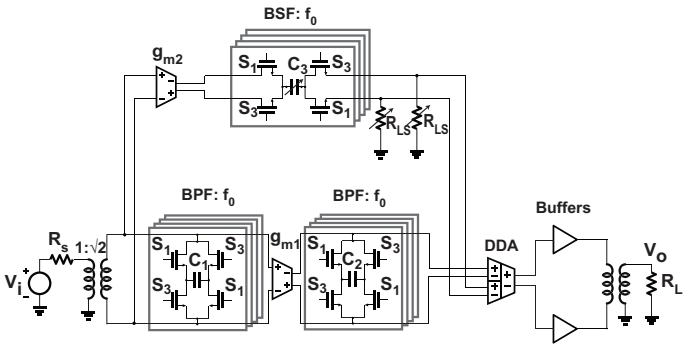

Fig. 1. (a) Proposed N-path bandpass filter with integrated notch.

A tunable bandpass filter with an integrated adaptive notch is presented in this paper. The filter will be used in front of the LNA to handle large out-of-band blockers. The filter can handle a particular blocker by generating a notch at the blocker

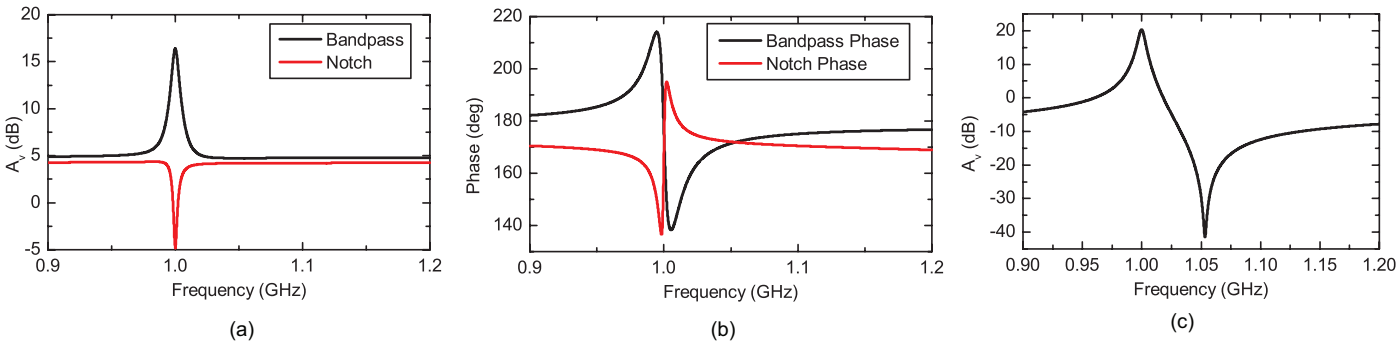

Fig. 2. (a) Magnitude response of bandpass and notch filter (b) Phase response of bandpass and notch filter (c) The overall filter response including DDA gain ($\sim$ 5 dB).

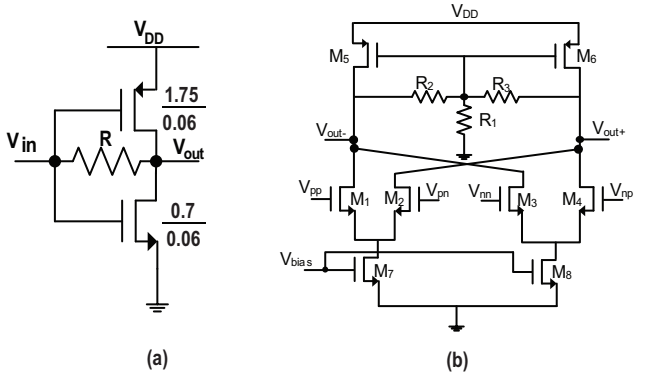

Fig. 3. (a) The unit $G_{\rm m}$ cell that is used with different scaling factors (b) The differential difference amplifier

frequency. In section II, the design of the proposed bandpass filter is demonstrated. Section III describes the simulation results and section IV concludes the paper.

II. Proposed Bandpass Filter Architecture

The proposed filter consists of two bandpass sections, g_m cells and one notch sections, all implemented with N-path switched-capacitor circuits. The bandpass filter is comprised of transconductor cell and two parallel resonant tanks implemented with 4-path switched-cap filters. The notch filter is comprised of transconductor cell and one series resonant tanks implemented with 4-path switched-cap filters. An N-path filter can resemble an LC tank with a tunable center frequency and constant bandwidth [6]. The schematic of the proposed filter is shown in Fig. 1. The g_m cells are used to match the gain in both the bandpass and notch sections and to reduce noise in subsequent stages. The gain of the notch section is changed by varying the output load resistance. A differential difference amplifier (DDA) takes the differential input of both the bandpass and notch sections and generate the differential output.

The basic operation of the filter is clearly understandable from Fig. 2. Fig. 2(a) shows the individual bandpass and notch filter magnitude response and Fig. 2(b) shows the corresponding phase response. The phase is identical at a particular frequency (1.052 GHz) and the magnitude difference is small. As a result, a notch is created in that frequency. The notch frequency can be shifted by changing the notch capacitance.

A $g_{\rm m}$ cell is incorporated after the first bandpass filter to increase the gain and to reduce the noise from subsequent stages. A single $g_{\rm m}$ cell is shown in Fig. 3(a). The g_m cells are implemented with self biased inverters and low V_{th} transistors are used in the g_m cells to reduce noise. 40 parallel $g_{\rm m}$ cells are used to implement $g_{\rm m1}$ and 5 parallel g_m cells are used to implement g_{m2}. The DDA schematic is shown in Fig. 3(b). The DDA has a common mode feedback implemented with resistors.

The transfer function of the notch filter is given by

$$H_{0,BS}(s) = -ND \times \frac{s g_{m2} r_{o2} R_{LS} C_3}{1 + s C_3 R_T} \times \mathrm{sinc}^2(\pi D) + (1 - ND) \quad (1)$$

where $r_{\rm o2}$ is the output impedance of the second transconductor cell (g_{m2}), R_{LS} is the load resistance of the notch filter, C_3 is the baseband capacitance used in the notch filter and $R_T = R_{sw} + r_{o2} + R_{LS}$. N is the number of phases and D is the duty cycle of the multiphase clock. In ideal case, $D = 25\%$ for a 4-phase filter. R_{sw} is the on resistance of the switches. By changing the load resistance of the notch filter, the gain of the notch filter can be changed and the notch can be created. The resistor is changed by placing a transistor in series with the load resistance. The transistor operates in triode region and the resistance is changed by controlling the gate voltage of the transistor. The nominal load resistance of the notch filter is 76 Ω. The transistor size is (W/L = 40 μm/60 nm).

The transistor sizes used in the bandpass and notch filters are (W/L = 10 μm/60 nm) and (W/L = 40 μm/60 nm) respectively. The baseband capacitors used in the bandpass filters are 80 pF. The baseband capacitor in the notch filter is changed from negative resistances are used after second bandpass filter to increase the Q of the filter. The negative resistances are implemented with back-to-back inverters. The negative resistors have a separate supply voltage with nominal value of 1.2 V. The parasitic capacitance at each node of the filter modifies the equivalent resistance of that node which is frequency dependent. As the clock frequency reduces, the Q-factor of the filter increases which leads to higher ripples in the pass-band of the filter for low clock frequencies. To overcome that problem, the supply voltage of the negative resistors is

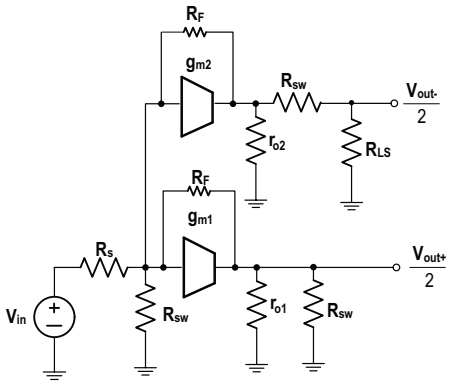

Fig. 4. A simplified schematic of the filter to calculate the stopband rejection. The baseband capacitors are shorted to ground for frequencies far from the passband of the filter.

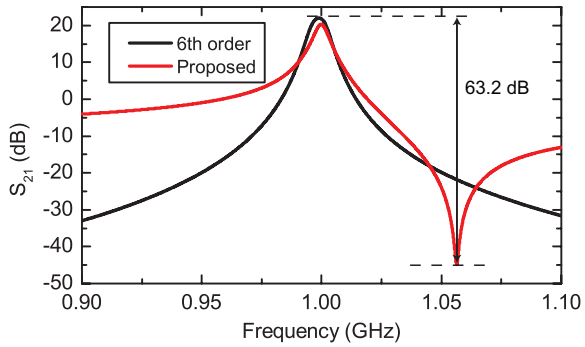

Fig. 5. Comparison between all pole filter and the proposed filter.

reduced for low clock frequencies.

The overall filter transfer function is given by

$$H_0(s) = \frac{N(s)}{(1+sCR_s)(1+sCR_{LS})(1+sCr_{o2})} \quad (2)$$

where, $C = C_1 = C_2 = C_3$

$$N(s) = (1+sCR_{sw})(s^2C^2(g_{m2}R_{LS}r_{o2}^2 - g_{m1}r_{o1}R_{sw}R_{LS}) + sCg_{m2}r_{o2}R_{LS} - g_{m1}r_{o1}) \quad (3)$$

We know that the gain of a simple N-path filter is $\mathrm{sinc}^2\left(\frac{\pi}{N}\right)$ at its center frequency. For perfect duty cycles, the stopband rejection, A_{sb} of the filter can be found using the simplified circuit shown in Fig. 4 and it is described in (4).

$$A_{\mathrm{sb}} = \frac{g_{m1}\left(R_{sw}\|r_{o1}\right) - g_{m2}R_{LS}}{\mathrm{sinc}^2\left(\frac{\pi}{4}\right) \times g_{m1}R_F} \times \left(\frac{R_{\mathrm{sw}}}{R_{\mathrm{s}} + R_{\mathrm{sw}}}\right) \quad (4)$$

where R_F is the feedback resistance used in the g_m cells and we assume $r_{o2} \gg R_{sw}$. The stopband rejection of the filter is 26.2 dB. The simplified block diagram of quadrature clock generator is shown in [7], where a master clock at 4 times the switching frequency is applied externally. A D flip-flop based divider divides the input clock by 4. The clock signals are ac-coupled to the gate of each switch with a bias voltage of 0.75V.

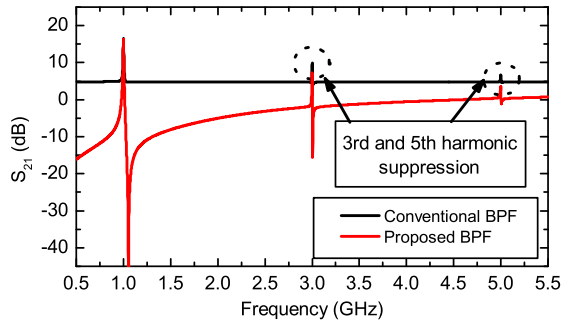

Fig. 6. The proposed filter shows both third and fifth harmonic suppression compared with all pole bandpass filter.

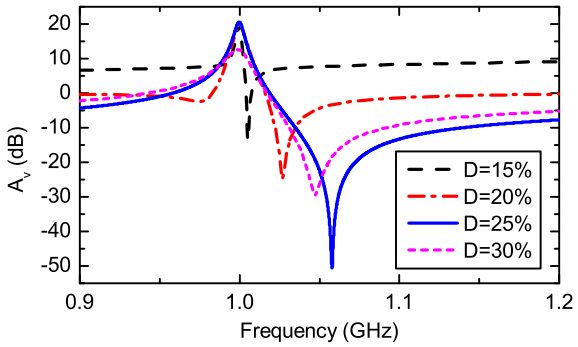

Fig. 7. The transfer function of the filter with duty cycle variations

III. Simulation Results

The proposed filter was designed using 65 nm CMOS technology. The baseband capacitors are realized by MIM capacitors and the resistors are implemented with N+ poly resistor without salicide. The proposed filter is compared with an all pole 6th order Butterworth filter as both the proposed and 6th order filter consume similar area. The proposed filter has 21 dB more rejection at 1.052 GHz compared with all pole filter. As a result, the proposed filter can significantly block the strong transmitter in the receive band. The filter has 20.3 dB gain provided by the g_{m} cells as shown in Fig. 5 with passband ripple of 0.2 dB. The filter has 63.2 dB rejection at 50 MHz offset from the center frequency of the filter. The NF is 3 dB which only degrades to 3.68 dB in presence of a 0-dBm blocker at 50 MHz offset. The third and fifth harmonics are also suppressed due to the subtraction of bandpass and notch filters. The third harmonic is suppressed by 3 dB and the fifth harmonic is suppressed by 8 dB as shown in Fig. 6.

The input frequencies around $(kN \pm 1)f_s$ will be folded back into the desired frequency band around f_s. The strongest folding term is from $3f_s$ and will become smaller as k is increased. The simulated harmonic folding ($|H_4| = -30$ dB) is quite small due to the suppression of third and fifth harmonics. The transfer function of the filter with different clock duty cycle is shown in Fig. 7. The figure clearly shows that the maximum notch depth is achieved for duty cycle=25%. The notch frequency can also be shifted by changing the notch

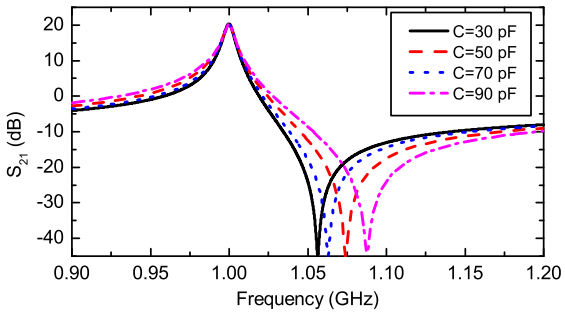

Fig. 8. The notch frequency is shifted by changing the notch filter capacitors

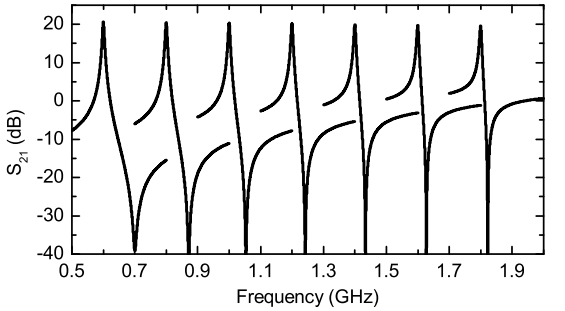

Fig. 9. The simulated transfer function of the filter shown at every 200 MHz over the frequency range from 0.6 GHz to 1.8 GHz.

filter capacitance (C_3). As a result, the proposed filter is robust against process and temperature variations. The transfer function of the filter with different notch capacitance is shown in Fig. 8. As the notch frequency is shifted approximately 30 MHz, the proposed filter can handle strong out of band blockers as well as the transmitter in that frequency range. The filter is tunable from 0.6 GHz to 1.8 GHz and the transfer function over the whole range is shown in Fig. 9. The notch offset is higher for low center frequency compared with high center frequency as very high values of capacitor is needed to create the notch at the same offset frequency. The BW of the filter is 8.7 MHz. The power consumption from the analog blocks is 24.4 mW and the digital power varies from 7.4 to 46.1 mW. The in-band IIP3 of the filter is -4.42 dBm. The simulated out-of-band (OOB) IIP3 for different offset frequencies from $f_{\rm lo} = 1$ GHz is shown in Fig. 10(a). The simulated out-of-band IIP3 (OOB) of +18.97 dBm is obtained at $\triangle f$ of 50 MHz and $f_{\rm lo}$ of 1 GHz. The layout of the proposed filter is shown in Fig. 10(b), which occupies 0.79 mm^2 area. The filter is compared with state-of-the-art integrated filters in Table I.

IV. Conclusion

A bandpass filter with integrated notch and harmonic suppression is presented. The proposed filter has been implemented in 65nm CMOS technology and can be integrated into the RF transceiver chips. The filter can handle large out-of-band blockers at a particular offset by creating a notch at that frequency. The notch frequency can also be shifted. As a result, the receiver is not desensitized by strong blockers including

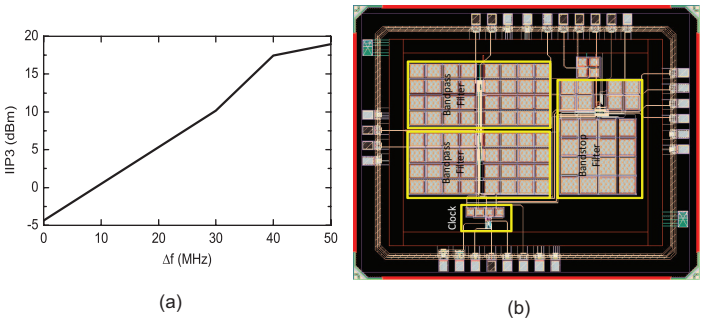

Fig. 10. (a) Simulated out-of-band IIP3 of the filter for different offset frequencies from center frequency of the filter. (f_{lo}=1 GHz) (b) Chip layout of the proposed filter.

TABLE I
Comparison Table

	Borna [2]	Park [5]	Ghaffari [6]	This work
Circuit Type	Receiver	Receiver	Filter	Filter
CMOS Tech. [nm]	90	65	65	65
Frequency range [GHz]	2.5	0.05–2.5	0.1–1	0.6–1.8
Gain [dB]	110 mS	38	-2	20.3
Blocker rejection @ 50 MHz offset	20	-	16	**63.2**
BW [MHz]	10	0.4∼20	35	8.7
NF [dB]	-	2.9	3–5	3.04
NF with 0-dBm blocker @ given offset [dB]	-	5.4 [23 MHz]	-	**3.68** [50 MHz]
IIP3 (OOB) [dB]	-6	10	>+14	**18.97**
$V_{\rm DD}$ [volts]	1.2	1.2	1.2	1.2
Power [mW]	84	20	2–20	31.8–70.5

the transmitter. The notch depth can be maintained constant by changing the load resistance of the notch filter. This filter will enable the implementation of reconfigurable multiband radio with variable bandwidth such as required for LTE.

References

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