Reconfigurable N-Path RF Front-end Filter with Improved Blocker Rejection

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Abstract— In this paper an RF channel select filter with improved blocker rejection is presented. The proposed filter consists of three parallel resonant tanks and two series resonant tanks all implemented with N-path switched-cap filters. Due to the inclusion of notch filters between the bandpass filters, the rejection of the filter in the vicinity of the passband is higher compared with any existing filters. Out-of-band blockers are suppressed due to high filter rejection. The filter is tunable from 0.2 GHz to 1.8 GHz. The proposed tunable filter has 48.3 dB rejection at 20 MHz offset and has 58.8 dB rejection at 45 MHz offset from the center frequency. The high stop-band rejection of 71.2 dB has been achieved by creating notches outside the bandwidth of the filter.

I. INTRODUCTION

A cellular radio receiver is required to recover a weak desired signal in presence of other in-band and out-of-band interfering signals (blockers). These interfering signals near the desired signal need to be suppressed. To that end, a band selection filter is used to provide attenuation for out-of-band signals, and a subsequent baseband lowpass channel select filters provide channel selection. Existing filters providing channel selection directly at RF for cellular applications does not have adequate rejection in the stopband to fulfil LTE requirements.

Current CMOS receivers exploit SAW filters to sufficiently attenuate large out of band blockers due to the high-Q of these filters. To cover different frequency bands multiple SAW filters are necessary which increase the cost and complexity of the system. It is desirable to have an integrated bandpass filter which is tunable over a wide frequency range. The desired tunable filter should have high selectivity to mitigate large out of band blockers to relax the out-of-band linearity requirement of the subsequent stages in the receiver chain and high dynamic range. Several techniques to implement on-chip CMOS band pass filters have been developed. CMOS LC filters with Q-enhancement [1] suffer from limited tunability and a limited dynamic range (DR). They are also not process scalable due to the use of on-chip inductors. $G_{\mathrm{m}} - C$ filters [2] suffer from trade-off between center frequency, DC power dissipation, dynamic range and Q factor. Separate tuning circuitry is also needed for those filters. N-path bandpass filters (BPFs) offer high-Q while their center frequency is tuned by the clock frequency. Compared to $G_{\mathrm{m}} - C$ filters, this technique decouples the required Q from DR.

There are no tracking filters that have good pass-band characteristics while having a high stop-band rejection outside the channel bandwidth of the filter. In the proposed work, a method for implementing a tracking filter with high stop-band rejection is described. The filter fulfils the requirements of LTE and WCDMA cellular radios in terms of stop-band rejection.

II. STATE OF THE ART

Recently there has been growing trend to implement N-path bandpass filters for RF channel selection. An N-path filter is composed of N identical linear time invariant networks (LTI) and 2N frequency mixers driven by time/phase shifted versions of the clock [3]. It can be shown that the mixing results in a band-pass around the mixing frequency, if the LTI networks exhibit a low-pass characteristic around DC. Expressed in other way, the input signal is down-converted to baseband, filtered by the LTI network and then up-converted again to the original band of V_{in}. The center frequency is determined by the mixing frequency, insensitive to filter component values. A high mixing frequency combined with a narrow low-pass filter bandwidth allows for a very high filter Q.

A tunable 6th order BPF is proposed in [4] for high rejection. This is an all pole Butterworth filter. The parallel LC tanks are implemented with N-path filters. The series LC tank is converted to a parallel LC tank by using two gyrators. The gyrators are lossy and unstable at high frequencies. The filter has 38 dB rejection at 20 MHz offset and approximately 45 dB rejection at 45 MHz offset from the center frequency, which is not adequate to fulfill the LTE requirement. Another N-path tunable bandpass filter is shown in [3]. The filter is tunable from 0.1–1.1 GHz. However, the filter rejection in the vicinity of the passband (as an example, 20 MHz away from the 3-dB bandwidth) is quite limited (8 dB). The filter rejection is primarily limited by the on resistance of the switches. Another bandpass filter based on $G_{\mathrm{m}} - C$ architecture is shown in [5]. The filter has limited tuning range from 0.24–0.53 GHz and the NF is high (8 dB). A GSM receiver for RF channel selection is proposed in [6]. The rejection is also limited (30 dB at 20 MHz offset) and the passband ripple is high.
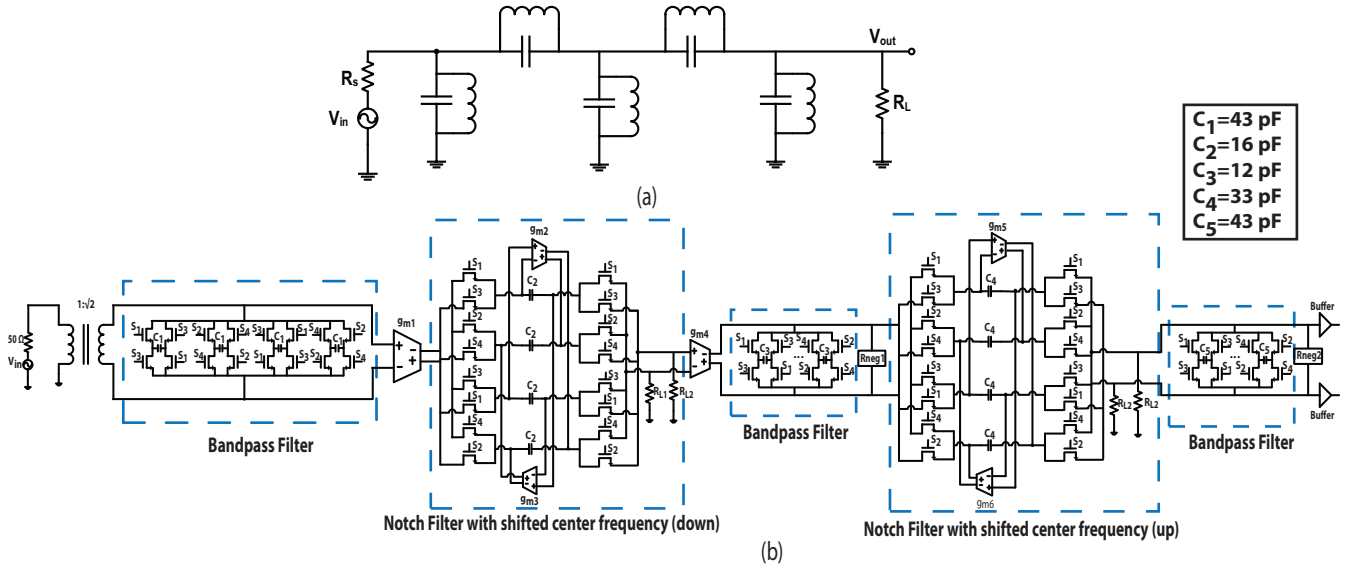
Fig. 1. (a) A conventional elliptic parametric filter (b) Transistor level schematic of the proposed filter

III. PROPOSED ARCHITECTURE

The proposed filter is based on elliptic filter topology. A conventional elliptic parametric BPF is shown in Fig. 1(a). A major advantage of the elliptic filter is the independent placement of zeros in the transfer function. An N-path filter can resemble an LC tank with a tunable center frequency and constant bandwidth [4]. The proposed filter schematic is shown in Fig. 1(b). Each shunt LC tank in the elliptic filter is implemented with N-path switched-capacitor bandpass filters [4] and each series LC tank is implemented with N-path switched-capacitor notch filters [7]. The tunable bandpass filter is implemented with R-C configuration of N-path filters. A g_m cell is incorporated after the first bandpass filter to increase the gain and to reduce the noise from subsequent stages. A single g_m cell (1x) is shown in Fig. 2(a). 15 parallel g_m cells are used to implement g_{m1}. The values of baseband capacitors are shown in Fig. 1.

If the notch filter has the same center frequency as that of the bandpass filter then the output of the filter is zero, which is not desirable. For that reason, the center frequency of the notch filter is shifted to a different offset frequency (as an example, 20 MHz below the center frequency of the bandpass filter) compared to the center frequency of the bandpass filter. The center frequency of the notch filters can be independently chosen irrespective of the center frequency of the bandpass filters. The tunable notch filter is implemented with C-R configuration of N-path filters. The resonant/center frequency of the notch filter is shifted by using two g_m-cells (g_{m2} and g_{m3}). A differential amplifier with common mode feedback is used to implement the gm cells as shown in Fig. 2(b). The modified baseband capacitance impedance due to feedforward and feedback gm cells is governed by (1).

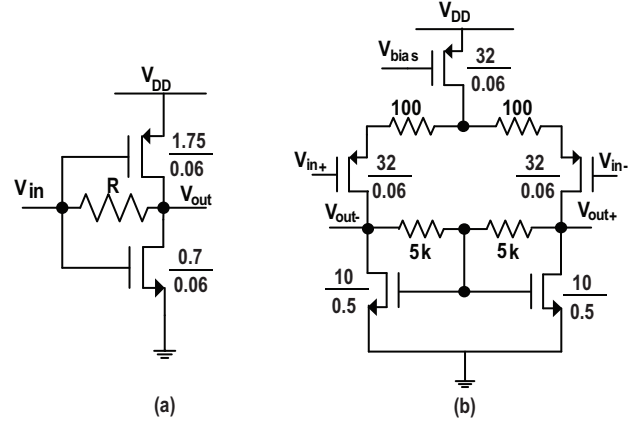$$Z_{C_2'}(\omega) = \frac{2R_{\text{sw}}}{1 + jR_{\text{sw}}C_2(\omega + \frac{2G_m}{C_2})} \quad (1)$$

Fig. 2. (a) The unit G_m cell that is used in the bandpass filter with different scaling factors (b) G_m cell used in notch filters

where R_{sw} is the on resistance of the switches and C_2 is the baseband capacitance of the notch filter. The equation clearly shows that the filter transfer function is simply shifted to the left by $2g_{m2,3}/2\pi C_2$. By adjusting the values of $g_{m2,3}$ and C_2, the N-path implementation of the notch filter with feed-forward and feedback gm cells shift the center frequency 20 MHz lower (where we want the notch) than the center frequency of the filter. The notch filter is clearly shown in Fig. 3.

To compensate the loss from the notch filter and to reduce the noise from subsequent stages another g_m cell (g_{m4}) is incorporated. Six identical gm cells (as shown in Fig. 2(a)) are used in parallel to implement g_{m6}. Then a second N-path bandpass filter is placed. After that a second notch filter is integrated with different center frequency (as an example, 20 MHz above the center frequency of the bandpass filter). The frequency is also shifted using the same feed-forward and feedback g_m cells. However, the inputs and outputs of the gm
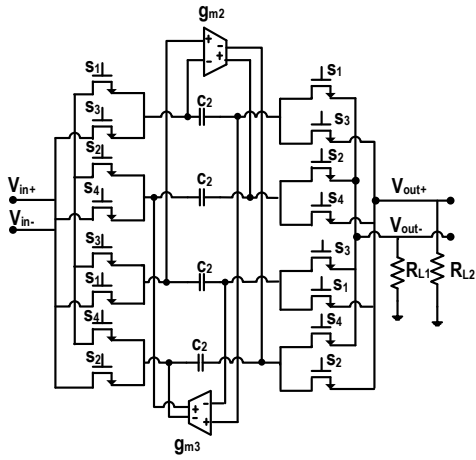
Fig. 3. A tunable notch filter with notch shifted to a value lower than clock frequency.
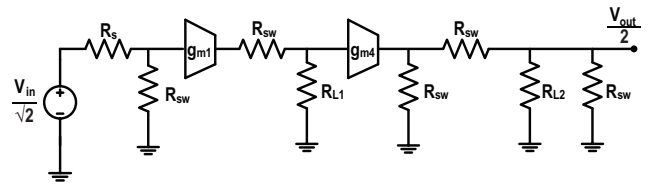

Fig. 4. A simplified schematic of the filter to calculate the stopband rejection. The baseband capacitors are shorted to ground for frequencies far from the passband of the filter and $\sqrt{2}$ is the voltage gain of the balun
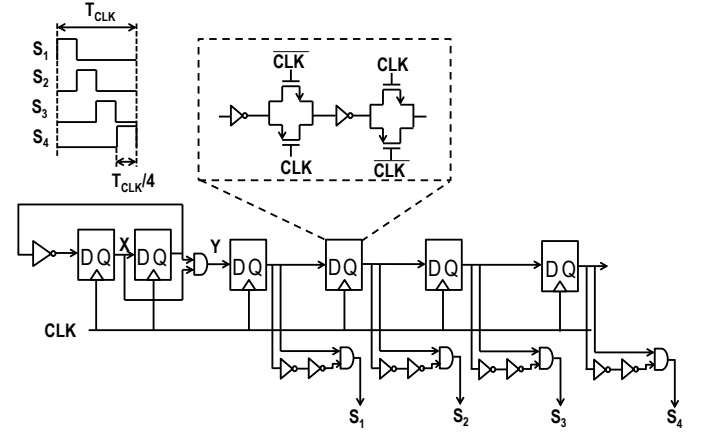

Fig. 5. Multiphase clock generator using D flip-flops

cells are different than the first notch filter as shown in Fig. 3. Finally an N-path tunable bandpass filter is placed with output buffers. The center frequency of individual bandpass filters is same; which is the center frequency of the proposed filter. The notches create zeros at offset frequencies of the filter.

Negative resistances are used after second and third band-pass filters to increase the Q of the filter. The negative resistances are implemented with back-to-back inverters. The negative resistors have a separate supply voltage with nominal value of 1.2 V. The parasitic capacitance at each node of the filter modifies the equivalent resistance of that node which is frequency dependent. As the clock frequency reduces, the Q-factor of the filter increases which leads to higher ripples in the pass-band of the filter for low clock frequencies. To overcome that problem, the supply voltage of the negative resistors is reduced for low clock frequencies.

The input impedance of a notch filter at a frequency $\omega = \omega_0 + \triangle\omega$ is given by

$$Z_{\text{in}1} \simeq \frac{R_{\text{sw}}}{1 + 2jQ_0 \frac{\triangle\omega}{\omega_0}} \qquad (2)$$

Similarly, the input impedance for the second bandstop filter is

$$Z_{\text{in}2} \simeq \frac{R_{\text{sw}}}{1 - 2jQ_0 \frac{\triangle\omega}{\omega_0}} \qquad (3)$$

However, both the input impedances can be simplified to R_{sw} if $\frac{\triangle\omega}{\omega_0} \ll 1$ and Q_0 is not high. We know that the gain of a simple N-path filter is $\text{sinc}^2\left(\frac{\pi}{N}\right)$ at its center frequency. For perfect duty cycles, the stopband rejection, A_{sb} of the filter can be found using the simplified circuit shown in Fig. 4 and it is described in (4).

$$A_{\text{sb}} = \frac{1}{\text{sinc}^2\left(\frac{\pi}{4}\right)} \times \frac{R_{\text{T}}}{R_{\text{L}2}} \times \left(\frac{R_{\text{sw}}}{R_{\text{s}} + R_{\text{sw}}}\right) \qquad (4)$$

where

$$R_{\text{T}} = \frac{R_{\text{sw}}\left(R_{\text{L}2}\|R_{\text{sw}}\right)}{2R_{\text{sw}} + \left(R_{\text{L}2}\|R_{\text{sw}}\right)} \qquad (5)$$

$R_{\text{L}1}$, $R_{\text{L}2}$ are the load capacitances of the first and second notch filters respectively. The values of the load capacitances used in the simulation are 30 kΩ and 10 kΩ respectively.

The simplified block diagram of quadrature clock generator is shown in Fig. 5. A master clock (CLK) is applied from off-chip which is 4 times faster than the switching frequency. A D flip-flop based divider divides the input clock by 4. The AND gate between node X and Y generate 25% duty cycle clock. The output and a delayed version of the output is send to an AND gate to generate the 25% duty cycle clock which reduces clock overlapping. The ideal 25% duty cycle clock is also shown in the figure.
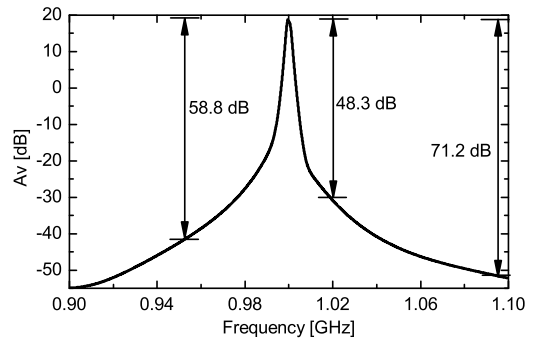

Fig. 6. The simulated transfer function of the filter.

TABLE I

PERFORMANCE SUMMARY

	Ghaffari [3]	Darvishi [4]	Oualkadi [5]	This work
CMOS Tech. [nm]	65	65	350	65
Frequency range [GHz]	0.1–1	0.1–1.2	0.24–0.53	**0.2–1.8**
Gain [dB]	-2	25	-2.2	18.2
Filter rejection @ 20 MHz offset	8	38	30	**48.8**
Filter rejection @ 45 MHz offset	16	45	34	**58.3**
BW [MHz]	35	8	2–5	4
NF [dB]	3–5	2.8	8	7.5
Stop-band rejection [dB]	15	59	38	**71.2**
IIP3 (OOB) [dB]	>+14	+26	-	17.96
V_{DD} [volts]	1.2	1.2	3	1.2
Power [mW]	2–20	18–57.4	63	24.1–72.8

Fig. 8. The simulated transfer function of the filter shown at every 100 MHz over the frequency range from 0.2 GHz to 1.8 GHz.
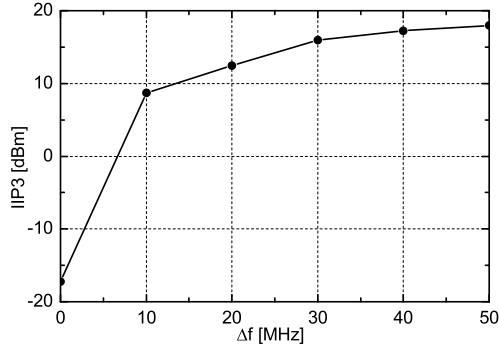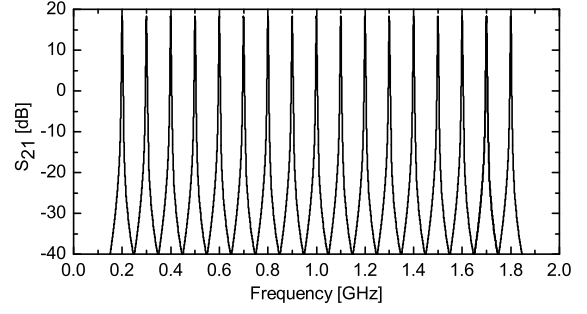

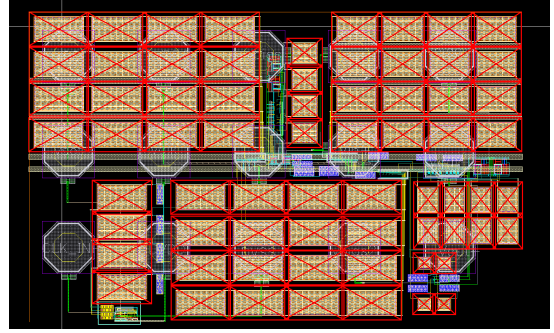Fig. 9. Chip layout of the proposed filter.

Fig. 7. Simulated out-of-band IIP3 of the filter for different offset frequencies from center frequency of the filter. (f_{lo}=1 GHz)

IV. SIMULATION RESULTS

The proposed filter was designed using 65 nm CMOS technology. The filter has 18.2 dB gain provided by the g_m cells as shown in Fig. 6 with passband ripple of 0.6 dB. The filter has 48.8 dB rejection at 20 MHz offset and has 58.3 dB rejection at 45 MHz offset from the center frequency as shown in Fig. 6. The stopband rejection is 71.2 dB. The high stop-band rejection is achieved by the notches created outside the bandwidth of the filter. The notches can also be independently tuned. The in-band IIP3 is -16.7 dB. The simulated out-of-band (OOB) IIP3 for different offset frequencies from f_{lo}= 1 GHz is shown in Fig. 7. The IIP3 (OOB) of +17.96 dBm is obtained at $\triangle f$ of 50 MHz and f_{lo} of 1 GHz. The filter is tunable from 0.2 GHz to 1.8 GHz and the transfer function over the whole range is shown in Fig. 8. The BW of the filter is 4 MHz. The power consumption from the analog blocks is 16.7 mW and the digital power varies from 7.4 to 56.1 mW. The high NF of 7.5 is due to the insertion loss of notch filters in the signal path of the filter. The notch filter has high NF at the center frequency. The chip layout of the proposed filter is shown in Fig. 9. The total chip area is 0.63 mm^2.

V. CONCLUSION

A new bandpass filter with high stopband rejection is proposed. The proposed filter has been implemented in 65nm CMOS technology and can be integrated into the RF transceiver chips. This will result in elimination of several band specific bulky and costly SAW filters and fixed channel selection filters from the handsets. This filter will enable the implementation of reconfigurable multiband radio with variable bandwidth such as required for LTE. The filter is widely tunable and it maintains the stop-band rejection over the wide frequency range.

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