Micromachined Silicon Channels for THz Interconnect

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***Abstract*—This paper, for the first time, presents planar silicon process compatible interconnect channels, which can be extended to THz frequencies for high performance interconnect systems to fill the long-standing intra-/inter- chip interconnect gap.**

***Keywords*—Channel; dielectric waveguide; interconnect; micromachined; THz.**

I. Introduction

Semiconductor technology advancements generate two side effects. On one side, it speeds up data processing and reduces energy consumption per bit. On the other side, it keeps increasing transmission data rate requirements and generates the larger gap from interconnect capabilities. Yablonolvich envisions that the energy used for data communication is orders of magnitude higher than the energy used for data processing and storage [1]. Therefore, in the near future, majority of the energy will be consumed by data transmitting.

Intra-/inter- chip interconnects impose a wide range of stringent performance requirements: energy efficiency, bandwidth density, reliability, cost, etc. To meet these requirements, small size, low loss and low cost interconnect channels are crucial. THz interconnect channels, due to small sizes, have been investigated based on a variety of materials and structures [2]-[5], with demonstrated losses of $<$ 1 dB/m. These low loss THz channels can potentially alleviate link budgets to boost interconnect efficiency.

However, till now, no investigations have been conducted on planar silicon process compatible THz channels for intra-/inter- chip interconnects, which have their unique features. This paper discusses the design of planar silicon process compatible THz channels for interconnect systems, together with fabrication and characterization procedures. The frequency choice of 200 GHz is based on characterization capabilities and test convenience. The design concept and fabrication procedure can be equally applied at higher frequencies.

II. Design of Channel and Coupler

A. Channel Design

The choice of channel material should consider several factors: 1) being compatible with silicon processing; 2) having large permittivity to concentrate the field along the channel for low loss and result in small channel size for large bandwidth density. Therefore, silicon, with relative permittivity around 11.9, is chosen as the channel material. To reduce the propagation loss, high resistivity (HR >5,000 Ω-cm^2) silicon is used in this work.

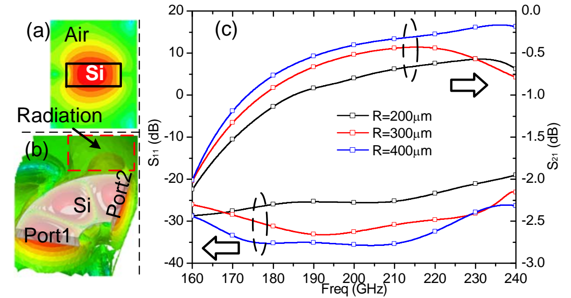

Figure 1. (a) The H-field distribution of Port, (b) the simulated H-field distribution of the bending structure, and (c) the simulated S_{11} and S_{21} of the bending structures with different radius.

To couple signals between two planar ICs, bending structure is a natural approach. The design of bending structure has several tradeoffs. First, it is preferred that the bending radius be small to be compact and low profile so that the channels are reliable. On the other hand, when the radius is too small, the propagating waves tend to leak outside of the channel to cause large losses. To choose optimal radius, we have conducted extensive simulation of the wave propagation based on different radius (Fig. 1).

Fig. 1(a) illustrates the H-field distribution on the excitation port, which indicates that the majority of the field is confined within the channel due to the large permittivity difference between silicon and the air. Fig. 1(b) shows the H-field distribution of a bending structure with the radius of 200 μm. It shows that some of field leaks out of the channel and increases the propagation loss. Fig. 1(c) presents the simulated S_{21} and S_{11} for different radius. S_{11}s are maintained $<$ -20 dB and S_{21}s are $<$ -1 dB for all the three cases, with S_{21} improving with a larger radius. Simulation results indicate that further increasing of the radius higher than 400 μm results in incremental improvement in insertion loss, which indicates that wave leakage becomes less significant.

B. Channel Coupler Design

The design of channel coupler also needs to be compatible with planar silicon processes, with minimum changes of the fabrication procedure. In addition, the generated field should be convenient to couple to the channel with minimum coupling loss. Therefore, we choose patch antenna based coupler, which is completely compatible with silicon processes and the perpendicular propagation pattern matches with channel feeding.

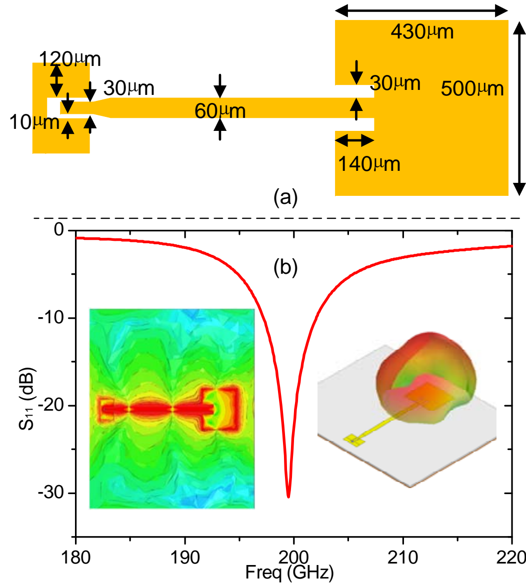

Figure 2. (a) The patch antenna based channel coupler structure, and (b) the simulated S_{11} with insets showing the near field and far field distribution at 200 GHz.

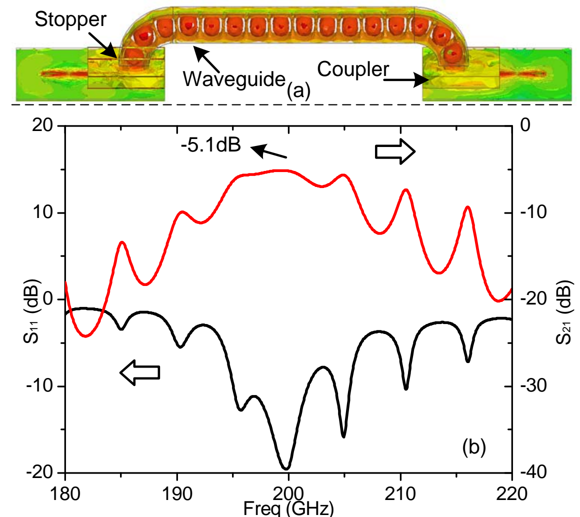

Figure 3. (a) The simulated H-field distribution, and (b) S_{11} and S_{21} of complete structure.

Rogers 3850, with 1 mil thickness and dielectric constant of 2.9, is chosen as the antenna substrate. The coupling structure consists of a coplanar waveguide (CPW), a transition from CPW to microstrip line, a microstrip line, and the patch antenna based channel coupler. All the metal, except the bottom copper-based ground, is for minimum oxidization. To simplify the coupler fabrication, a via-less CPW to microstrip line transition is adopted. The bottom metal is ac-coupled through the thin substrate. Furthermore, by choosing ground plane width much smaller than the signal wavelength, higher order modes can be avoided to reduce insertion loss [6]. The complete channel coupler structure and dimension are shown in Fig. 2(a). Fig. 2(b) presents the simulated S_{11} with a -10 dB bandwidth of 4.8 GHz. The insets show the near-field and far-field distribution at 200 GHz.

C. Complete Interconnect Channel Structure

To accurately control the coupling gap between the coupler and the channel, a low loss dielectric stopper is employed. SU-8 has been reported to have low loss tangent (6.3×10^{-6}) at THz [7]. With a dielectric constant of 2.9, the SU-8 stopper changes the coupler resonant frequency and the feeding impedance. The final coupler sizes (400 μm $\times$ 500 μm) with SU-8 are therefore adjusted through EM tools to resonate around 200 GHz.

Fig. 3(a) shows the complete interconnect structure, including the channel, the stopper, and the coupler, together with a plot of the magnitude of H-field. The total loss through the link path is approximately 5.1 dB at 200 GHz as shown in Fig. 3(b).

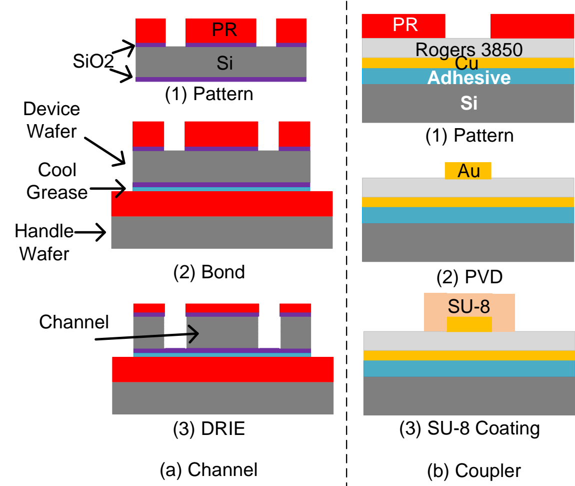

Figure 4. (a) The silicon channel fabrication procedure, and (b) the patch antenna fabrication procedure.

III. Fabrication and Measurement Results

A. Fabrication Procedure

The micromachining fabrication process is summarized in Fig. 4. The channel is fabricated based on lithography and deep reactive ion etching (DRIE). First, a thick ($\sim$17 μm) photoresist (PR) is patterned on the high resistance (HR) silicon wafer and hard-baked. Using cool grease, the HR silicon wafer is bonded on the top of a handle wafer. The HR wafer is then etched by DRIE process. After removing the cool grease, the individual channels can be separated.

The patch coupler is fabricated using lithography and physical vapor deposition (PVD). First, using an adhesive, Rogers 3850 is bonded on the top of a handle silicon wafer. Then the top copper is etched off. The antenna pattern is then defined by a layer of photoresist. A layer of titanium (50 nm) and

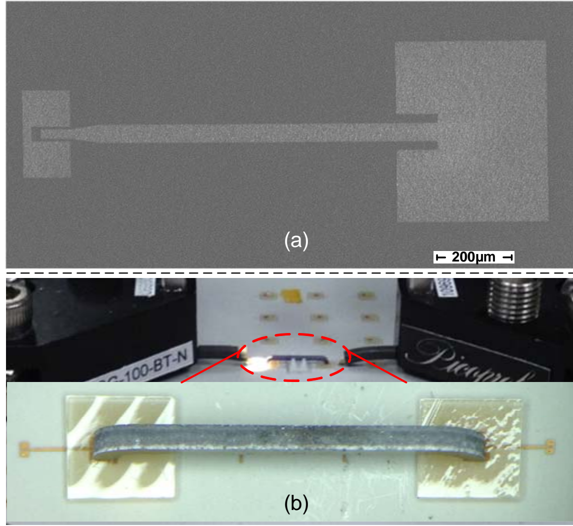

Figure 5. (a) The SEM photograph of the coupler, and (b) the photo of the test bench.

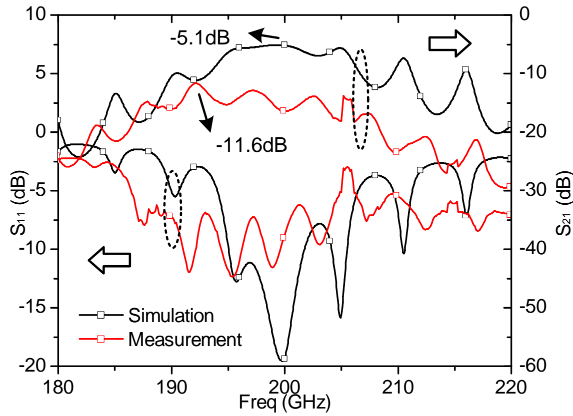

Figure 6. The comparison of S_{11} and S_{21} of simulation and measurement.

gold (300 nm) is evaporated onto the substrate to form the top metal by a lift-off process. A 200-μm thick SU8-2075 layer is then patterned to construct the dielectric stopper.

To support the channel and facilitate assembly, a 3D printed holder with a low dielectric constant material (about 2.7) is utilized, which has negligible effects on the signal propagation based on full-wave simulation. Fig. 5(a) shows the scanning electron microscope (SEM) photograph of the coupler and Fig. 5(b) presents the test bench consisting of the probe, the interconnect structure, and the holder. The measurement is done with an Agilent PNA-X network analyzer, with a pair of Virginia Diodes frequency extenders to cover the G-band (140 $\sim$ 220 GHz) frequency range.

B. Measurement Results

Fig. 6 and Fig. 7 summarize the measurement results. In Fig. 6, the channel length is 6 mm, the bend radius is 300 μm, and the channel thickness is 400 μm. It presents the measured S parameters with the comparison of simulation results. The

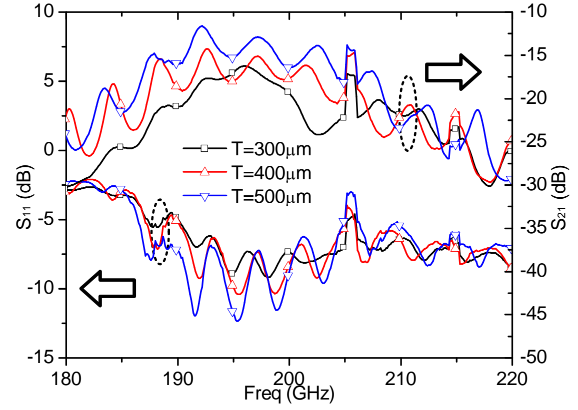

Figure 7. The comparison of S_{11} and S_{21} of measurement results among channels with different thickness.

peak S_{21} is -11.6 dB, which presents 6.5 dB performance degradation comparing with simulation results. The resonant frequency is shifted from 200 GHz to 190 GHz. In Fig. 7, the channel and bend radius is same as Fig.6′s device. It shows the measured SPs for different channel thickness, from 300 μm to 500 μm and demonstrate the insertion loss varying from -16.2 dB to -11.6 dB.

The 6.5 dB difference between simulation and measurement results may come from several factors, such as larger loss tangent of the substrate and SU-8 than that of expected, worse conductivity due to Titanium introduced than pure gold, mis-alignment, non-uniformity of the stopper, and surface roughness of the channel. Further investigation is needed.

IV. Conclusions

This paper, for the first time, demonstrates the interconnect channels to be compatible with planar silicon processes and can be scaled up to THz, which has the potential to eventually solve the long-standing interconnect problems for intra-/inter-chip communications.

Acknowledgment

The authors would like to thank NSF and Dr. George Haddad for funding support.

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