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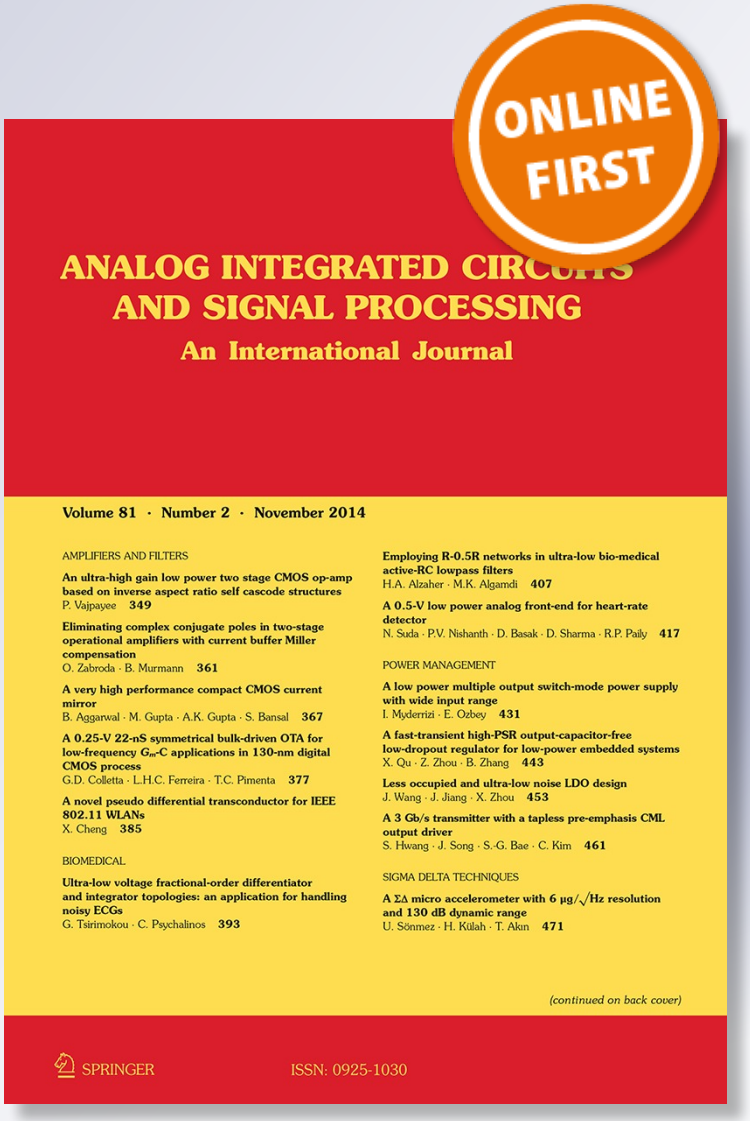

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Integrated D-band transmitter and receiver for wireless data communication in 65 nm CMOS

Zhiwei Xu · Qun Jane Gu · Yi-Cheng Wu · Mau-Chung Frank Chang

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Abstract A 140 GHz transmitter (Tx) and receiver (Rx) chip set has been developed in 65 nm CMOS by using on–off keying non-coherent modulation to support high speed proximity data communication. To the author's best knowledge, it enables the first integrated multi-Gbps data link in D-band by saving power hungry frequency synthesizer, high speed data convertors and complicated digital signal processor. The Tx and Rx occupy 0.03 and 0.12 mm^2 chip areas, respectively. To validate the communication at 140 GHz carrier frequency, a data link has been built to demonstrate up to 2.5 Gbps data rate with power consumption of 115/120 mW for Tx/Rx respectively.

Keywords Injection locking buffer · Low noise amplifier (LNA) · Non-coherent modulation · On–off key · Power amplifier (PA) · Mm-wave circuits · Voltage controlled oscillator (VCO)

1 Introduction

Since the first transatlantic transmission by Marconi, wireless communication has experienced over a century advancement and developed many standards to fulfill various requirements, which cover long distance applications like satellite/cellular communications, short distance applications including wireless local area network (WLAN) and wireless personal area network (WPAN), etc. The recent emerging short-distance 60 GHz technology, specified by IEEE 802.15.3c and 802.11ad, benefits bandwidth hungry applications such as high definition video and high capacity data storage, and promises extremely fast wireless peer-to-peer connectivity [1]. Recently, the electromagnetic spectrum beyond 60 GHz starts to attract increasing interests for multi-gigabit/sec wireless communications. Due to CMOS's substantially increased device speed benefiting from the continuous technology scaling, it is gaining ground in these applications, which are conventionally dominated by III-V processes [2]. For example, the f_T and f_{MAX} of 65 nm CMOS are better than 200 and 250 GHz respectively [3] and make it feasible for emerging millimeter (mm) wave applications. Several higher than 100 GHz mm-wave circuits and systems have already been demonstrated in CMOS [4–8].

In this paper, we want to further push the frontier by demonstrating the a low power, integrated system with 140 GHz carrier that offers up to 2.5 Gbps wireless data link for proximity communications, which address recent increasing data speed demands under bandwidth, space and power limited and reliability/cost constrained conditions for backplane, inter- and intra- chip communications. This paper extends the conference paper [8] with more theory analysis and experiment data. Section II discusses the system architecture of the intended data link. Section III provides detail transmitter and receiver design. Section IV demonstrates the measurement results followed by conclusions in Section V.

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2 System architecture

Wireless communication tends to use complicated modulation methods, i.e. spread spectrum or orthogonal frequency-division multiplexing (OFDM), to cope with severe channel conditions like frequency-selective multipath fading and save sophisticated equalization filter. However, the channel for short range communications, where multipath is not a serious problem, might not be as brutal as that for long distance communications. Especially given a short wavelength of mm-wave frequency (< a few millimeters), the communication link tends to present line-of-sight (LOS) condition representing as a point-to-point link. It greatly simplifies the modulation concerns. On the other hand, in congested low frequency bands, the spectrum efficiency measured by bit/Hz is also a vital consideration for communication systems that generally leads to complicated modulation schemes. Fortunately, spectrum efficiency is not a serious concern in mm-wave regime with tens of GHz available spectrum. Therefore, simple modulation schemes, such as FSK, ASK and PSK, can be adopted to effectively reduce the hardware complexity and still offer multiple Gbps communication data rate. Among them, on–off keying (OOK) modulation, the simplest form of ASK, can represent the data as the presence or absence of a high frequency carrier through binary amplitude modulation. It has been widely used in high data rate optical communication through time-division-multiplex or wavelength-division- multiplex. For wireless communications, OOK has also been applied to establish power efficient links, and V-band transmitters/receivers based upon OOK [9] are also demonstrated to achieve > 1 Gbps data rate.

OOK modulation could offer simple transmitter realization, which results in significant hardware saving and power reduction. In receiver, non-coherent OOK is also favorable to trim down the chip size and power consumption without stringent carrier frequency accuracy requirement. However, such scheme is sensitive to the noise and co-channel interferences, which hurt system's sensitivity when exposed to crowd environments. Additionally, the spectrum efficiency is not optimized due to the directly modulated transmitter without signal shaping. Fortunately, the frequency band at 140 GHz is relative vacant and has tens of GHz spectrum to host high speed data. In addition, non-coherent receiving scheme significantly reduces power consumption by eliminating synthesizers and LO drivers. These lead us to a transmitter/receiver architecture based on non-coherent OOK for intended proximity wireless data communications.

Figure 1 sketches the system architecture. In transmitter, a VCO generates a high frequency signal running at 140 GHz as the carrier, a VCO buffer isolates the VCO core from the OOK modulated PA to stabilize the carrier frequency as well as to support a large output signal swing. The PA accomplishes both signal modulation with 90 % modulation depth and power amplification before transmitting the signal through the antenna. In the receiver, the LNA provides over 20 dB power gain with more than 20 GHz bandwidth centered at 142 GHz. An envelope detector (ED) directly demodulates the incoming OOK RF signal into a low frequency baseband signal, which is then amplified by the following PGA before sending off-chip.

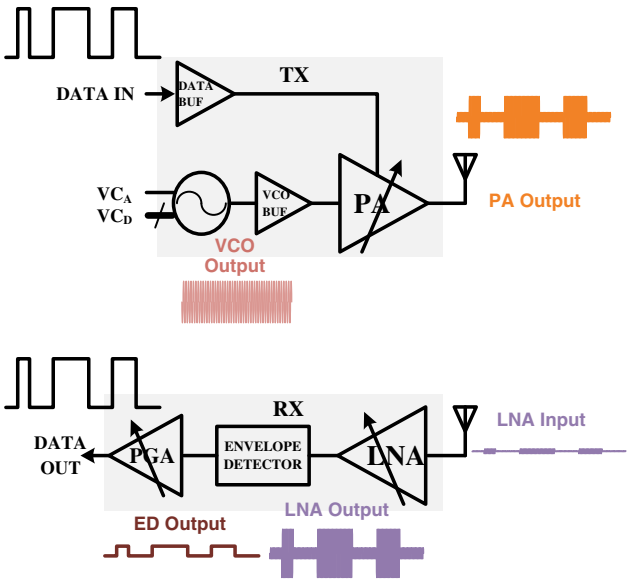


Fig. 1 System architecture of the proposed 140 GHz proximity wireless communication with on–off keying modulation

3 Transmitter and receiver

3.1 Mm-wave device modeling

Accurate device modeling is critical to achieve successful mm-wave circuit design. Normally, foundries do not provide accurate active device model in mm-wave regime; their passive component library is also lack of transformers, transmission lines and inductors at mm-wave frequencies. Therefore, it mandates designers to model both active and passive devices for an effective design. One key reason that active device's performance deviates from its low frequency behavior described by the foundries' model at mm-wave frequencies is due to the external parasitics induced by connections and routing. A proper mm-wave device model, which includes the effects from parasitics, can be assembled by adding the device external parasitics on top of core device model from foundries. Figure 2 illustrates the approach to estimate the external parasitics to

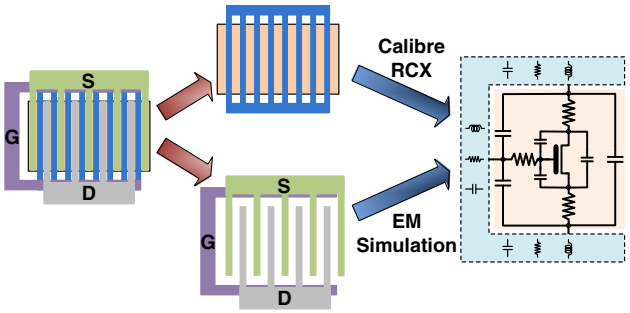


Fig. 2 Active device modeling in mm-wave frequency

be added on top of core device model. First, we separate the device external connection network from the core device. Second, we model the proximity connections with caliber RCX to incorporate the local coupling effects. Then, we utilize EM simulation tools, such as ADS momentum or AnSoft HFSS, to model the accessing lines. The final active device model will be formed by adding these two parts on top of the core device model provided by foundries. As for passive components and inter-stage interconnects, EM simulation tools are used to optimize the design. Corresponding scalable lumped passive component models are built to facilitate circuit optimization in Cadence.

3.2 D-band low noise amplifier

Figure 3 shows the designed fully differential 140 GHz CMOS amplifier. It features a fully differential, 3-stage CS-CG cascode structure with on-chip transmission lines and transformers based inter-stage impedance matching. Different from single-ended amplifiers using capacitor coupling to isolate DC bias between stages, the proposed amplifier utilizes transformers, T1 and T2, to efficiently couple the signals and provide independent bias optimization symmetrically for each stage along the signal path.

When operating at ultra-high frequencies in the intended mm-wave spectra, we find the on-chip transformer and balun quite efficient and can achieve $Q > 25$ and coupling coefficient >0.8 through metal coil stacking. Under such circumstances, signals can be more effectively transmitted between stages by using transformers than capacitors with transmission line stubs. It also leads to more compact circuit layout by merging the transformer with other parasitics as inter-stage T-matching network. Unlike the capacitor coupling that always renders lower voltage swing to the next stage, the transformer coupling offers extra design flexibility to increase next stage input signal voltage swing by increasing the transformer's secondary-to- primary turn ratio. In many cases, this also provides extra design freedom to optimize amplifier's linearity. However, the transformer design is delicate due to its bi-directional nature and requires more precise modeling and design iterations.

To validate the 140 GHz amplifier performance, an individual test chip has been designed and fabricated in 65 nm CMOS [10]. With 2 V supply, the LNA achieves better than −10 dB S11 from 142 to 157 GHz with larger than 10 dB gain from 128 to 157 GHz and a positive gain from 126 to 166 GHz. The measured highest gain is around 20 dB at 143 GHz. The amplifier isolation is better than 25 dB and S22 is less than −5 dB across the desired band. When biased with 1.4 V supply, the amplifier gain drops about 2.5 dB. It is mainly due to the decreased bias current from 51 mA under 2 V to 39 mA under 1.4 V, and the lowering trans-conductance of each stage. The measurement results matched with simulation results with the gain difference about 4 dB. Large signal measurement shows the amplifier delivers larger than 5.7 dBm saturated output power and higher than 3.6 % PAE, which is currently constrained by the low signal source power up to −7 dBm.

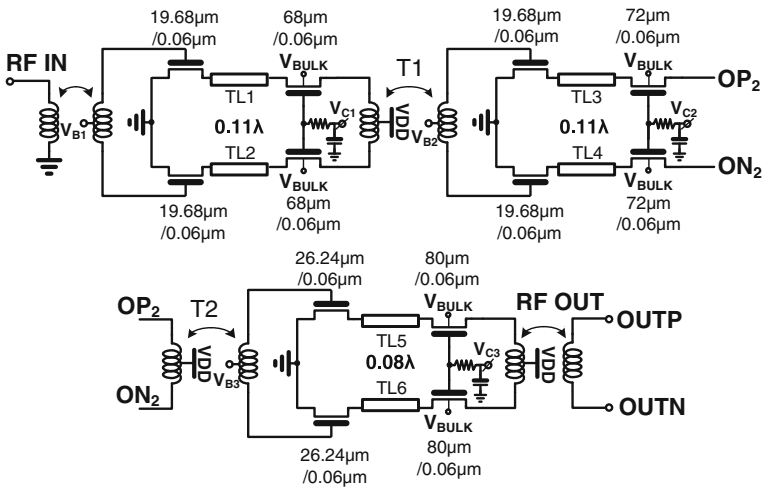


Fig. 3 Schematic of the three-stage 140 GHz LNA

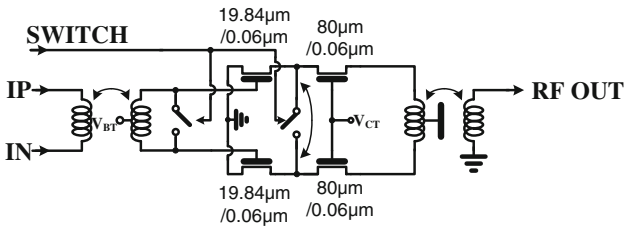


Fig. 4 Schematic of one-stage 140 GHz PA

Also, the measured OP1 dB is about 5 dBm @ 154 GHz. Although the standalone LNA features similar design as the integrated fully differential LNA, there are performance differences due to the different output stages. In standalone LNA, the gain may be lower because it needs to drive 50 ohm external load that has lower impedance compared with the on-chip ED equivalent loading to the integrated LNA. So it is expected that the integrated LNA has a higher gain, where simulation indicates 5 dB more than the standalone LNA.

3.3 GHz power amplifier

PA needs to deliver large output power into antenna to alleviate the tight link budget and accomplish the data modulation in the OOK transmitter. The PA schematic is shown in Fig. 4. Cascode amplifier architecture, similar to the receiver LNA, is adopted to allow high output power with 2 V supply voltage and reliable amplification with excellent stability. Instead of switching the VCO and the buffer on/off, which resists high speed modulation due to the long oscillation startup time, the PA gain can be configured in GHz speed for fast modulation. As shown in Fig. 4, two switches are inserted in front of the PA and between the amplification and cascode devices. When they are open, the PA works in amplification mode (ON) and delivers power to the antenna; when they are closed, the PA shorts differentially and only tiny power is leaked out. Therefore, the 140 GHz modulated signal, as shown in Fig. 1, can be formed. Because the OOK modulation works in saturation mode, the PA linearity requirement can be greatly relaxed. The transmitter delivers > 4 dBm saturated Pout at 140 GHz by simulation.

3.4 D-band vco and injection locking pre-drive

Deep scaled CMOS technology has boosted device speed and 65 nm digital CMOS achieves about 200 and 250 GHz f_T and f_{MAX}, respectively. However, the substrate loss, gate/source contact resistance, and circuit parasitics still limit the circuit maximum operation frequency. Conventional cross-coupled VCO hardly achieves oscillation near its intrinsic cut-off frequencies due to the excessive load introduced by device/interconnect parasitics. We devised a new oscillator architecture by stacking a negative-resistance tank atop the traditional resonant tank to boost the fundamental oscillation frequency. The detailed circuit operation mechanism can be found in [8]. The measurement results demonstrated 131–141 GHz oscillation, which are slightly lower than simulated ones and might be introduced by ineffective switch capacitors/varactors modeling and passive components characterization inaccuracy in D-band.

It is undesirable to use VCO directly drive the power amplifier due to tuning range and pulling concerns, which necessitates a pre-driver serving as buffer to isolate the VCO core from the high output power PA that reduces the capacitance load and mitigates the kick back noise. Figure 5(a) shows a differential cascode amplifier that is often used to buffer the high frequency signal and isolate the VCO. The cascode stage is inserted to alleviate the capacitance load and improve isolation by mitigating the miller effect. However, it requires large power consumption to support desired signal strength in mm-wave frequency and presents significant load to the VCO. To mitigate such effect, an injection locking buffer is proposed as shown in Fig. 5(b). Different from the traditional direct buffer, it adopts negative impedance formed by a cross-coupled pair to boost the tank Q and signal strength. When the negative impedance is relative small and not enough to offset the tank real impedance, it serves as Q booster and enhances the equivalent tank resistance to allow a smaller amplification stage device size with lower power consumption; when the negative impedance is large enough to offset the tank real resistance, it assembles into an oscillator together with the tank load, and can be injection locked to the desired frequency.

Assuming the tank is formed by parallel L, C and Rp, and the conventional differential buffer's gain G can be expressed as Eq. (2). The output signal amplitude V_{amp} is determined by the bias current and tank impedance product. Both follow the tank impedance profile.

$$G = \sqrt{\frac{2I_{Bias}W_{amp}C_{ox}\mu}{L_{amp}}}\frac{j\omega R_p L}{R_p - \omega^2 R_p LC + j\omega L}$$
$$V_{amp} = \frac{I_{Bias}}{2}\frac{j\omega R_p L}{R_p - \omega^2 R_p LC + j\omega L} \quad (2)$$

where I_{Bias} is the amplifier bias current.

When the Q booster is inserted as Fig. 5(b), it generates negative impedance $-\sqrt{\frac{L_{neg}}{2I_{neg}W_{neg}C_{ox}\mu}}$, which offsets the tank resistance loss and enhances its impedance. When $\sqrt{\frac{L_{neg}}{2I_{neg}W_{neg}C_{ox}\mu}}$ larger than tank impedance, the LC tank achieves a higher Q. To achieve identical peak amplitude

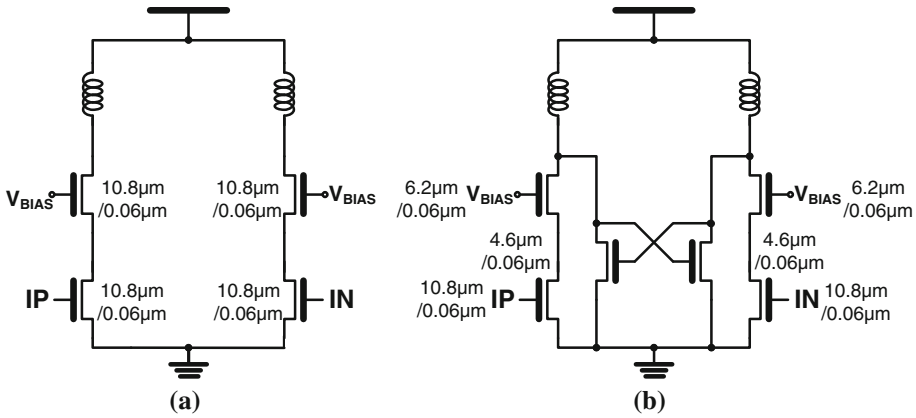


Fig. 5 Schematic of (**a**) traditional differential cascode amplifier (**b**) injection locking pre-driver utilized in this work

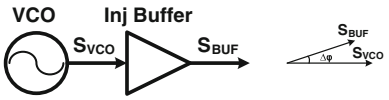


Fig. 6 Injection locking with different center frequencies between the VCO and the injection locking buffer

and gain, the bias current can be reduced, and the amplification NMOS channel width can also be reduced, so as the equivalent loading capacitance to the VCO.

When the generated negative impedance overly compensates the tank resistance, the tank evolves into an oscillator. If its self-oscillation frequency ω_0 is close to the VCO's, it can be injection locked and serve as a high frequency buffer with large output voltage swing. The buffer working range can be defined by the injection locking range and expressed by.

$$\Delta\omega_m = 2 \times \frac{\omega_0}{Q_{tank}} \sqrt{\frac{P_{inj}}{P_0}} = \frac{\omega_0 \mathrm{I}_{inj}}{Q_{tank} \mathrm{I}_{neg}} \tag{3}$$

where Q_{tank} refers to the passive LC tank quality and equals to $R_p/\omega L$, I_{neg} is the cross-couple negative impedance generation stage bias current, I_{inj} stands for inject signal strength that is determined by $\sqrt{\frac{2I_{Bias}W_{amp}C_{ox}\mu}{L_{amp}}}V_{vco}$. Since the V_{vco} is large enough to drive the injection device fully on/off, the I_{inj} can be simplified as injection stage bias current I_{Bias}. Thus the injection locking range is determined by the bias current ratio between injection stage and the negative impedance generation stage. So the injection stage can use a small transistor with a large injection voltage signal to generate given injection current, which further reduces the capacitance load to the VCO.

When there is frequency difference between the VCO and the injection locking buffer self-oscillation, as shown in Fig. 6, it induces a phase discrepancy between their outputs as

$$\Delta\varphi = sin^{-1}(2 \times \frac{\omega_{vco} - \omega_0}{\Delta\omega_m}) \tag{4}$$

And the final output amplitude is the vector summary of the injection signal and self-oscillation signal, which can be expressed as Eq. (5).

$$V_{out} = \sqrt{\frac{(i_{Bias}^2 + i_{neg}^2 + 2i_{Bias}i_{neg}Cos(\Delta\phi))}{1 + Q^2(1 - \frac{\omega^2}{\omega_0^2})^2}} \times R_p \tag{5}$$

It suggests the injection locking buffer output amplitude might not be same as the tank impedance profile. Figure 7 presents the predicted conventional differential buffer and injection locking buffer amplitude profiles based upon Eqs. (2) and (5) analytically as well as the simulated results. The injection locking buffer demonstrates narrower bandwidth, which is not an issue as long as it covers VCO frequency range. And its input stage transistor size can be one-third of its conventional differential buffer counterpart, which saves significant capacitance loading for the VCO to increase the tank inductance so as to improve phase noise performance and save current consumption.

To ensure the pre-driver proper functionalities, digital switch capacitor bank is incorporated into the proposed injection locking buffer as well to increase the effective injection locking range, which should cover the VCO tuning range by more than ±12 %. Because the buffer is injection locked, it introduces negligible phase noise performance degradation.

3.5 Envelope detector and programmable gain amplifier

ED is often used in control and energy estimation systems to assess the signal strength at either the RF input or power amplifier output. It is designed to process low frequency envelop signal by using an op-amp based feedback loop. Conventional opamp based feedback ED suffers from a low operation speed mainly due to the limited gain bandwidth

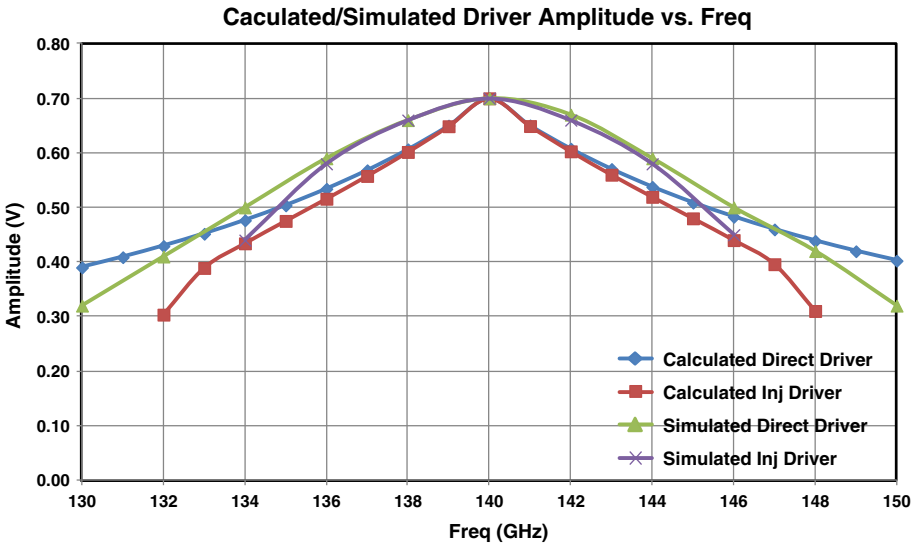


Fig. 7 Calculated and simulated conventional buffer and injection locking buffer amplitude profile

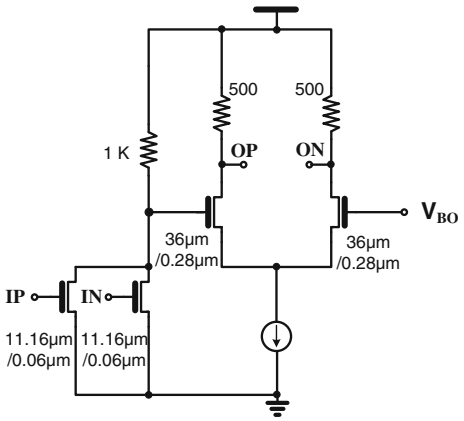


Fig. 8 Envelope detector schematic

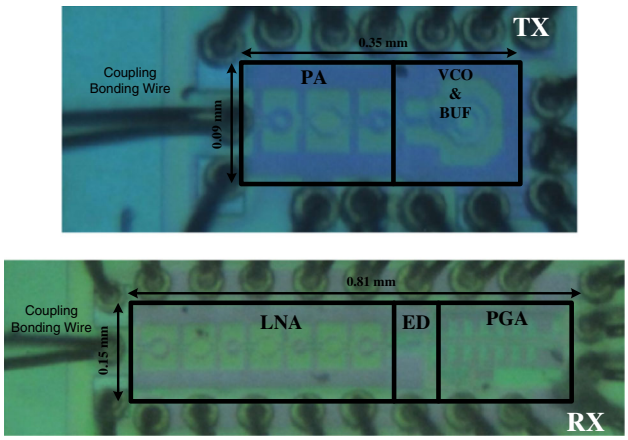


Fig. 9 TX and RX die photos in 65 nm CMOS

of the opamp. Open loop trans-impedance amplifier based ED increases the operating speed to several hundred MHz. Gyrator-C active inductor has further been incorporated in the OTA to compensate the transfer function with a zero and boost the ED bandwidth up to GHz. However, it still cannot satisfy the desired ultra-high speed data link with multi-giga-bit/sec incoming data at D-band carrier frequency.

Figure 8 sketches the implemented high speed ED circuit based upon differential amplifier configuration: two input NMOSs extract the signal envelope from its D-band carrier, which is then amplified and filtered out. The input devices are with feature channel length and biased as a class-B amplifier so that the incoming differential signals with carrier frequency can be rectified to preserve the signal envelope in high speed. The subsequent baseband differential amplifier amplifies the demodulated signal envelope and improves the circuit's power supply rejection ratio (PSRR), whose reference bias VBO adaptively follows the input bias through a passive low-pass filter.

To further amplify the output data and render a large RX dynamic range, a seven-stage PGA with 42 dB gain range, 6 dB gain step is incorporated in the RX chain together with a DC offset cancellation loop with 1 MHz cancellation corner.

4 Measurement results

The intended 140 GHz TX/RX are fabricated in 65 nm CMOS. Figure 9 shows their respective chip photos, whose cores occupy 0.35×0.09 mm^2 and 0.81×0.15 mm^2 chip area, respectively. A 2 V supply is used for the LNA, VCO and PA, and a 1 V supply is for the ED and PGA. To validate the TX function, a data "1" is set as the input signal therefore the PA is fully operating and delivering a CW tone at the carrier frequency 140.3 GHz. When a pseudo random data sequence is then sent to the TX, a spread spectrum should be observed, which, however,

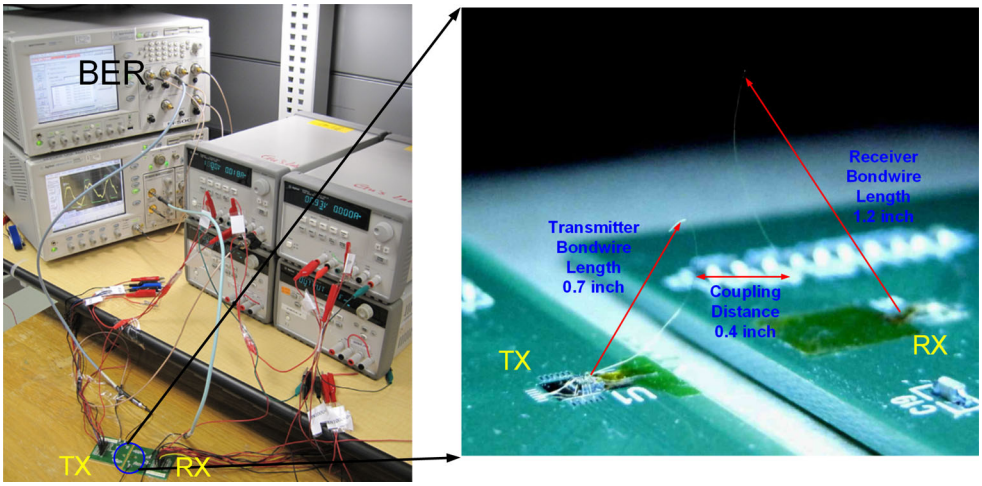
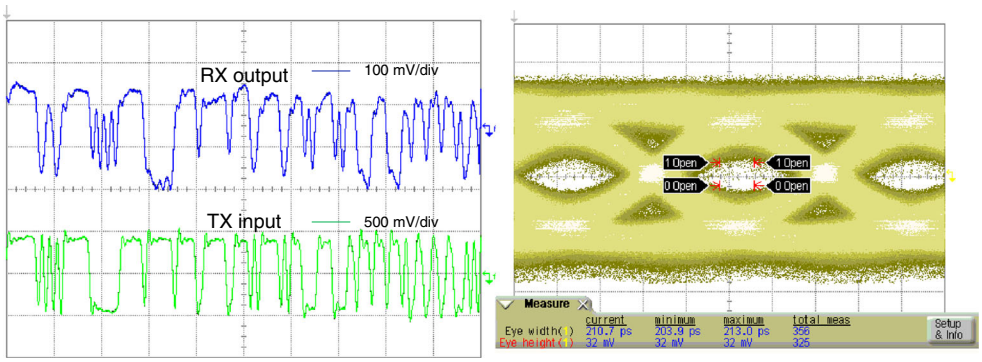


Fig. 10 Measurement setup and coupling antenna using bonding wires



(a) **(b)**

Fig. 11 **a** Measured RX output and TX input with 215-1 PRBS at 2.5 GHz, and **b** output eye diagram

Table 1 D-band data link performance summary

Technology	1P6 M 65 nm CMOS
Chip area	TX: 0.03 mm^2; RX:0.12 mm^2
Power consumption	TX: 115 mW; RX:120 mW
Carrier frequency	140 GHz
Data link speed	2.5 Gbps
BER	4.1×10^{-6}
Energy efficiency	94 pJ/bit

cannot be easily identified from the high noise floor due to the significant loss of the measurement setup.

To characterize the data link, the TX and RX chips are placed in close proximity ($\sim$1 cm) and coupled with bond wire, as shown in Fig. 10. Figure 11(a) presents both input and output signal waveforms with the data rate of 2.5 Gbps of 2^{15}-1 PRBS pattern with the output signal eye diagram shown in Fig. 11(b). A measured 4.1×10^{-6} bit error rate (BER) is achieved with 1 cm distance. Currently, the communication quality is mainly limited by the low transmitter output power, and the data rate is limited by the 1.2 GHz RX baseband bandwidth. Table 1 summarizes the TX/RX data link performance.

5 Conclusion

A 2.5 Gbps data link at D-band between independently integrated TX and RX made of 65 nm CMOS is successfully demonstrated. The TX/RX only occupies 0.03/0.12 mm^2 die area and burns 115 mW/120 mW, respectively. This successful demonstration of D-band wireless link in CMOS technologies clears the way for implementing short-distance (<10 cm) and ultra-high-speed data communications between board-to-board, board-to-backplane and chip-to-chip for space and cost constrained computer, communication and consumer electronics systems.

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Heterojunction Bipolar Transistor (HBT) and *BiFET* (Planar HBT/MESFET) integrated circuit technologies from the research laboratory to the production line (now Conexant Systems and Skyworks). The *HBT/BiFET* productions have grown into multi-billion dollar businesses and dominated the cell phone power amplifiers and front-end module markets (currently exceeding one billion units/year). Throughout his career, his research has primarily focused on the development of high-speed semiconductor devices and integrated circuits for RF and mixed-signal communication and sensing system applications. He was the principal investigator at Rockwell in leading DARPA's ultra-high speed *ADC/DAC* development for direct conversion transceiver (*DCT*) and digital radar receivers (*DRR*) systems. He was the inventor of the multiband, reconfigurable *RF-Interconnects*, based on FDMA and CDMA multiple access algorithms, for *ChipMulti-Processor* (CMP) inter-core communications and inter-chip *CPU-to-Memory* communications. He also pioneered the development of world's first multi-gigabit/sec *ADC, DAC* and *DDS* in both *GaAs HBTs* and *Si CMOS* technologies; the first 60 GHz radio transceiver front-end based on *transformer-folded-cascode* (*Origami*) high-linearity circuit topology; and the low phase noise CMOS VCO (FOM < -200 dBc/Hz) with Digitally Controlled on-chip Artificial Dielectric (*DiCAD*). He was also the first to demonstrate CMOS oscillators in the Terahertz frequency range (324 *GHz*). He was also the founder of an RF design company G-Plus (now SST Communications) to commercialize WiFi 11b/g/a/n power amplifiers, front-end modules and CMOS transceivers. Dr. Chang has authored or co-authored over 270 technical papers, 10 book chapters, authored 1 book, edited 1 book and holds >20 U.S. patents. He was a co-editor of the *IEEE Transactions on Electron Devices* (1999–2001) and served as the Guest Editor for the IEEE *Journal of Solid-State Circuits* in 1991 and 1992, and for the Journal of High-Speed Electronics and Systems in 1994.