Recent Development Progress of an X-Band High Efficiency Transmitter Using Class E PA and Split-Band Supply Modulation

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Abstract: A 10GHz high efficiency transmitter with wideband supply modulation is developed under the DARPA MPC program. The technology is implemented for envelop restoring modulation by integrating a contour modulated class E PA and a split-band power supply. This method allows for a wide modulation envelope bandwidth without significant efficiency penalty.

Keywords: AlGaN/GaN, transmitter, class E amplifier, supply modulator, phase modulator, contour modulation, CMOS, pulse width modulation, X-band

Introduction

The majority of RF transmitters suitable for power levels and signal bandwidths of interest for defense applications share common system architectures for power conversion, where the final stage of power conversion forming the DC supply to the semiconductor PA uses large, fixed-voltage power converters of mature design. This system constraint fundamentally limits RF system choices for amplifier operation class, output power, power added efficiency and is a barrier to higher levels of system integration. Typically an RF PA achieves peak power efficiency at a single operating voltage corresponding to peak output power. However, many RF systems employ complex modulation techniques with high peak-to-average ratios in signal amplitude. Although the systems are designed for fixed operation at the peak condition, the PAs operate well below peak output power much of the time. At a fixed operating voltage, PA efficiency drops rapidly as the output power is reduced from its peak value by either lower input drive or wasteful attenuation, resulting in low average conversion efficiency of DC power to useful RF signals.

Northrop Grumman Systems Corporation (NGSC) teamed with UCLA under the DARPA Microscale Power Conversion (MPC) program has developed a method to implement envelope restoring modulation, using both contour modulation of a power amplifier and a split-band power supply, integrated with a high efficiency class E amplifier to meet the performance target \geq 75% PAE. This method allows for a wide modulation envelope bandwidth without significant efficiency penalty. As in contour modulation by definition, a switching RF amplifier can be backed off in power by at least 6dB and up to 13dB as previously demonstrated by UCLA researchers [1,2]. This has been accomplished with-

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out an efficiency penalty by adjusting the duty cycle of the input RF waveform, and pulling the output impedance with switched reactive networks. Supply modulation is used in conjunction with contour modulation to minimize the excursions in duty cycle and load pull which contour modulation entails, and to extend back-off range. A comprehensive sub-banded modulation scheme results from dividing the supply modulator into a lower frequency and mid-band portion, and using the contour modulation of the PA for the highest frequency portion of the modulation envelope. This combined contour and supply modulation technique is applied to an X-band GaN-based class E amplifier.

This paper provides an overview of the technology development to date, system architecture and implementation, and supply modulator prototypes for concept demonstration, as well as some measured performance of GaN MMICs and CMOS ASICs obtained. Additional up-to-date results will be presented at the conference.

System Implementation

A simplified block diagram of the transmitter architecture is shown in Figure 1, which consists of five key system blocks including a 10GHz class E HPA, a supply modulator consisting of a low-frequency buck converter and a mid-band bi-directional converter, CMOS phase modulators, a pulse width modulated waveform driver, and a control block implemented into a FPGA. The system diagram shown in the figure is color coded to distinguish GaN and CMOS parts of the solution. The proposed system is a split-band combination of a supply modulator and a new "contour modulated" class-E PA. The supply modulator tracks 0-100 MHz envelope content whereas the envelope



>100 MHz is imposed on the PA output by the "contour modulated" class-E PA.

The system architecture offers several benefits. First, the contour modulation maintains class-E PA efficiency over significant power back-off. As it imposes the 100-500 MHz envelope on the output, the class-E PA maintains its inherently high efficiency. Second, the sub-banded supply modulator needs to track only 0-100 MHz envelope content where the 0-1 MHz band high efficiency buck converter handles >85% of total power, and thus high supply modulator efficiency can be achieved. Lastly, the mostly digital architecture allows sophisticated digital calibration and predistortion to enable excellent linearity.

The contour modulation realizes wide band envelope variations using a combination of open-loop duty cycle and load network switching on a GaN class-E PA. It ensures that the PA efficiency remains high while tracking envelope variations. The load network switching is achieved using switchable capacitor banks; appropriate control signals are generated based on the desired envelope digital signal and a lookup table (LUT). The phase content of the modulation is introduced into the 10 GHz PA drive using phase modulators up to 2 GHz phase switching. Two phase modulators are used and their outputs combined in the GaN MMIC driver to realize open loop duty cycle control. The phase modulators and a 10 GHz LO generator are implemented in the 65nm CMOS technology.

The 0-100 MHz supply modulator is itself sub-banded: a high efficiency buck converter tracks 0-1 MHz envelope content whereas an open loop bidirectional class-E rectified DC:DC converter tracks the 1-100 MHz envelope content in which its variations are realized by dynamically changing the duty cycle of the 1 GHz drive open loop. The load network may also be dynamically changed as in the contour modulated 10 GHz PA to minimize efficiency degradation at low DC:DC output levels. All necessary control signals are generated in the CMOS ASICs.

Figure 2 shows the power measurement of a "static" 10W, X-band class E PA from the first generation GaN MMIC fabricated at NGSC Advanced Technology Laboratory. This PA does not have contour modulation and is the base-



Figure 2 Measured Power Output And Power-Added Efficiency of a "Static" 10W X-Band Power

line design with a conventional input matching network and a fixed output matching network. Figure 3 plots the optimal power-added efficiency (PAE) and power output vs. drain voltage for three different control arrangements: (1) varying drain voltage only with a fixed gate voltage of -1.75V and Pin=31dBm, (2) varying drain voltage and input power with the gate voltage fixed at -1.75V, and (3) varying drain and gate voltage and input power. The data shows that PAE can be maintained between 55-60% range over a 6dB power back-off from 34 dBm to 40 dBm.



Figure 3 Measured Power-Added Efficiency (PAE) and Output Power (Pout) vs. Drain Voltage for Three Control Cases

A 10W, X-band contour modulated PA MMIC was also designed and fabricated, which has an input PWM driver circuit to provide pulse-width modulated waveforms to the class E GaN FET and a contour modulated output impedance network with a 2-bit capacitance bank which provides four different states of output impedance. The chip also includes a level shifter circuit to translate CMOS compatible control signals to the voltage levels required by the GaN FET switches. Figure 4 shows the photo of the MMIC.



Figure 4 Photo of a Fabricated Contour GaN HPA. This is a Nominal 10W X-Band Design with 2-Bit Contour Modulation Control of the Output Net-

Measurements were performed using an Agilent PNA-X with dual signal sources and phase control option which

allows the relative phase of the two input signal to be controlled with high precision. The complete measurement setup with up-to-date results will be reported at the conference.

Two versions of the buck GaN MMIC were designed. One version relies on an external driver for the upper buck switch, and the other has internal CMOS compatible level shifts. Figure 5 shows the buck MMIC photo and its circuit without the input CMOS level shifter. Performance for quick demonstration was measured on a test fixture in open loop with an Agilent 8110 programmable pulse generator as the signal source. The switches run in tandem to provide 2x frequency bandwidth with negative voltage sent directly to the buck's lower switch from the pulse generator and a positive logic level signal to an IL710 isolator to drive the upper switch. Switch timing was adjusted to allow 5ns dead-time between upper and lower switches. A peak efficiency of 91.5% was observed.

For the mid-band portion of the supply modulator, two bidirectional supply modulator prototypes at 1.6MHz and 10MHz using off-the-shelf components were constructed to demonstrate the concept. Figure 6 shows the simulated and measured performance of the modulator for a fixed frequency and duty cycle control method with no dynamic contour modulation. The green waveform is the voltage modulation at the load, while the yellow and purple waveforms are the voltages across the FETs that make up the bidirectional converter. A more rigorous control method is in development to accurately predict hardware performance and dynamically operate the converter along its zerovoltage-switching contour. The bi-directional converter prototype implemented in MMICs for higher switching and its characterization will be reported at [3].



Figure 5 (A) Buck MMIC Photo, and (B) Buck Circuit with High Side and Low Side Switches



Figure 6 (A) Simulated, and (B) Measured Performance of the 1.6MHz Bi-Directional Modulator Prototype for a Fixed Frequency and Duty Cycle Control Method with No Dynamic Contour Modulation

A wide bandwidth digitally controlled open-loop phase modulator in 65 nm CMOS process was developed to achieve data bandwidth up to 500 MHz and phase switching frequency up to 2 GHz at 10 GHz carrier frequency [4]. The architecture utilized a combination of 6-bit and 9-bit phase interpolators buffered with phase/amplitude error compensation controls to provide phase modulated waveforms with 12 bits resolution. This modulator is anticipated to consume only 140 mA at a 1 V supply. Two of the 12bit phase modulators are arranged in ping-pong style as each operates at half of the phase switching frequency and has data synchronized at 10 GHz, which is half of the input clock frequency.

The initial measurement of the 10GHz CMOS PLL, shown in Figure 7, shows that it exhibits a phase noise performance of -103dBc/Hz at 1MHz offset from the carrier frequency and tuning range of 20% centered at 10 GHz. A more thorough study of its performance is still under development, and its results along with that of the phase modulators will be reported at the conference.



Figure 7 The Initial Measurement of the Phase Noise Performance of The 10 GHz PLL, -103dBc/Hz @1MHz Offset.

Conclusion

The recent development progress of a high efficiency digital RF transmitter is reported. The transmitter system employs NGSC's 10W X-band class E power amplifier technology in 0.1µm AlGaN/GaN HEMT process in conjunction with contour modulation of the power amplifier and a sub-banded switching supply modulator to target wide modulation envelope bandwidth. The RF amplifier can be backed off in power by more than 6dB without a significant efficiency penalty. The contour modulated control implemented in 65nm CMOS technology uses dynamic, open loop, digital control of both class-E PA drive duty cycle and load network to enable ultra-wide bandwidth envelope variation while simultaneously maintaining optimal PA efficiency.

This highly integrated supply/transmitter technology will provide a new capability for the efficient operation of RF systems and is particularly useful for power limited/space constrained communication, surveillance, radar, and cognitive radio systems.

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