A 10 GHz 2 Gb/s Open-Loop Phase Modulator

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Abstract: *Wide bandwidth open-loop phase modulator architecture is proposed and two 12-bit modulators are designed for bandwidth of 500 and 150 MHz and data rate of 2.0 and 0.3GHz at 10 and 2.5GHz carrier frequencies in 65nm CMOS process. Simulated DNL is between +0.55 and -0.15 and ENOB is 9-bit.*

Keywords: wide bandwidth, open-loop phase modulation, phase interpolator, phase interpolation, high resolution.

Introduction

Wide bandwidth phase modulators are essential in high efficiency polar/out-phasing transmitters because phase modulators need to cover approximately ten times wider bandwidth than the channel bandwidth [1]-[3]. Also, digital phase control architecture is preferable because it provides convenient ways to control delay mismatch between phase and amplitude modulation path and for digital AM-PM pre-distortion.

Fig. 1 shows a conventional architecture of open-loop phase modulator. The open-loop phase modulator consists of phase generator (and/or selector) and digital control logic. The phase generator/selector receives a clean signal at the carrier frequency from phase-locked loop (PLL), and generates multiple sub-phases and selects one of them to make phase modulated output signal under the control of digital logic which decodes transmission data (ϕ[n]) at the clock frequency.

The phase generator and selector is composed of frequency divider and multiplexer in [4], but the output number of phases is limited by four. To overcome the limited phase resolution, delta-sigma modulator (DSM) is used which increases out-of-band noise significantly. Ring oscillator or delay line [5] is also used as multiple phase generation circuit, but they have high phase noise. Thus, they are not suitable for high resolution phase modulators.

Fig. 2 (a) shows the phase interpolator whose output phase is dependent on the current control X [6], where the value of X is between 0 and 1. The output phase ϕ varies from ϕ_1 to ϕ_2 as X increases from 0 to 1 (Fig. 2 (b)). It is suitable for fine phase control and immune to noise due to its fully differential structure.

In this work, a very wide bandwidth, high resolution open-loop phase modulator architecture is proposed based on the phase interpolator in Fig. 2 (a). To verify the proposed architecture, two open-loop phase modulators are designed at 10 and 2.5 GHz carrier frequencies to have 12-bit digital phase control, data bandwidth of 500 and 150 MHz, and phase switching frequency of 2 GHz and 300 MHz, respectively.

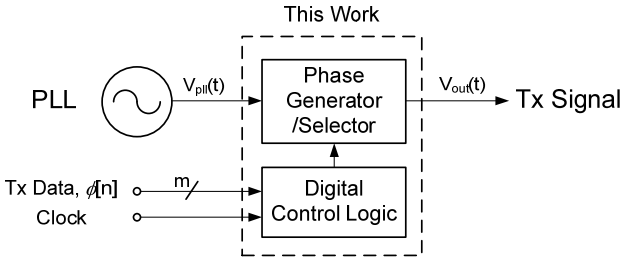

Fig. 1. A conventional open-loop phase modulator.

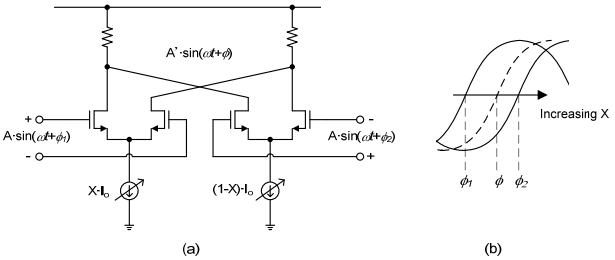

Fig. 2. Phase interpolation based on current summation [6]. (a) Circuit. (b) Conceptual operation.

Architecture and Circuit Design

Output phase linearity of the phase interpolator in Fig. 2 (a) is highly dependent on the input phase difference $\Delta\phi$ (= ϕ_1 - ϕ_2). Fig. 3 compares calculated differential non-linearity (DNL) of output phase when $\Delta\phi$ is 45° and 90°. DNL varies between -0.09 ~ 0.05 and -0.36 ~ 0.27, for 45° and 90°, respectively. In our interpolator design, 45° input phase difference ($\Delta\phi$) is selected because it shows much better linearity. $\Delta\phi$ can be reduced further for better linearity, but it will make the design of multiple phase generator be complex.

The proposed open-loop phase modulators at 10 GHz and 2.5 GHz carrier frequencies are shown in Fig. 4 (a) and (b), respectively. They are composed of octant phase interpolator and sub-octant phase interpolator. The octant phase interpolator generates two differential signals in 45° phase difference, and the sub-octant phase interpolator, composed of phase interpolator in Fig. 5, makes the wanted output phase signal. Each modulator is controlled by the 12-bit phase modulation data: 3-MSBs control octant phase interpolator

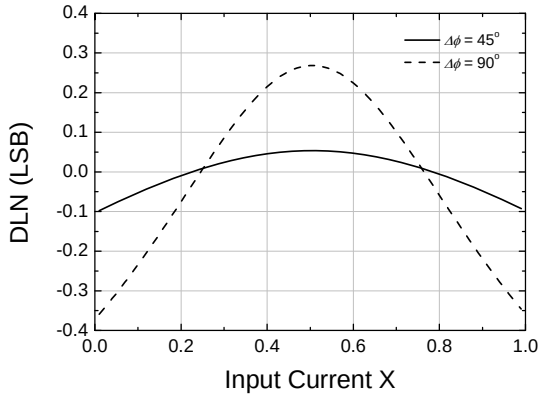

Fig. 3. Phase linearity comparison when $\Delta\phi = 45^{\circ}$ and 90°.

and 9-LSBs control sub-octant phase interpolator. The two phase modulators have 10 GHz quadrature phase input signal generated from 20 GHz PLL frequency synthesizer.

The 10 GHz phase modulator in Fig. 4 (a) has phase/amplitude control buffers at the input to compensate phase/amplitude errors caused by device and layout mismatches. This can compensate the static errors of the 10 GHz input signal and in the phase modulator itself. The octant phase interpolator in Fig. 4 (a) generates 45° phase difference signals from 90° phase signals at the same frequency of 10 GHz. Because the quadrature input does not provide four phases (45°, 135°, 225°, and 315°) among the wanted eight phase, they should be interpolated from the quadrature input.

The phase interpolator in Fig. 2 (a) has amplitude variation at the output by the current control (X in Fig. 2 (a)), and non-linearity increases when amplitude mismatch presents between the two inputs. Thus, the output amplitude mismatch of the octant phase interpolator can degrade phase linearity of 9-bit sub-octant phase interpolator. To get high linearity, the four phase-switching multiplexers, 6-bit leading/lagging phase interpolators, and decoder generate amplitude balanced 45° phase difference signals.

The four multiplexers are grouped into two parts. Each part selects 90° phase difference signals for 6-bit leading/lagging phase interpolators. The two 6-bit interpolators generate new phases to have 45° phase difference between their outputs. If the binary input code is 000, for example, the leading phase interpolator receives 270° and 0° signals and lagging phase interpolator receives 0° and 90° signals. Then, the current controls (X) of the leading and lagging phase interpolators are set to 1/4 and 3/4, which is complementary. Now, the output phases of leading and lagging phase interpolators are 337.5° and 22.5°. Because the amount of current weighting is same in the two 6-bit interpolators but in opposite direction, this control ensures the same amplitude at the output. In this manner, the octant phase interpolator generates two

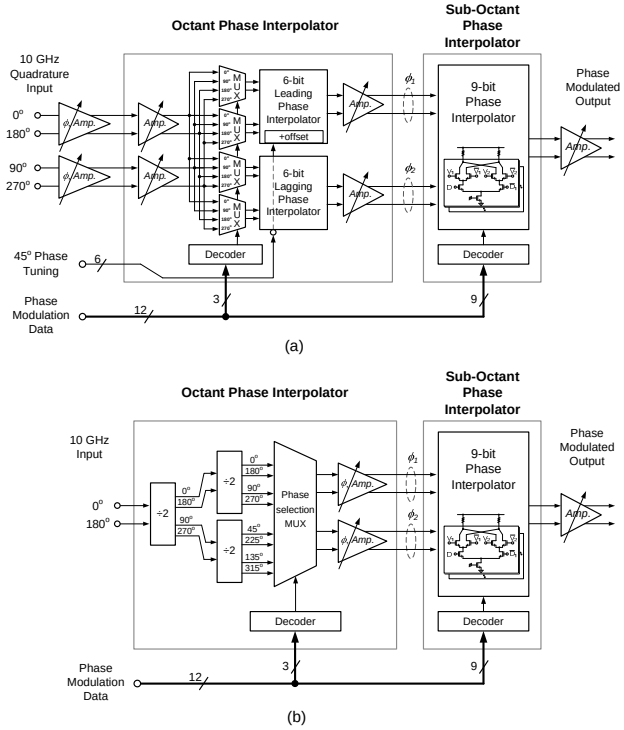

Fig. 4. Proposed 12-bit open-loop phase modulator architectures. (a) 10 GHz, 2 Gb/s phase modulator. (b) 2.5 GHz, 300 Mbps phase modulator.

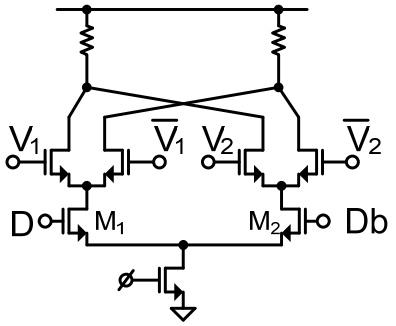

Fig. 5. Interpolator unit circuit in 9-bit sub-octant phase interpolator.

differential pair signals at 22.5°, 67.5°, 112.5°, 157.5°, 202.5°, 247.5°, 292.5°, and 337.5° phases with 45° phase difference. The octant phase interpolator also includes amplitude control buffers to optimize its performance.

Fig. 4 (b) shows 2.5 GHz phase modulator. The octant phase can be easily generated by dividing 10 GHz quadrature input by two-stage CML dividers. The multiplexer selects two differential signals in 45° phase difference to provide input of 9-bit sub-octant interpolator. The phase/amplitude control buffers at the final stage of octant phase interpolator can compensate phase/amplitude errors.

Fig. 5 shows the unit interpolator circuit in 9-bit sub-octant

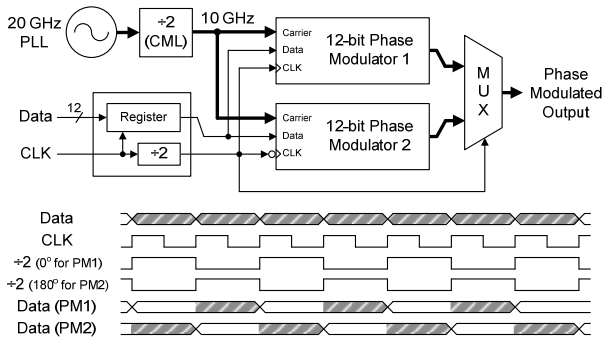

Fig. 6. Ping-pong architecture of the proposed phase modulator and its timing diagram.

phase interpolator. It has additional input D compared to the conventional interpolator in Fig. 2 (a). To realize phase modulator, the current weight X should be updated at the clock frequency, and MOS switch is usually used to steer current. In our design, NMOS switches M_1 and M_2 are used to receive digital data. The shared source of the two NMOS switches (M_1 and M_2) can improve the speed of current switching because this phase interpolator does not turn-off the current mirror.

Any phase interpolator has finite settling time, and it may cause non-linear phase transition at the output. Ping-pong architecture can resolve this issue when each modulator operates at the half of the phase switching frequency. Fig. 6 shows the ping-pong architecture used. There are two identical 12-bit phase modulators, a multiplexer at the output, a data register clocked at the phase switching frequency (2 GHz), and a divid-by-2 to generate half of the phase switching frequency (1 GHz). The timing diagram at the bottom shows input data, clock, lower frequency clocks which are in complementary, and retimed data for each phase modulators. In the first half clock period of each phase modulator, data is updated (blank region) and phase changes to wanted value. The multiplexer selects this settled signal in the succeeding half clock period (shaded region). In such a way, phase transition becomes smooth and settling issue is resolved. This ping-pong architecture is only used in 10 GHz phase modulator because 2.5 GHz phase modulator has sufficient settling time at the 300 MHz phase switching frequency.

Simulation Results

The phase modulators are designed in 65 nm RF CMOS process. 10 GHz phase modulator dissipates 140 mA from a 1.0 V supply. Fig. 7 (a) is simulated differential non-linearity (DNL) result. DNL is between +0.55 and -0.15 when 1 LSB is 24.4 fs. Because phase linearity characteristic is periodic by 90°, DNL for the first 90° phase range is shown only range (from 0 to 1023 of control code). Fig. 7 (b) is the simulated integrated jitter performance over 10 kHz to 1 GHz

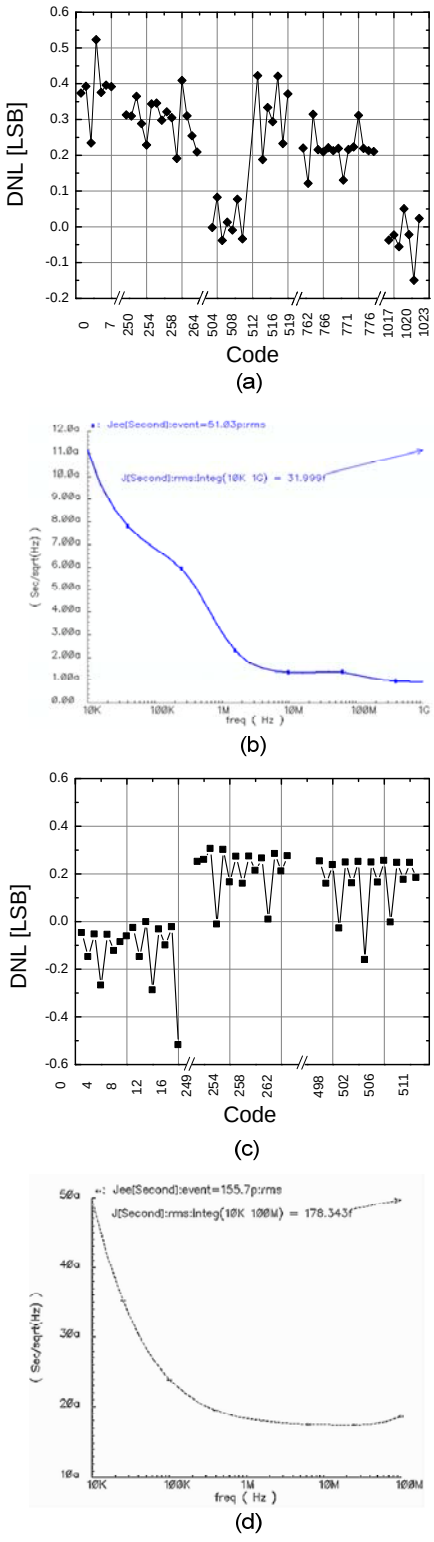

Fig. 7. Phase modulator simulation results. (a) DNL results. (b) Integrated jitter performance from 10 KHz to 1 GHz.

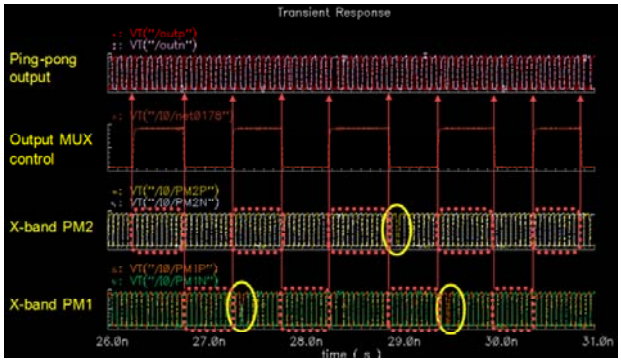

Fig. 8. Time domain output waveform of the ping-pong phase modulator.

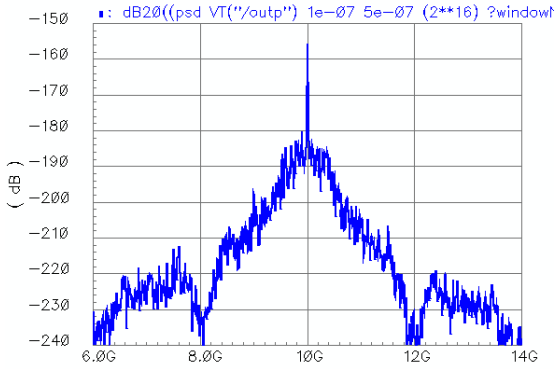

Fig. 9. Power spectral density of output signal at 10 GHz.

bandwidth at 10 GHz carrier frequency. The integrated jitter is 32 fs,rms (-57 dBc) which is over 9-bit ENOB.

2.5 GHz phase modulator consumes 14 mA from 1.0 V supply. Its DNL is in between -0.55 and 0.32 when 1 LSB is 167 fs. The DNL of this 2.5 GHz phase interpolator is periodic by 45°, so the corresponding phase range (from 0 to 511 of control code) is shown in Fig. 7 (c). The integrated jitter is 178 fs,rms (-54 dBc) which is 8.7-bit ENOB. Fig. 8 is time domain output waveform of the ping-pong phase modulator. The three ellipses denote non-linear phase transition at the each 12-bit phase modulator. The output multiplexer control signal selects settled output from one of the two phase modulators. Therefore, the ping-pong output shows smooth transition of phase. Fig. 9 is the power spectral density of output signal with a data bandwidth of 500 MHz and a phase switching frequency of 2 GHz. Fig. 10 shows chip layout. The area consumption for 10 GHz and 2.5 GHz phase modulators are 1.2 mm^2 and 0.9 mm^2, respectively.

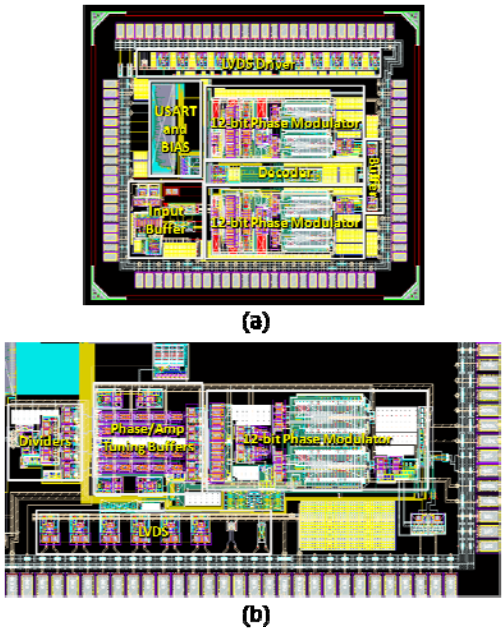

Fig. 9. Chip micrograph. (a) 10 GHz phase modulator. (b) 2.5 GHz phase modulator.

References

1. J. Zhuang, K. Waheed, and R. B. Staszewski, “A technique to reduce phase/frequency modulation bandwidth in a polar RF transmitter,” *IEEE Trans. Circuits Syst. I*, vol. 57, no. 8, pp. 2196–2207, Aug. 2010.
2. P. Su and S. Pamarti, “A 2.4 GHz Wideband Open-Loop GFSK Transmitter With Phase Quantization Noise Cancellation,” *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 615-626, Mar. 2011.
3. G. Marzin, S. Levantino, C. Samori, and A. Lacaita. “A 20Mb/s Phase Modulator Based on a 3.6GHz Digital PLL with -36dB EVM at 5mW Power.” *ISSCC Dig. Tech. Papers*, pp. 342-343, Feb. 2012.
4. Y.-H. Liu and T.-H. Lin, “A wideband PLL-based G/FSK transmitter in 0.18 μm CMOS,” *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2452–2462, Sep. 2009.
5. P. K. Hanumolu, V. K. Kratyuk, G.-Y. Wei, and U.-K. Moon, “A Sub-Picosecond Resolution 0.5-1.5 GHz Digital-to-Phase Converter,” *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 414–424, Feb. 2008.
6. S. Sidiropoulos and Mark. A. Horowitz, “A Semidigital Dual Delay-Locked Loop,” *IEEE J. Solid-State Circuits*, vol. 32, no. 11, pp. 1683–1692, Nov. 1997.