

# W-Band Transmitter with Injection Locking Frequency Multiplier based Phase Shifter for Large Phase Array Systems

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**Abstract:** This paper presents a new W-band transmitter with the proposed injection locking frequency multiplier based phase shifter to enable a low frequency local oscillator (LO) distribution. This scheme eliminates sophisticated high frequency phase shifters and LO distribution networks to reduce system design complexity and power consumption, and more importantly, offers great array scalability.

**Keywords:** Array system; frequency multiplier; injection locking scheme; LO distribution network; phase shifter; transmitter.

## Introduction

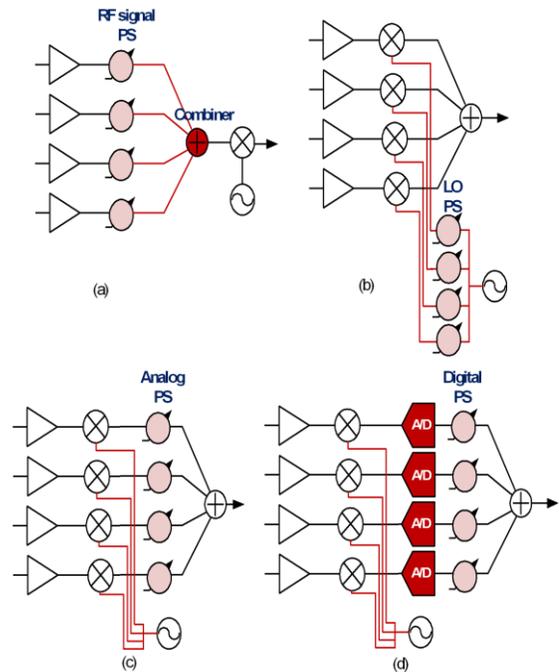
Silicon millimeter wave and sub-millimeter wave system-on-a-chip has drawn substantial interests due to their high potentials in various applications [1, 2]. However, existing silicon devices encounter big challenges to design high output power transmitter ( $>30$  dBm) and low noise receiver (noise figure  $< 4$  dB). To overcome these constraints, phase array systems are a viable solution to alleviate transmitter output power and receiver noise figure requirements for each element. In phase array systems, the LO distribution network and phase shifter are the two critical and challenging components, especially for high frequency operations, such as in the range of mm-wave/sub-mm wave frequencies.

To overcome the aforementioned issues in mm-wave/sub-mm wave systems, we propose an injection locking frequency multiplier based phase shifter (ILFM\_PS) to permit a low frequency LO distribution network. The advantages of this method include the elimination of power hungry high frequency phase shifters, and the high efficiency and strong drivability of low frequency LO distribution. In addition, low frequency LO distribution enables good scalability for a large array size. By integrating this ILFM\_PS, we present a single element W-band transmitter with a simulated power consumption of 170 mW and a chip area of  $950 \times 750 \text{ um}^2$ .

## Conventional Phase Array Architectures

There are mainly four typical phase array architectures based on different phase shifter schemes: RF signal phase shifter, LO phase shifter, analog baseband phase shifter and digital baseband phase shifter [3, 4], as shown in Figure 1. Each scheme has its own pros and cons. (1) A RF signal phase shifter occurs along the signal path, which saves the design effort on high frequency LO distribution. However, it requires a challenging wide-band phase shifting operation for RF input signal and high frequency signal combination from all the elements before mixing with LO. (2) A LO phase shifter utilizes LO phase adjustment to compensate the RF signal path time delay,

which has the advantage of narrow bandwidth operation, however, at the cost of very challenging high frequency LO distribution with programmable phases. (3) An analog baseband signal phase shifter reduces the phase shifter operating frequency to baseband to facilitate the design. However, the challenges are the ultra-wide band phase shifting operation and high frequency LO distribution. (4) A digital baseband phase shifter provides great system flexibility due to the powerful digital signal processing to conduct the phase shifting function. However, the system power and area overhead may be intolerable because each element requires a complete transceiver all the way to ADC/DAC. In addition, this approach is not suitable for high speed systems because ultra-high speed digital signal processing is very challenging in nowadays technologies.

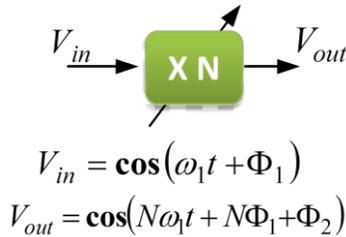


**Figure 1.** Existing phase shifter based array architectures: (a) RF signal phase shifter, (b) LO phase shifter, (c) analog baseband phase shifter, and (d) digital baseband phase shifter with challenging design parts highlighted by red color

Besides the aforementioned drawbacks, one common issue of the existing phase shifting approaches is that all of them are hard to expand or scale. That means once the design is complete, expanding or scaling the array size would require tremendous work or almost redesign the entire system, which is not efficient.

### Proposed ILFM Based Phase Shifter Architecture

To overcome the drawbacks of existing solutions, we propose an injection-locking frequency multiplier based phase shifter (ILFM\_PS) scheme to enable low frequency LO distribution. The concept is shown in Figure 2. By changing input signal phases of a frequency multiplier, the output signal phase will be amplified by the circuit multiplication ratio. It suggests that shifting a small phase value ( $\phi_1$ ) at the low frequency input will lead to a large phase ( $N * \phi_1$ ) shifting at the high frequency output. Therefore, this ILFM\_PS can realize both frequency and phase multiplication and allow a fine phase adjustment at the low frequency input to cover wide phase shifting range at the high frequency output. To boost working frequency and signal drivability, we utilize injection locking approaches in frequency multiplier implementations.



**Figure 2.** The proposed ILFM\_PS working concept

With this ILFM\_PS design idea, low frequency LO,  $f_{LO}/N$ , instead of  $f_{LO}$ , will be distributed to feed each element. Inside each element, the low frequency LO signal will be multiplied to the desired system LO frequency  $f_{LO}$  with the accomplished LO phase shifting function. This ILFM\_PS scheme with low frequency LO distribution will significantly reduce system power consumption and design complexity. More importantly, this scheme enables excellent array scalability. Table I summarizes the comparison between the existing four phase shifter based architectures and the proposed ILFM\_PS based one.

### ILFM\_PS Design

One of the key design issues of the proposed ILFM\_PS is the phase nonlinearity. As presented in Figure 2, the ILFM\_PS output signal phase is determined by two factors:  $\phi_1$  and  $\phi_2$ , where  $\phi_1$  is the input signal phase and

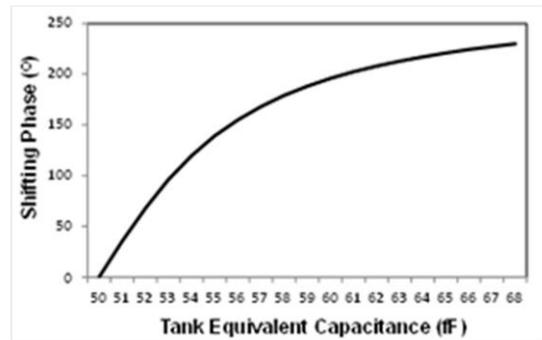
$\phi_2$  is the phase shifting of the current ILFM\_PS stage. Among these two phase parts, input determined part of  $N \times \phi_1$  demonstrates very linear relationship versus input signal phase. However, the phase shifting from the current ILFM\_PS stage,  $\phi_2$ , is highly nonlinear and determined by various resonant tank components. Equation (1) is the equivalent tank parallel impedance with the assumption of a second order LC tank.

$$Z(j\omega) = \frac{R_p}{1 + j\frac{2Q}{\omega_N}(\omega_o - \omega_N)} \quad (1)$$

where  $R_p$  is the tank equivalent parallel impedance,  $Q$  is the tank quality factor,  $\omega_N$  is the tank natural frequency and equals to  $1/\sqrt{LC}$ . The phase shifting due to tank impedance contributes a major part in  $\phi_2$  of Figure 2, therefore represented in Eq. (2) as:

$$\Phi_2 \approx \Phi_{Z(j\omega)} = -\arctan\left(\frac{2Q}{\omega_N}(\omega_o - \omega_N)\right) \quad (2)$$

Equation (2) clearly presents high nonlinearity of the shifting phase versus tank parameters. Figure 3 exemplifies one example of such nonlinearity by plotting shifting phase  $\Phi_2$  versus tank capacitance.

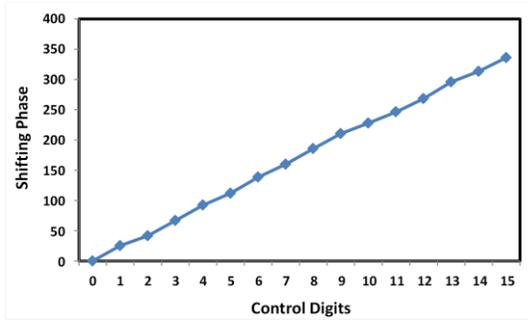


**Figure 3.** Simulated shifting phase versus tank equivalent capacitance presents strong nonlinearity

To improve phase nonlinearity, digital assisted self-healing and calibration is needed. Figure 4 shows the improved phase linearity with digital assisted calibrations, which demonstrates about 3 degree coarse control accuracy

**Table I.** System comparison with existing four phase shifter approach based architectures

	Power	LO Distribution	mm-Wave Design Complexity	Area	Scalable
RF Signal Phase Shifter	High	Easy	High	Medium	Hard
LO Phase Shifter	High	Hard	Medium	Medium	Hard
Analog Baseband Phase Shifter	Medium	Hard	Medium	Small	Hard
Digital Baseband Phase Shifter	Very High	Hard	Medium	Very Large	Hard
Proposed ILFM_Phase Shifter	Low	Medium	Low	Medium	Easy



**Figure 4.** The simulated ILFM\_PS phase shifting after digital calibration demonstrates 3° degree coarse control accuracy with the coverage of 360°

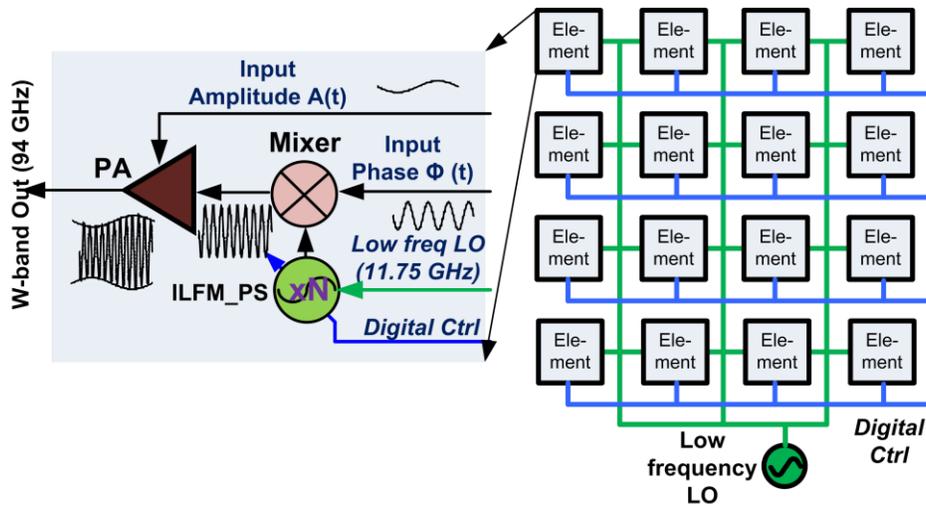
### W-Band Transmitter Element with ILFM\_PS

To verify this injection locking frequency multiplier based phase shifter (ILFM\_PS) concept, we have integrated an ILFM\_PS with a W-band transmitter as one array element, shown in Figure 5. It consists of a W-band power amplifier (PA), an ILFM\_PS with multiply-by-8, and an up-conversion mixer. We adopt polar direct modulation structure. The reason to choose polar modulation over Cartesian modulation scheme is because of the high efficiency provided by polar modulation, which is due to the fact that the PA can be switching type to boost efficiency. Baseband signal is separated into amplitude  $A(t)$  and phase information  $\Phi(t)$ . Amplitude information directly modulates PA power supply, while phase information is modulated through an up-conversion mixer.

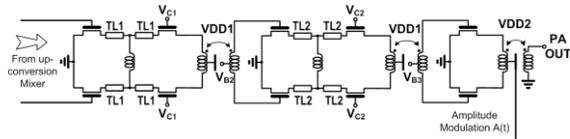
The PA is demonstrated separately through a CMOS 65nm technology. As shown in Figure 6, this PA features three stages, with the first two stages based on cascode structure to boost signal gain and improve isolation and the last

stage based on common source structure to boost output signal power and transmission efficiency. Because of the cascode structure from the first two stages, higher power supply can be applied without affecting device liability. Therefore, there are two power domains in this PA, VDD1 for the first two stages and VDD2 for the third (the last) stage. The signal amplitude is modulated through VDD2. To alleviate large parasitic capacitance in the inner node between the amplification device and the cascode device, a T matching network is inserted to realize power matching to reduce signal loss for high gain and high power efficiency. This PA is designed with differential configuration for better common mode and noise rejection. To facilitate testing, output signal is converted into single-ended format through a transformer based balun. The inter-stage matching is also realized through transformers, which integrates several functions together: compact layout, individual bias optimization, and symmetrical physical design, etc. These features allow a high power efficiency and a high output power design. An individual PA has been fabricated with a 65 nm CMOS technology with single-ended input and output signals, converted by on-chip baluns. Figure 7(a) shows the die photo with core chip area 0.45 mm X 0.09 mm. Figure 7(b) illustrates the measured small signal gain, output power, and power added efficiency (PAE) versus input signal power. It achieves about 10 dB small signal gain, 12 dBm saturated output power (P<sub>sat</sub>) and 11% PAE.

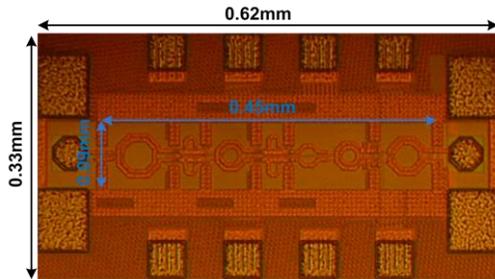
Another critical component in this W-band transmitter is our newly proposed injection locking frequency multiplier based phase shifter (ILFM\_PS). Figure 8 (a) illustrates the schematic. It has three multiply-by-2 stages, resulting in X8 overall multiplication ratio. The input signal is 11.75 GHz and the output is 94 GHz. Each multiply-by-2



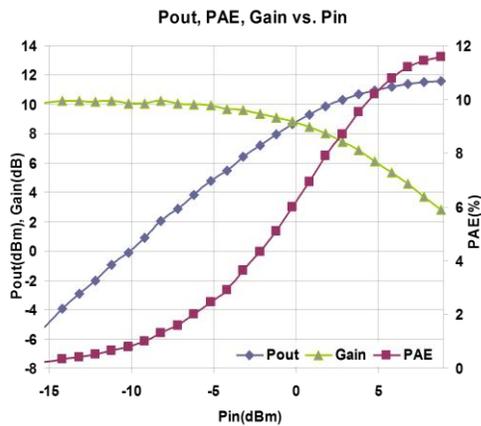
**Figure 5.** A W-band Tx element with injection locking frequency multiplier based phase shifter enabled low frequency LO distribution network in phase array systems



**Figure 6.** The included 3-stages W-band PA with off-chip amplitude modulation control on the last stage power supply



(a)

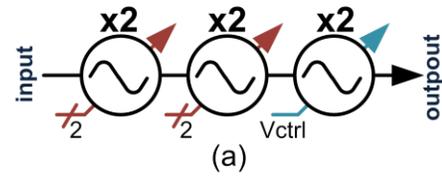


(b)

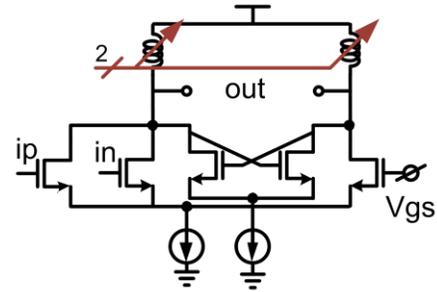
**Figure 7.** (a) The W-band PA die photo in 65nm CMOS, and (b) the measured PA performances

stage is presented in Figure 8(b) with the device biased at class-B region for optimum second-order harmonic generation. The phase shifting is implemented by changing tank capacitance. Both digital control switching capacitor and analog control varactor are used to generate a desired output phase. First two stages utilize digital control to form as most significant bit (MSB) control and the last stage adopts analog varactor based control to further fine tune output phase. Figure 4 presents the simulated phase shifting versus 4-bit digits from the first two stages, which demonstrates a linear phase shifting relationship with about  $3^\circ$  resolution. The linearity resolution will be further improved through the analog phase adjustment of the last stage.

This transmitter has been implemented in a 65nm CMOS technology, with the layout shown in Figure 9. The chip area including pads is 0.75 mm X 0.9 mm.

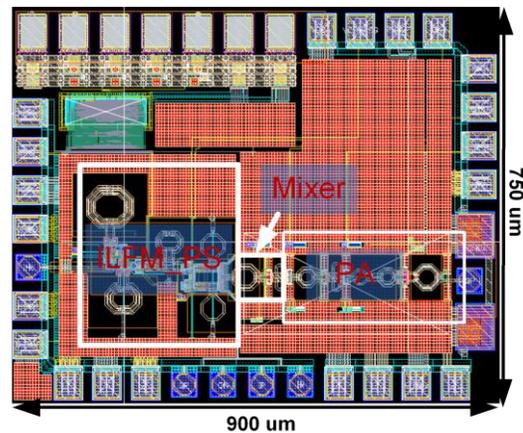


(a)



(b)

**Figure 8.** (a) The ILFM\_PS structure in this W-band transmitter with 3 cascade multiply-by-2 stages, and (2) the schematic of each multiply-by-2 circuit operating at Class B status



**Figure 9.** The layout of a W-band Transmitter element with ILFM\_PS in 65nm CMOS technology

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