Two-Way Current-Combining W-Band Power Amplifier in 65-nm CMOS

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***Abstract*—This paper presents a two-way current-combining-based W-band power amplifier (PA) in 65-nm CMOS technology. An analytical model and design method for W-band power combiners are presented, which indicates current combining is preferred for millimeter-wave frequencies due to a good current handling capability, symmetrical design, and low sensitivity to parasitics. To demonstrate the concept, a two-way current-combining-based PA has been fabricated, where each channel utilizes compact and symmetrical transformer-based inter-stage coupling to realize a preferred fully differential implementation. This PA operates from 101 to 117 GHz with maximum power gain of 14.1 dB, saturated output power ($P\mathrm{sat}$) of 14.8 dBm, and peak power-added efficiency of 9.4%. The core chip area without pads is 0.106 mm^2.**

***Index Terms*—Power amplifier (PA), power combiner, W-band.**

I. Introduction

THE W-band of the electromagnetic (EM) spectrum is promising for various applications such as wireless sensing, imaging, and communications. Its unique characteristic of penetration through fog/rain/cloud could enable all-weather radar and sensing. The wide bandwidth around this frequency also makes it very attractive to ultrahigh-speed wireless and satellite communications [1]–[3]. In these W-band systems, power amplifiers (PAs) are one of the most challenging components because of the requirements of high output power and energy efficiency. Conventionally, W-band amplifiers are mainly based upon discrete III–V compound semiconductor devices [4], [5]. However, current III–V semiconductor processes are not suitable to support very large scale integrated (VLSI) digital circuits, which is indispensable for system-on-a-chip (SoC). Therefore, multichip integration becomes necessary, and tends to produce a large form factor system. The associated inter-chip integration also introduces the complicated interface circuitries among different chips.

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On the other hand, silicon processes, especially CMOS technologies, have the advantages of high level integration, small form factor, and potential low cost. Therefore, CMOS millimeter-wave circuits have the potential to materialize wide deployment, and thus attract lots of research interest [6]–[11]. In millimeter-wave PA research, V-band (50–75 GHz) CMOS PAs have been demonstrated to deliver up to 20-dBm saturated output power with 20% power-added efficiency (PAE) [12]–[19]. Recent W-band CMOS PA studies have also demonstrated higher than 10-dBm $P\mathrm{sat}$ with power efficiencies less than 6% [20], [21].

To further increases output power and efficiency of W-band CMOS PAs, the inherent drawbacks of silicon processes must be overcome. First, the existing CMOS device speed is still limited. For instance, f_T and f_{MAX} of the devices in 65-nm CMOS technology are around 200 GHz. It does not provide sufficient margin to process W-band frequency signals. Therefore, switch-mode PAs, potentially with higher efficiency, are not applicable due to the required high-order harmonic operations. It suggests a linear PA approach at the cost of low efficiency. Second, silicon processes inherent high losses degrade PA efficiency. The losses include silicon substrate coupling losses, interconnect electrical and magnetic coupling losses, and contact ohmic losses. Such a drawback mandates optimization of both active and passive devices for high-frequency PAs. Third, low supply and breakdown voltages in deep-submicrometer CMOS technologies constrain high power delivery. Reducing output impedance can increase output power, but at the cost of low efficiency due to higher losses from the impedance matching network with a higher impedance transformation ratio. Consequently, such optimization leads to tradeoffs between output power and efficiency. To mitigate this issue, power-combining structures with multiple PA channels are widely adopted [14]–[20]. Three power-combining schemes are normally used in millimeter-wave PAs: direct current combining, Wilkinson power combining, and transformer-based power combining. Each scheme has its own pros and cons and will be discussed in Section II.

After a detailed comparison among existing power combiners, we conclude that transformer-based current combiners are more suitable for ultrahigh-frequency operations. Hence, he demonstrate a two-way current-combining W-band PA in a 65-nm CMOS technology. Section II describes the design in detail, including the CMOS PA challenges, comparisons of power combiners, advantages of current combiners and the associated designs, and the optimization of each channel PA. Section III presents measurement results, and is then followed by a conclusion in Section IV.

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II. Two-Way Current-Combining PA

A. Millimeter-Wave CMOS PA Challenges

The detailed circuit specifications, especially the required PA output delivery power, must be studied based on the system link budget analysis before circuit design. For instance, a wireless link with a 10-m distance between a transmitter and receiver has an 84.4-dB path loss based on the Friis propagation equation (1), where a 4-dBi antenna gain from both a transmitter and a receiver at 100-GHz frequency is assumed. Given -70-dBm receiver sensitivity, the minimum output power from a transmitter PA must be larger than 14.4 dBm

$$P_t = P_r - G_t - G_r - 20\ \log\left(\frac{\lambda}{4\pi R}\right) \tag{1}$$

where P_t is the required transmitter output power, P_r is the receiver sensitivity, G_t and G_r are the transmitter and receiver antenna gain, respectively, λ is the signal wavelength, and R is the propagation distance. Such high output power is challenging for one channel of the CMOS PA due to low breakdown and supply voltages of the technology.

To simultaneously achieve high power delivery while meeting device reliability constraints due to low breakdown and supply voltages, a small output impedance $R_{\rm PA}$ is needed. While a low output impedance often demands a high-impedance transformation ratio, $r = R_l/R_{\rm PA}$, where R_l is the load impedance and is normally equal to 50 Ω in conventional systems. A high r tends to result in a low efficiency of the impedance transformation network $\eta_{\rm net}$. The relationship between $\eta_{\rm net}$ and the transformation ratio r has been presented in [22]

$$\eta_{\rm net} = \frac{Q_{\rm ind}^2 + 1}{Q_{\rm ind}^2 + \dfrac{r + \sqrt{r^2 + 4Q_{\rm ind}^2(r-1)}}{2}}. \tag{2}$$

For example, in order to deliver 100-mW output power, PA output impedance needs to be lower than 5 Ω (or $r = 10$) under a 1-V supply. With a typical inductor quality factor of 10, the efficiency of such an impedance transformation network $\eta_{\rm net}$ is only about 70%, which greatly limits PA efficiency

Another issue of low PA output impedance is the associated high sensitivity to parasitic resistance. A low $R_{\rm PA}$ indicates a high output current $I = V_{DD}/R_{\rm PA}$, and thus induces a high power loss of $I^2 R_{\rm par}$ due to parasitic resistances $R_{\rm par}$. Still using the above example, to deliver 100-mW output power requires an output current rms value of about 140 mA. A serial 1-Ω parasitic resistance may consume ∼20-mW power, which introduces another extra 20% degradation on top of the overall power efficiency.

Moreover, a high operating frequency further constrains power efficiency. Since W-band frequency is close to device cutoff frequencies, it is very hard to support higher order harmonics. Consequently, it is challenging to realize switching-type PAs at such frequencies for high efficiency. For example, the devices in the 65-nm CMOS technology, used in this PA design, has the unit current gain frequency f_T of about 200 GHz, which will further drop significantly due to external parasitics from device layout. Since a fast device is still beneficial to the PA output power and efficiency, it is preferred to maximize device operating speed. To achieve so, the PA devices are normally biased at saturation region, which results in the unavoidable constant current flowing through the active devices and leads to large power waste. Another critical factor to degrade power efficiency at high frequency is the reduced device power gain. Fig. 1 shows the simulated available power gain versus frequency for an nMOS device with the size of 20 μm/60 nm. At 100 GHz, the maximum available power gain is only about 8.7 dB. To achieve a high power gain, e.g., 20 dB, multiple stages are needed. Compared to a single-stage PA operating at lower gigahertz frequencies, multistage structures degrade the power efficiency. In addition, skin effect at high frequencies further increases interconnect and contact resistance. These extra resistances not only consume more power through ohmic losses, but also further degrade the performances of both active and passive devices. For example, skin effect reduces the passive devices' quality factor Q. All these issues challenge high-power and high-efficiency PA design.

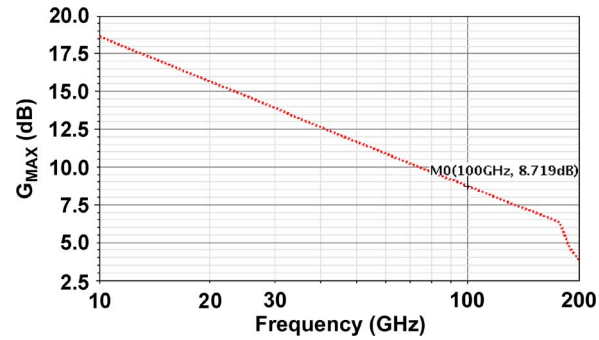


Fig. 1. Simulated maximum available power gain of a 65-nm nMOS device with the size of 20 μm/60 nm.

To achieve an optimum tradeoff between output power and efficiency for high-frequency CMOS PAs, multichannel amplifiers with power combining are a viable solution. The following section discusses power combing techniques and compares three different types of power combiners.

B. Power Combiner Comparisons

To boost transmitter output power, power-combining techniques are utilized in RF integrated circuits (ICs) and monolithic microwave integrated circuits (MMICs) and systems, such as space power combining [23] and on-chip power combining [14]–[20]. Space power combining requires multiple antennas and a wide channel spacing (typically around $\lambda/2$) for on-chip implementations at millimeter-wave frequencies, which may induce high design complexities and large chip areas. Therefore, on-chip combining methods are more widely adopted. Among them, there are mainly three structures: direct power combining, Wilkinson power combining, and transformer-based power combining, as shown in Fig. 2. Direct power combining has been utilized in [17], which directly combines the currents from multiple channels and applies them on the output load for a large power. To optimize each PA channel output power and efficiency, impedance transformation network is necessary. Typical tuning-stubs-based impedance-transformation networks may induce large losses and asymmetrical layouts

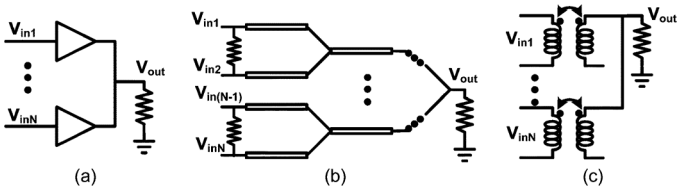


Fig. 2. Three different power-combining structures. (a) Direct power-combining structure. (b) Wilkinson power-combining structure. (c) Transformer-based power-combining structure.

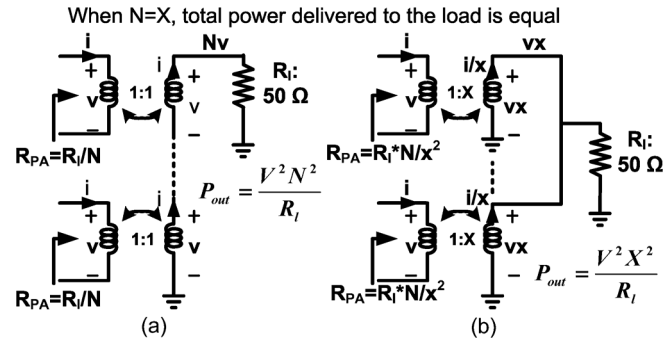


Fig. 3. Transformer-based power combiners. (a) Voltage combiner with 1:1 turns ratio. (b) Current combiner with 1:X turns ratio.

to complicate PA design and degrade circuit performance. Transmission-line-based Wilkinson power combining achieves good isolation with a matched condition for all ports at a designated frequency. Since a transmission line has a long length for on-chip implementations at millimeter-wave frequencies, lumped-element-based Wilkinson combiners are often used to save chip area. However, Wilkinson combiners are mainly suitable for only a narrow frequency range and sensitive to coupling and component parasitics. When the operating frequency deviates away from the designed frequency or there are large parasitics, the port isolation and matching conditions will be deteriorated significantly. The third approach is transformer-based power combining. It integrates power-combining and impedance-matching functions to provide a symmetrical and compact method, and therefore is adopted in this PA design.

C. Two-Way Transformer-Based Combiner

There are two types of transformer-based power combiners: voltage combiners and current combiners. In lower gigahertz operations, voltage combiners are widely utilized [24], [25] because they naturally transfer a low PA output impedance $R_{\rm PA}$ to the load, $R_l = 50\ \Omega$, as shown in Fig. 3(a). This provides the advantage of high output power delivery from each PA of $V_{DD}^2/R_{\rm PA}$. For 1:1 turns ratio, an N-way power combiner results in PA output impedance of $R_{\rm PA} = R_l/N\Omega$, and overall power delivery of an N-way voltage combiner is $P_{\rm overall_v} = V^2 \times N^2/R_l$, where V is the voltage swing of each channel's primary winding. $R_{\rm PA}$ is inversely proportional to the number of combining channels and can drop to a very small value for large N, and thus makes the PA sensitive to parasitics. The sensitivity ratio, $a = R_{\rm par}/R_{\rm PA}$, is inversely proportional to $R_{\rm PA}$. Such relation implies that the higher the sensitivity ratio α, the worse PA's reliability is in the presence of process and temperature variations. Due to this concern, voltage combiners are not preferred for combining with a large number of channels [26].

On the other hand, an N-way current combining with 1:1 turns ratio leads to a higher PA output impedance of $R_{\rm PA} = R_l \times N\Omega$. The parasitic sensitivity factor $a = R_{\rm par}/R_{\rm PA}$ is better than that of voltage combiners. However, the power delivered from each channel is reduced due to a higher output impedance. To alleviate that, a transformer ratio of 1:X can be applied with X larger than 1, as shown in Fig. 3(b). Therefore, the PA output impedance$R_{\rm PA}$ scales down to $(R_l \times N/X^2)\Omega$. Each channel primary winding current and secondary winding current are $I_p = V \times X^2/R_l \times N$ and $I_s = V \times X/R_l \times N$. Therefore, an N-way current combiner with 1:X turns ratio has the overall power delivery of $P_{\rm overall_c} = V^2 \times X^2/R_l$. Interestingly, the total power deliverable to the load in current combiner structures is independent to the number of channels given a fixed voltage swing from each primary channel, but proportional to the square of the coupling transformer turns ratio. However, increasing the number of channels reduces the output power delivery requirement from each PA channel. To establish fair comparison between voltage combiners and current combiners, let us set the same power delivery for both structure, which is satisfied by setting $X = N$.

Given the same power delivery, current power combiners are preferred for two key reasons. First, although each channel primary winding impedances and currents are the same when $X = N$, the current of the secondary winding is different for the two cases: $I_{s_c} = V \times X/R_l \times N$ for current combining versus $I_{s_v} = V \times N/R_l$ for voltage combining. Therefore, the high current of secondary winding in voltage combining not only demands high current handling capability, but also makes them sensitive to parasitic resistance in the secondary winding due to the power loss of $I^2 R_{\rm par}$. This difference can be explained intuitively from current distribution scenario. A current combiner distributes current among different channels. Thus, each channel only carries a smaller current with a lower current handling requirement. However, a voltage combiner needs to propagate the current from all the channels, and therefore requires higher current handling capabilities.

A second and even more important reason favoring current combining over voltage combining is due to the physical design constraints, especially in terms of channel symmetry. Any amplitude and phase mismatches degrade power-combining efficiency. Some system calibration method scan be adopted to mitigate mismatch issues. However, the schemes are normally band-limited and impose design complexities. Therefore, channel symmetry becomes one of the key merits in power combiner physical design, where current combining has advantages over voltage combining. In order to evaluate this characteristic, we designed two-way combiners in both voltage- and current-combining manners, as shown in Fig. 4.

To form a fair comparison, both combiners use the same transformer structure for each channel with the same distance between channels. The only difference between these two combiners is the output combining approaches: with parallel current combining shown in Fig. 4(a) and voltage series combining

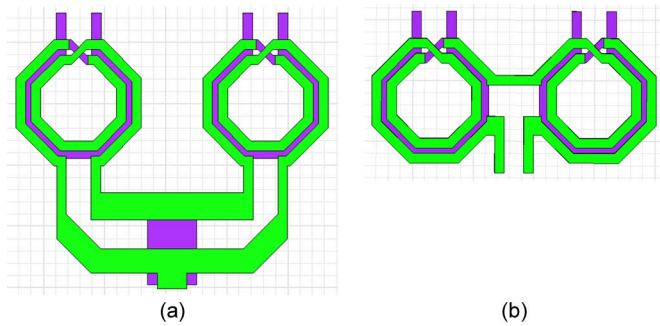


Fig. 4. Layout structures for performance comparison between: (a) two-way current combiner and (b) two-way voltage combiner.

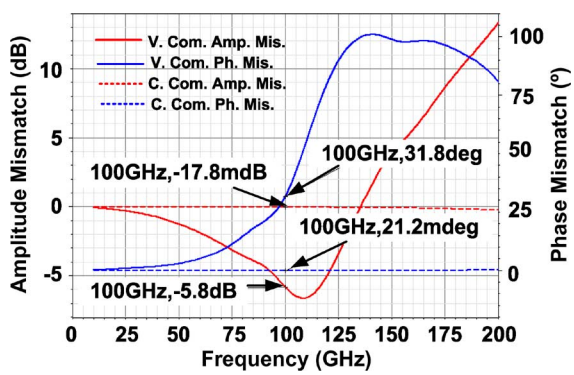


Fig. 5. Amplitude and phase mismatch for both voltage and current combiners. Solid lines represent the voltage combiner and dashed lines represent the current combiner with red (in online version) for amplitude mismatches and blue (in online version) for phase mismatches.

shown in Fig. 4(b). Fig. 5 presents the simulated amplitude and phase mismatches from both combiners. The current combiner shows amplitude mismatch of 0.02 dB and phase mismatch of 0.03° at 100 GHz. However, the voltage combiner presents very large mismatches with 5.8 dB in amplitude and 32° in phase, which results in higher than 2-dB combining loss. This can be explained through a simplified model, as shown in Fig. 6. For simplicity, each transformer can be represented as a magnetic coupling device and some parasitic to the ground, as shown in the dashed line boxes in Fig. 6. Without losing generality, we use a capacitor to represent the parasitic impedance to the ground. Fig. 6(a) illustrates the voltage combiner. To facilitate description, a source is applied at the secondary winding side, which is the output of the combiner, to observe the coupling signals at the input sides. Passive combiners' reciprocal feature ensures the validity of this analysis. Due to the leakage current to the ground through the parasitic capacitors, the current flowing through each channel magnetic coupling device is different with $i_{S1} = i_{S2} + i_{\mathrm{gnd2}}$. This leads to different coupling current to the primary windings, i.e., $i_{P1} \neq i_{P2}$, and thus causes mismatches among channels. However, the current-combining structure is fully symmetrical and has no mismatches among channels, as shown in Fig. 6(b). The simulated minor mismatches may come from the finite accuracy from EM simulation tools. To summarize, the key reason of large mismatches in voltage combiners is due to the cascade configuration in the secondary winding, which has leakage current to the ground in each stage that results in the current

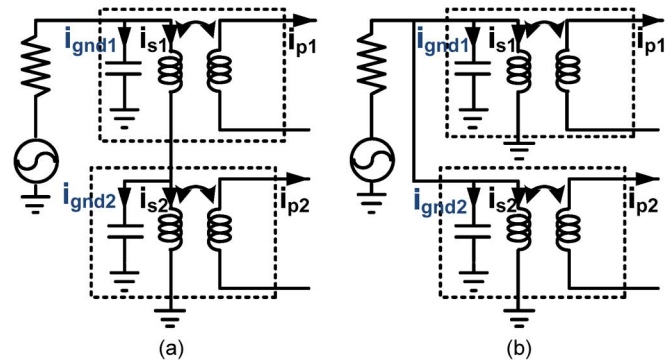


Fig. 6. Both: (a) voltage and (b) current combiners built by a simplified transformer model.

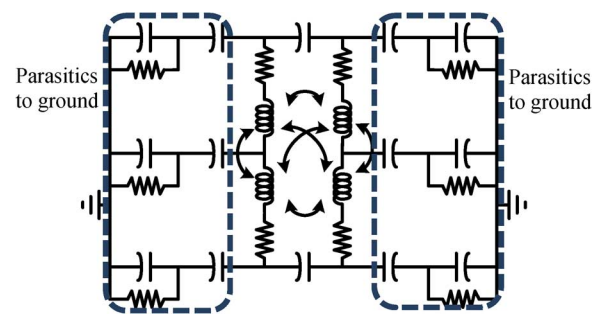


Fig. 7. Physical model for the transformer used in the combiners.

reduction along the path. The larger number of the combining channels, the more mismatches will show up, and the higher the operating frequency, the more mismatches kick in. These are due to a greater portion of the current leaking into the ground.

To verify this concept, we have built an equivalent physical model to represent the transformer, as shown in Fig. 7. We then use this model to construct both current and voltage combiners. With the original model shown in Fig. 7, the phase and amplitude mismatches match with EM simulation results: current combining has perfect match conditions and voltage combining shows large mismatches. To validate the above theory, we purposely removed the parasitics to ground (the circled part in Fig. 7). The voltage combining also then shows perfect matched scenarios because there is no current leaking to the ground. Fig. 8 shows the simulated phase and amplitude mismatches of voltage combiners with two different transformer models: the original model from Fig. 7 and the modified model by purposely removing the parasitics to the ground. The mismatches with original model are serious, which are similar to that shown in Fig. 5. However, once the parasitics to the ground are removed, voltage combining also demonstrates perfect matching performance.

Based on above analysis, we then conclude that current combining is more suitable in ultrahigh-frequency operations due to better current handling capability and better amplitude and phase matches among channels, therefore leading to a low combining loss. In this two-way combining PA structure, there are two combiners or splitters: the one at the input as a power splitter and the one at the output as a combiner. Since combiners and splitters are reciprocal, they can be designed from an identical power-combining point of view. At the input side, to match

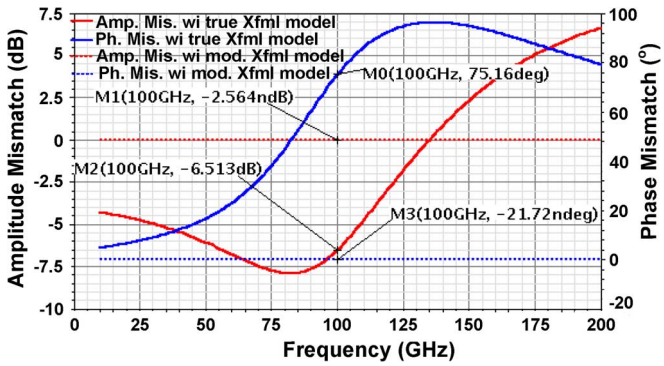


Fig. 8. Voltage combiner amplitude and phase mismatches with both the transformer physical model and a modified transformer model by removing the parasitics to ground. Solid lines represent mismatches with the physical model and dashed lines represent mismatches with the modified transformer model.

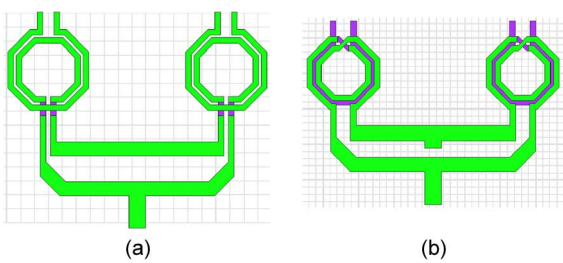


Fig. 9. (a) Input power splitter and (b) output power combiner designed in the W-band PA.

higher input impedance at the device gate, the 1:1 turns ratio is chosen as shown in Fig. 9(a). It deploys a lateral coupling structure to maximize the usage of top ultra-thick metal (> 3.4 μm) for minimum losses. The larger winding turn is utilized at the internal PA input and the smaller winding turn connects the chip input. This provides extra voltage gain at the PA input, and the output power combiner uses a 1:2 turns ratio for lower output impedance and larger output delivery power, as discussed earlier in this section. As shown in Fig. 9(b), the primary winding has one turn, implemented with the combined second and third top metals (0.9 and 0.22 μm). The secondary winding is two turns and is majorly implemented by the top ultra-thick metal. The primary and secondary coils are stacked with an offset instead of directly vertical to maximize mutual magnetic coupling and boost its self-resonant frequency by minimizing the capacitive coupling.

D. PA Design

One of the biggest challenges in W-band PA design is the device optimization and modeling. At such high frequencies, the active device model becomes highly layout dependent, which makes it difficult to offer a universal model. In particular, the extrinsic parasitic, such as gate, source, and drain resistance, substrate resistance and coupling capacitors among them, ultimately determines the maximum achievable gain. The MOS f_T and f_{MAX} can be approximated as

$$f_T = \frac{g_m}{2\pi C_{\mathrm{gt}}} \quad f_{\max} = \sqrt{\frac{f_T}{8\pi R_g C_{\mathrm{gd}}}} \tag{3}$$

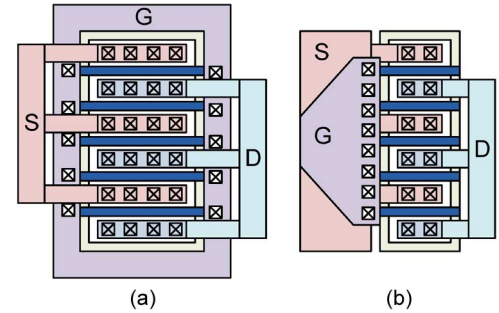


Fig. 10. MOS device connection. (a) RF device provided by Foundry. (b) Device layout design in this W-band PA.

where C_{gt} is the gate total capacitance, R_g is the gate resistance, and C_{gd} is the gate–drain capacitance. All these must be minimized to provide optimum performance. However, these optimizations do not follow the same trend and reinforce tradeoffs. For example, a multifinger structure reduces the gate resistance for wide gatewidth. It not only boosts device f_{MAX}, but also significantly improves noise figure. However, the gate to substrate and gate to drain/source capacitances increase with the number of fingers, which in turn degrades f_T. Double gate connection could be used to further reduce the serial gate resistance. However, it inevitably increases the gate coupling capacitance and even routing inductance, which becomes more severe at high frequencies. In our design tradeoffs, 0.6-μm finger width is chosen in this amplifier with a single side gate connection. It not only provides relatively small gate serial resistance and capacitance, but also allows area efficient connection that offers low resistance source/drain ties. Same as gate resistance, the device metal connections also significantly affect performance. The wiring style of RF device provided by the foundry, shown in Fig. 10(a), may not be optimized for such high frequency due to its large gate connection resistance, excessive parasitic capacitance, and especially the coupling capacitance between gate and drain that contributes to parasitic miller capacitance. Given wide signal wiring inside millimeter-wave amplifiers, a new device access scheme using single gate connection illustrated by Fig. 10(b) may render better performance by offering smaller gate resistance through paralleling and minimizing gate drain capacitance.

The existing BSIM3V4 models, supported by foundries, are dedicated to low-frequency operations and cannot be directly applied to millimeter-wave amplifier design. An improved model equipped with extrinsic parasitics, including serial resistors, coupling capacitors, substrate capacitors, and access line effects is used to facilitate the design as shown Fig. 11(a). R_G, R_D, and R_S stand for the serial resistance of gate, drain, and source introduced by connections; C_{GS}, C_{GD}, C_{DS} are coupling capacitors, and the transmission lines embody the access line effects, which incorporate both resistive/capacitive and magnetic effects. Practically, it is hard to model these parasitics into lumped fashion so the corresponding EDA tools are necessary to assist the procedure. The proximity parasitic resistance and capacitance are extracted through Caliber RCX. The metal wirings are then simulated with EM tools to cover the access line effects. The ultimate millimeter-wave device

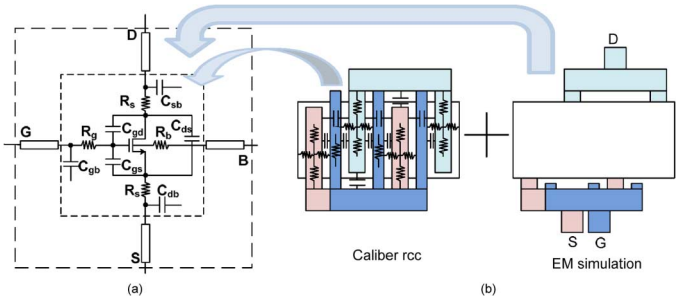


Fig. 11. (a) Adopted millimeter-wave MOS device model in the PA design. (b) Caliber RCX extracts rcc of device proximity area and EM simulation models access lines.

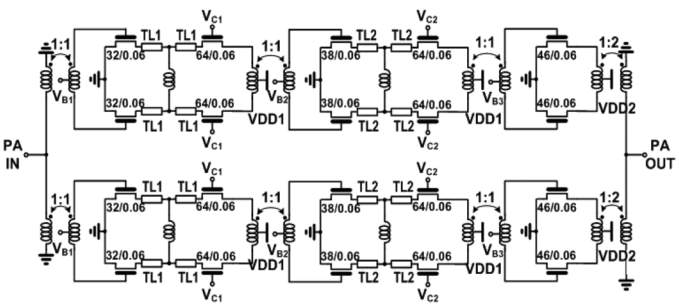


Fig. 12. Schematic of the two-way current-combining PA.

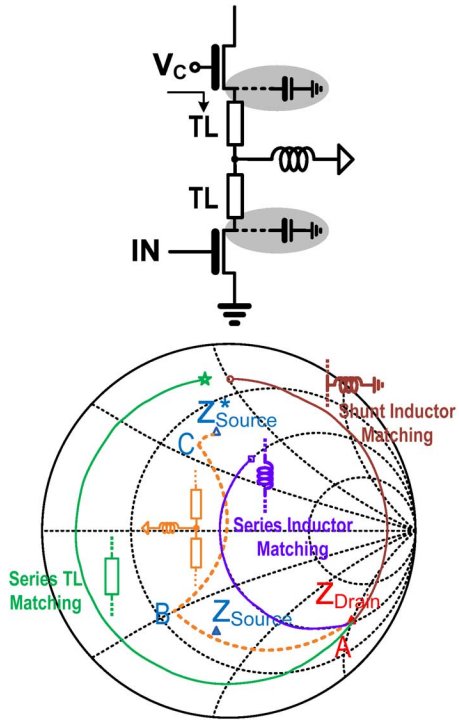


Fig. 13. (a) PA inter-stage T-matching network. (b) Smith chart representation.

model is built by adding these two parts on top of the foundry provided core model, as depicted in Fig. 11(b).

Fig. 12 presents the proposed two-way current combined PA schematic. A power splitter separates the input signal into two paths and a power combiner merges the output for higher delivery power. Both the power splitter and combiner also serve input and output matching purposes.

To increase gain and boost stability, a cascode structure has been adopted in the first two stages. However, such a structure creates low-impedance paths from cascode nodes to ground through stray capacitance of the devices and interconnects. At millimeter-wave frequencies, this path significantly wastes power and degrades PAE. A T-network is then inserted at the cascode node to achieve wideband matching between common source (CS) and common gate (CG) devices, as shown in Fig. 13. A transmission line stub is used first to transform the impedance from capacitive node A of the CS device drain to node B. A shunt inductor and another transmission line stub are used afterwards to transform the impedance to inductive node C and then fulfill the conjugate match. This network mitigates the lossy path and consequently improves the amplifier gain and PAE. However, it slightly degrades the amplifier linearity by 0.7 dB due to the increased cascode node impedance. According to our simulations, the proposed T-network improves the cascode amplifier's gain by >4 dB and reduces amplifier's dc power consumption by 50% for the same amplification gain. Compared with simple inductor shunting and inductor/transmission line series matching, this T matching network could fulfill conjugate matching with minimum loss.

The PA inter-stage coupling is achieved by transformers [27]. This structure has several prominent characteristics. First, it provides innate dc blocking so that each stage can optimize its own bias independently. Second, flexible voltage/current gain can be achieved by adjusting the turns ratio. The coil turns ratio is chosen to provide a larger voltage swing to the next stage input while keeping a smaller swing at its own output to ensure PA driver stages away from early saturation for high linearity. Third, the natural inter-stage T matching network accomplishes inter-stage tuning and matching. Fourth, the physical separation between input and output signals forms necessary space for isolation and eliminates extra undesired wiring for symmetrical/compact physical design. These features contribute to the high-performance PA design.

The PA last stage is designed with CS configuration to deliver maximum output power. To realize compact design, the output current combiner at the drain load serves as frequency tuning, impedance transformation, as well as current combining. Due to the bidirectional feature of transformers and EM couplings, the design optimization must include all the circuit components and peripheral structures. Therefore, we have conducted the EM simulation for the entire PA structure implemented in the layout to ensure all the couplings are included in our design optimizations. To tradeoff the PA gain, linearity, and reliability concerns, there are two power domains. VDD1 is the supply for the first two stages in the cascode configuration. Due to the cascode configuration and the cascode device's bulk connecting to a higher votlage instead of ground, VDD1 can be set higher than the normal supply voltage. VDD2 is the supply of the last CS stage and is set at typical supply conditions.

III. Measurement Results

The proposed two-way current combined PA has been fabricated in a 65-nm CMOS technology. To characterize the PA small-signal performance, an Agilent vector network analyzer

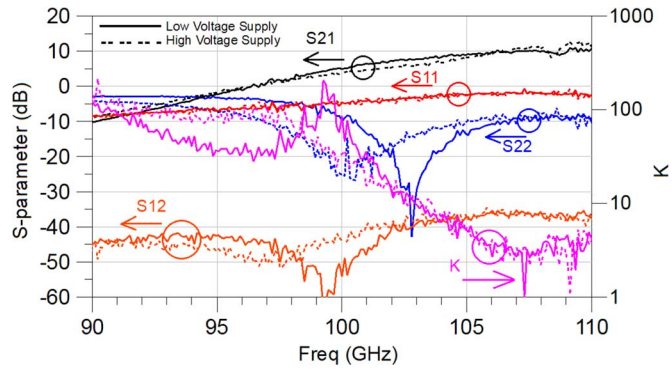


Fig. 14. Measured S-parameters at two supply conditions: a low supply condition with $VDD1 = 1.4$ V and $VDD2 = 1$ V, and a high supply condition with $VDD1 = 2$ V and $VDD2 = 1.2$ V.

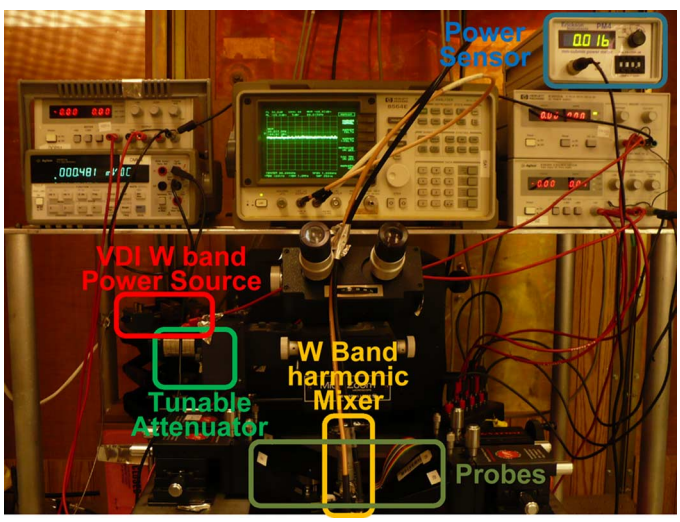


Fig. 15. W-band PA measurement setup for large-signal characterization.

(VNA) with frequency extension to 110 GHz is utilized. We measure the PA at two different supply conditions: a low supply condition with $VDD1 = 1.4$ V and $VDD2 = 1$ V; a high supply condition with $VDD1 = 2$ V and $VDD2 = 1.2$ V. Fig. 14 shows the S-parameter measurement results and associated K factor below from 90 to 110 GHz at the two different supply conditions. It shows the PA has peak gain around 109 GHz, which is close to 11 and 13 dB for the two supply conditions.

Fig. 15 shows the large-signal measurement setup. A harmonic mixer is used to sweep the PA gain quickly first, then a power sensor is used to characterize the amplifier output power, linearity, and PAE. The power source consists of a W-band power source provided by Virginia Diode Inc. (VDI), Charlottesville, VA, and a tunable attenuator with 50-dB dynamic range.

Fig. 16 shows the measured PA saturated output power, PAE, and corresponding power consumption across the frequency from 100 to 120 GHz at the two supply conditions. The maximum gains are 13 and 14.4 dB correspondingly and the 3-dB bandwidth is about 9 GHz from 101 to 110 GHz. Peak PAEs occur around 107 GHz. When generating saturated output power in this frequency, the low supply condition consumes 165

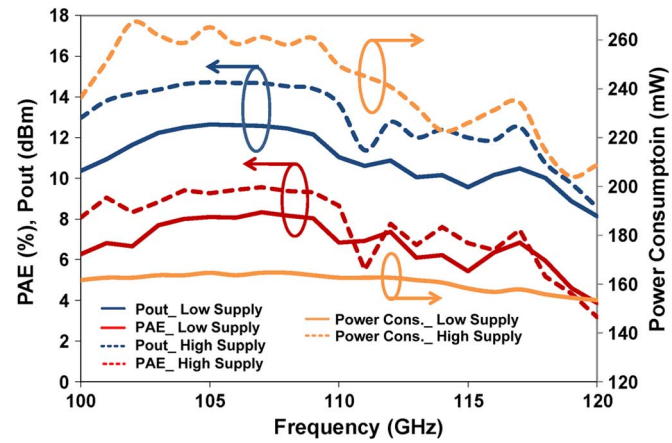


Fig. 16. Measured W-band PA saturated output power, PAE, and corresponding power consumption from 100 to 120 GHz with solid lines for low supply condition and dotted lines for high supply condition.

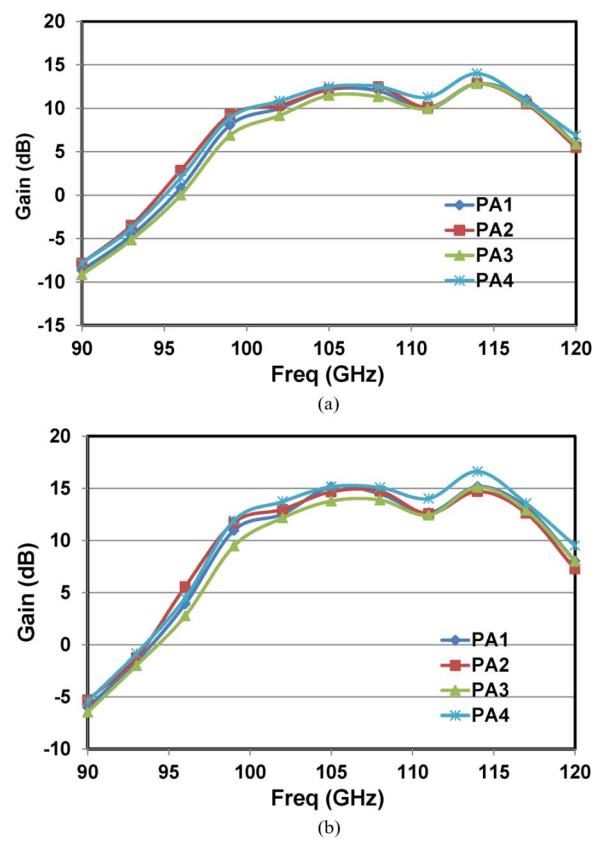
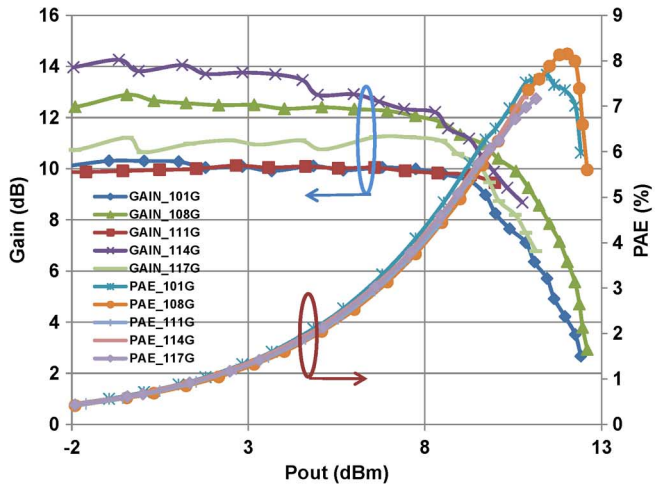


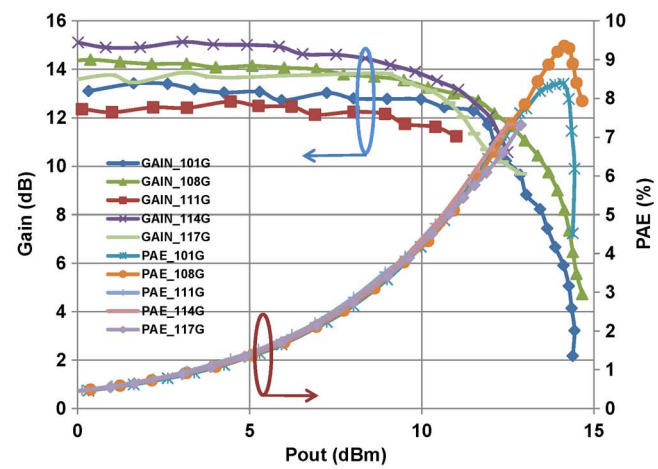
Fig. 17. Measured W-band PA gain from four different dies under: (a) $VDD1 = 1.4$ V, $VDD2 = 1$ V and (b) $VDD1 = 2$ V, $VDD2 = 1.2$ V.

mW with VDD1 drawing 77 mA at 1.4 V and VDD2 drawing 57 mA at 1 V. The high supply condition consumes 267 mW with VDD1 drawing 90 mA at 2 V and VDD2 drawing 72 mA at 1.2 V. The low saturated output power beyond 111 GHz is mainly due to the low source power and a lower PA gain, which is also the reason that we cannot fully characterize the PAE.

Fig. 17 presents the PA gain versus input signal frequency measured from four dies with a harmonic mixer at the same two supply conditions. The PA delivers on average 3-dB more gain when biased at higher supply conditions due to larger device



(a)



(b)

Fig. 18. Measured W-band PA gain and PAE versus $Pout$ at 101, 108, 111, 114, and 117 GHz under: (a) $VDD1 = 1.4$ V, $VDD2 = 1$ V and (b) $VDD1 = 2$ V, $VDD2 = 1.2$ V.

TABLE I
PERFORMANCE SUMMARY AND COMPARISONS

PA technology	Working Frequency	Gain (dB)	Psat (dBm)	Peak PAE (%)	P1dB (dBm)	Core Area (mm^2)
This work (VDD1=1.4V, VDD2=1V)	101-117 GHz	12.2	12.9	8.2	9.6	0.106
This work (VDD1=2V, VDD2=1.2V)	101-117 GHz	14.1	14.8	9.4	11.6	0.106
[19] 65nm CMOS	85-100 GHz	10	13	4	7	0.069
[20] 90nm CMOS	91-108 GHz	18	11.8	6	9.3	0.4 (wi PAD)

trans-conductance. Under higher supply setup, the PA delivers >15-dB maximum power gain and provides >10-dB gain over 20-GHz bandwidth (98 ∼ 118 GHz).

Fig. 18 shows the measured PA gain and PAE versus output power under the two supply conditions. The output power at 111 GHz is not high enough to measure the OP1 dB due to the lower output power of the VDI power source at that specific frequency. The PA OP1 dB is about 11.6 dBm when $VDD1 = 2$ V/$VDD2 = 1.2$ V, 2 dB higher than the OP1 dB 9.6 dBm when the supplies are lower.

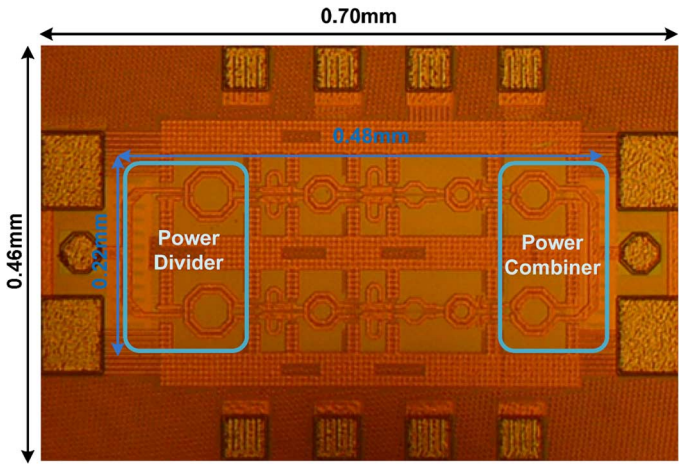


Fig. 19. Two-way current-combining W-band PA die photograph in 65-nm CMOS.

Table I summarizes this current-combined PA performance, and compares its performance with prior arts. Among all, this proposed PA delivers to date the highest output power with 9.4% PAE beyond 100 GHz in CMOS technologies.

Fig. 19 shows a PA chip photograph, which occupies 0.70 mm × 0.46 mm and 0.48 mm × 0.22 mm with and without pads, respectively. The input power divider and output power combiner use a similar architecture, but with different sizes, which can be clearly shown in the figure. The input and output PADs are also modeled and incorporated into the simulation to achieve optimum matching.

IV. CONCLUSION

A current-combined 101–117-GHz W-band CMOS PA has been demonstrated in 65-nm CMOS. It achieves 14.8-dBm saturated output power with better than 9.4% PAE and larger than 10-dB power gain across the frequency band of interest. It further extends the technology frontier and paves the way for future integrated sub-millimeter-wave high data-rate wireless communications and active imaging applications in CMOS technology.

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