CMOS THz Generator With Frequency Selective Negative Resistance Tank

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***Abstract*—This paper reports a CMOS terahertz oscillator with a novel frequency selective negative resistance (FSNR) tank to boost its operating frequency. The demonstrated oscillator can operate at a fundamental frequency of about 0.22 THz, exceeding the CMOS device cutoff frequency of f_T. The proposed architecture suppresses undesired 2nd and odd harmonics and boosts the fourth-order harmonic (0.87 THz), which radiates through an on-chip patch antenna. The THz oscillator's output spectrum is profiled by using a Michelson interferometer. The oscillator circuit consumes 12 mA from a 1.4 V supply and occupies a 0.045 mm^2 die area in a 65 nm CMOS technology.**

***Index Terms*—CMOS, interferometer, oscillator, resonant tank, terahertz (THz).**

I. Introduction

THE terahertz frequency range, from 300 GHz to 3 THz, has been identified as a critical spectrum range for numerous scientific and engineering systems. This is due to the wealth of molecular resonances that occur in this frequency band and the unique properties of the THz waves. such as the effective penetration through fabric/fog, and non-ionizing radiation with reduced health risks (as opposed to X-rays). Thus, there is increasing interest in THz imaging and spectroscopy for medical diagnosis, remote sensing of terrestrial/atmosphere, astronomy, and defense/safety applications [1]–[3].

However, the THz spectrum has not been explored as much as its lower or higher frequency counterparts due to both technology and physics limitations. For instance, traditional transit-time based electronic devices are typically limited by their low cut-off frequencies (i.e., f_T and f_{MAX}) and photonic devices are limited by their material's energy gap related to the emission energy. Currently, THz sources are usually fabricated with non-silicon materials. These devices include backward wave oscillators, cascade quantum lasers, Gunn diodes, and III-V HBT/HEMT based multipliers, which are all discrete, costly and bulky, thus limiting their uses [4]–[8]. Scaling of CMOS technologies provides high speed transistors [9], [10], which may offer a new approach and enable integrated THz systems with smaller form factor, lower cost and more convenient deployment for various applications. Several techniques have been reported for high frequency CMOS oscillators, such as a 320 GHz fourth-harmonic oscillator [11], a 410 GHz 2nd harmonic oscillator [12] and a 300 GHz fundamental frequency oscillator [13]. Recent demonstrations on THz imager and high power mm-wave oscillators have also marked rapid development in this area [14], [15].

In Gu *et al.*[16], we proposed a new oscillator architecture, which utilized a frequency selective negative resistance (FSNR) tank, in parallel with the conventional tank, to boost both the operating frequency and the loop gain for a fundamental oscillation frequency higher than the device f_T [16]. In this paper, we will elaborate with a comprehensive discussion of the oscillator design well beyond the content covered by the conference paper. This paper includes a more rigorously theoretical analysis of the FSNR technique, its sensitivity to non-idealities, such as mismatches, the design considerations and constraints, and the on-chip THz patch antenna design. We also provide a comparison between analytical, simulation and measurement results in the presence of mismatches.

We will describe challenges in terahertz CMOS oscillator design in Section II with a detailed circuit topology and operation mechanism discussion in Section III. Section IV discusses circuit design issues and trade-offs with subsequent optimizations. We then discuss the on-chip antenna design in Section V, present measurement results in Section VI and summarize the paper in Section VII.

II. Challenges on CMOS Terahertz Design

Despite a continuous increase in the device cut-off frequencies (f_T or f_{MAX}), deep-scaled CMOS IC technologies still suffer major drawbacks in realizing terahertz circuits and systems. These include:

1) Device speed limitation. The intrinsic device speed is still insufficient for THz circuits/systems. For instance, a 65 nm CMOS device has cutoff frequencies of f_T and f_{MAX} about 200 GHz. Therefore, novel circuit/system architectures and circuit designs must be devised to boost operation into THz frequency range.
2) Large losses. CMOS technology has more parasitics and other losses than its III-V counterparts. It includes gate and contact parasitic resistances, metal and substrate losses, interconnects mutual couplings, as illustrated in Fig. 1(a).

Manuscript received July 06, 2011; revised October 31, 2011; accepted December 06, 2011. Date of publication February 10, 2012; date of current version March 02, 2012.

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Digital Object Identifier 10.1109/TTHZ.2011.2181922

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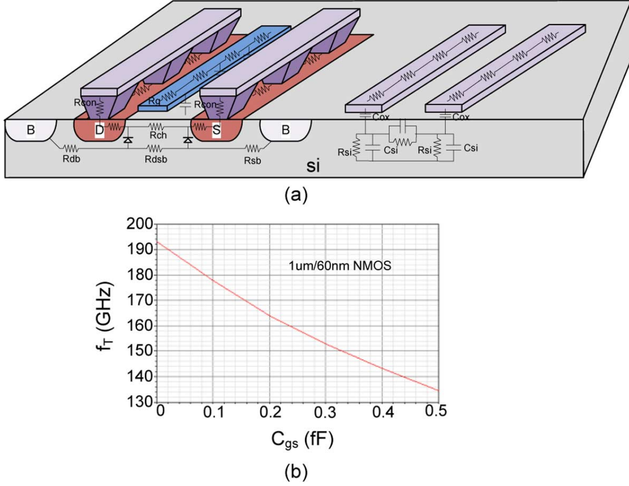


Fig. 1. (a) Loss mechanisms in CMOS technology. (b) Simulated f_T versus parasitic capacitance C_{gs}.

These parasitics, losses and couplings not only degrade device quality factor Q, but also limit a circuit's highest operating frequency to a fraction (1/3 to 1/2) of core active device's cut-off frequencies. Short channel devices in deep-scaled processes exacerbate parasitic capacitance between device electrodes due to their close proximity in physical layouts. Fig. 1(b) shows that f_T decreases significantly with the increase of the parasitic capacitanceC_{gs}. When the parasitic capacitance increases to 0.5 fF, the f_T decreases from more than 190 GHz to about 130 GHz with 0.2 mA bias current.

3) Ultrahigh frequency design challenges. To minimize device parasitic for terahertz signal generation, smaller active devices and passive components are generally required. Choosing a small inductor L leads to low tank parallel impedance,$R_p = \omega_N LQ$, which in turn demands larger active device transconductance g_m (or large device size) to satisfy gain requirement $g_m \times R_p \geq 1$. A larger device size increases the load capacitance, which in turn reduces the operating frequency instead. One may otherwise choose to reduce the active device size for a smaller tank load capacitance, which then leads to smaller transconductance and requires a higher inductor L for larger $R_p$to provide sufficient oscillation gain. It decreases the operating frequency as well. This dilemma persistently challenges the THz frequency oscillator design, especially when the operation frequency is close to or higher than device cut-off frequencies.

Consequently, nontraditional circuit design approaches must be created to overcome the deep-scaled CMOS technology limitations for terahertz circuits and systems.

III. Proposed CMOS THz Oscillator

A. Double Push–Pull Harmonic Frequency Generator

As discussed in Section II, it is difficult for silicon-based fundamental frequency generator to reach the THz frequency range due to device speed limitation. Therefore, a double push-pull superposition architecture is adopted for fourth-order harmonic signal generation. It couples two identical differential oscillators in quadrature phase to form the desired I and Q paths. The output signal is then constructed by superposing I/Q signals and is sensed at the common-mode node of the combined I/Q paths.

In the circuit design, the devices are biased at a class-AB condition to generate strong harmonics. At the common mode output node, the oscillation frequency's odd harmonics cancel each other out and can be ignored for simplicity in the analysis. Here, we only focus on the 2nd and 4th even harmonics. We assume the fundamental signals are $\pm A\cos(\omega_0 t)$ and $\pm A\sin(\omega_0 t)$ for I and Q paths, respectively.

For the I path, the second and fourth harmonics can be described at the common-mode node as

$$G_1 * (A\cos(\omega_0 t))^2 = G_1 * \frac{A^2}{2}(1+\cos(2\omega_0 t)) \quad (1)$$

$$G_2 * (A\cos(\omega_0 t))^4 = G_2 * \frac{A^4}{4}\left(\frac{3}{2} + 2\cos(2\omega_0 t) + \frac{\cos(4\omega_0 t)}{2}\right). \quad (2)$$

For the Q path, the second and fourth harmonics can be quantified at the common-mode node as

$$G_1 * (A\sin(\omega_0 t))^2 = G_1 * \frac{A^2}{2}(1-\cos(2\omega_0 t)) \quad (3)$$

$$G_2 * (A\sin(\omega_0 t))^4 = G_2 * \frac{A^4}{4}\left(\frac{3}{2} - 2\cos(2\omega_0 t) + \frac{\cos(4\omega_0 t)}{2}\right) \quad (4)$$

where G_1 and G_2 are the gain scaling factors and depend on circuit parameters. The combined output receives the signals from both I and Q paths and superposes them. According to (1)–(4), the second-order harmonic signals are out-of-phase from I/Q paths and cancel each other. However, the fourth-order harmonic is in-phase and produces a strong signal at the common-mode output node.

However, inevitable mismatches introduce non-desired harmonics and suppress desired ones. For example, when there are differential mismatches, odd harmonics cannot be suppressed efficiently. When quadrature mismatches exist, the second-order harmonic suppression is not infinite and the fourth-order harmonic signal power will be reduced. We have analyzed the mismatch effect and will present the associated analytical and simulated results for both second-order and fourth-order harmonics in the latter part of this section.

B. Frequency Selective Negative Resistance Tank

As discussed in Section II, one of the main reasons that the oscillator's operating frequency is limited is the severe losses in CMOS technology, which is hard to compensate through existing techniques. Ultrahigh frequency oscillation places limits on tank capacitance which, consequently, constrains the CMOS device size with insufficient negative transconductance g_m, normally formed by a traditional cross-coupled structure, to overcome the overall losses to meet oscillation criteria. One possible remedy is to add another negative resistance to reduce the losses with negligible loading to ensure terahertz oscillation.

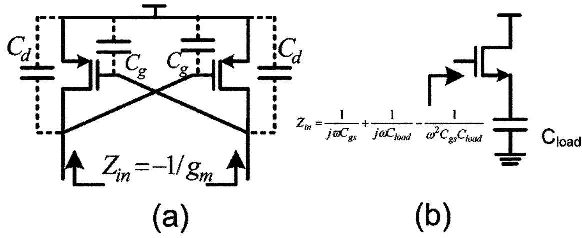


Fig. 2. Existing negative resistance generators: (a) cross-coupled pair and (b) gate impedance with capacitor load at the source.

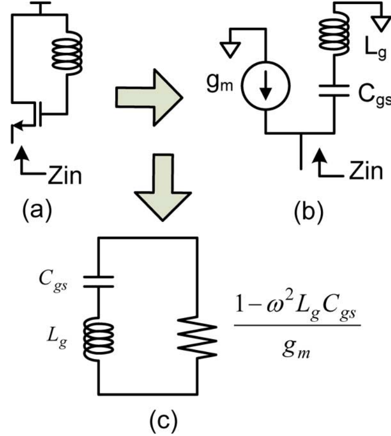
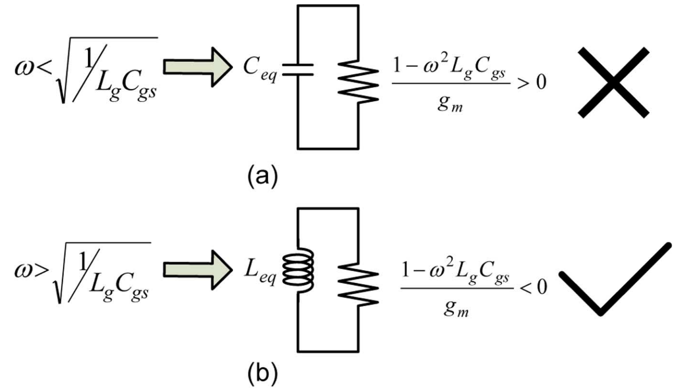


Fig. 3. (a) Proposed circuit to generate negative resistance. (b) Its small signal model and (c) equivalent circuit of source input impedance.



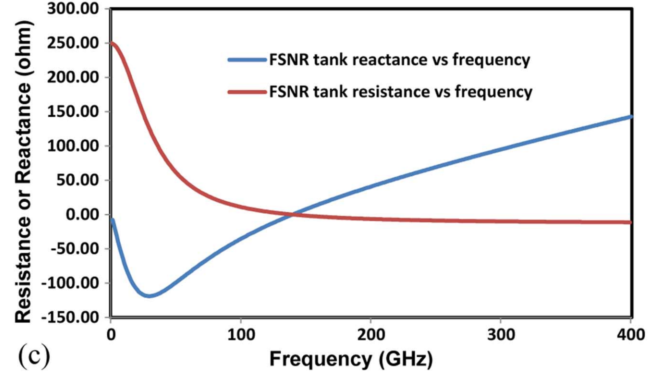


Fig. 4. FSNR tank behavior at different frequency ranges: (a) lower than resonant frequency; (b) higher than resonant frequency; and (c) simulated resistance and reactance values versus frequency.

Fig. 2 presents the existing negative resistance generator options. As shown in Fig. 2(a), the conventional cross-coupled pair for negative resistance is not viable because it substantially loads the tank with both the gate and drain capacitances, significantly reducing the oscillation frequency. Fig. 2(b) depicts another negative resistance generator [17], which creates a negative resistance at the gate with a capacitor source load. However, this approach cannot satisfy the requirement, either; this is due to the extra loading contributed by $C_{\rm gs}$ and $C_{\rm load}$.

An alternative approach shown in Fig. 3(a) offers a unique characteristic with a frequency selective feature [18]. The input impedance looking into the device source can be derived through the small signal equivalent model, shown in Fig. 3(b), as

$$\begin{aligned} Z_{\rm in} &= \frac{1-\omega^2 L_g C_{\rm gs}}{g_m} \left\| \frac{1-\omega^2 L_g C_{\rm gs}}{j\omega C_{\rm gs}} \right. \\ &= \frac{1-\omega^2 L_g C_{\rm gs}}{g_m} \left\| \left(\frac{1}{j\omega C_{\rm gs}} + j\omega L_g \right) \right. \end{aligned} \quad (5)$$

where L_g is the gate inductance, $C_{\rm gs}$ and g_m are the gate source capacitance and transconductance, respectively. It can be represented as an equivalent circuit shown in Fig. 3(c), which consists of the series-connected L_g and $C_{\rm gs}$ path in parallel with a resistor of value $(1-\omega^2 L_g C_{\rm gs})/(g_m)$.

This structure offers a unique frequency selective characteristic: it provides both inductance and negative impedance in a designed frequency range. Fig. 4 illustrates its operation mechanism. When the operating frequency$\omega < \sqrt{1/L_g C_{\rm gs}}$, the LC serial path is equivalent to a capacitor, $C_{\rm eq}$, which is in parallel with a positive resistance. This extra capacitance $C_{\rm eq}$ loads the original tank and lowers its resonant frequency. The resistance $(1-\omega^2 L_g C_{\rm gs})/(g_m)$ further reduces the overall parallel impedance, as shown in Fig. 4(a), which is not desired. However, when the operating frequency $\omega > \sqrt{1/L_g C_{\rm gs}}$, the LC serial path presents as an equivalent inductor,$L_{\rm eq}$, which is in parallel with a negative resistance, as shown in Fig. 4(b). This extra inductance, $L_{\rm eq}$, reduces the overall tank inductance and leads to a higher resonant frequency. The parallel negative resistance also boosts the tank overall parallel impedance to meet oscillation requirements, which satisfies the needs. Simulation results confirm the analysis, as shown in Fig. 4(c). The FSNR tank resistance is positive at frequencies less than resonant frequency ($\sim$140 GHz) and becomes negative at frequencies higher than the resonant frequency. Thus, this FSNR tank not only generates negative resistance beyond its resonance frequency, but also further pushes it higher by lowering the overall tank inductance.

The mechanism can be elaborated further by using Fig. 5, which presents the tank by combining the FSNR tank with a conventional LC tank. It creates a fourth-order resonant tank with two resonant frequencies, which can be derived through the tank impedance.

According to Fig. 5, the tank impedance can be expressed as

$$\begin{aligned} Z =& j\omega L_{\rm tank} \left\| \frac{1}{j\omega C_{\rm tank}} \right\| \\ & \times R_p \left\| \left(j\omega L_g + \frac{1}{j\omega C_{\rm gs}} \right) \right\| \frac{1-\omega^2 L_g C_{\rm gs}}{g_m}. \end{aligned} \quad (6)$$

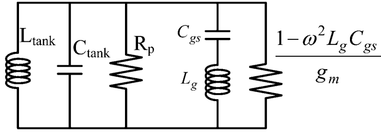


Fig. 5. Fourth-order LC tank by combining the FSNR tank with conventional tank.

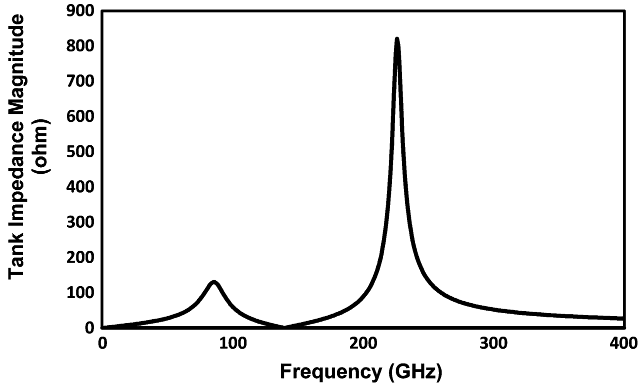


Fig. 6. Simulated tank impedance by combing FSNR tank and conventional tank, which demonstrates two resonant frequencies.

By solving (6), we can derive the two resonant frequencies, ω_1 and ω_2, as shown in (7) and (8) at the bottom of the page. By selectively choosing $\omega_1 < \sqrt{1/L_g C_{\rm gs}}$ and $\omega_2 > \sqrt{1/L_g C_{\rm gs}}$, the resistance of $(1-\omega^2 L_g C_{\rm gs})/(g_m)$ is positive at ω_1, which loads the tank to decrease the overall tank impedance, while the resistance of $(1-\omega^2 L_g C_{\rm gs})/(g_m)$ at ω_2 becomes negative to boost the overall tank impedance. Fig. 6 shows the simulated impedance of the combined tank. The lower resonant frequency leads to a lower tank impedance due to the extra loading from FSNR tank, as presented in Fig. 4(a). The higher resonant frequency leads to a higher impedance due to the FSNR tank's negative resistance at that frequency, shown in Fig. 4(b).

The lower frequency oscillation at ω_1, is unsustainable due to its low tank impedance and low gain, and the higher frequency oscillation at ω_2 can be sustained due to its relatively high impedance and high gain. The combined tank oscillation frequency is higher than either $\sqrt{1/L_g C_{\rm gs}}$ or $\sqrt{1/L_{\rm tank} C_{\rm tank}}$ as shown in Fig. 6, which is clear by comparing its resonant frequency (~230 GHz in Fig. 6) with that of the individual FSNR tank (~140 GHz in Fig. 4(c)) and cross-coupled tank (~160 GHz). If not combined with the cross-coupled tank, the individual FSNR tank becomes a regular oscillator and can only oscillate at low frequencies. Similarly, the individual cross-coupled tank also only oscillates at lower frequencies without the FSNR tank.

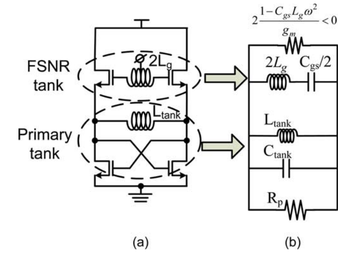


Fig. 7. (a) Constructed THz differential oscillator with FSNR tank. (b) Its equivalent tank models.

C. Proposed CMOS THz Oscillator With FSNR Tank

We propose integrating the FSNR tank and the conventional cross coupled pair to construct a new differential THz oscillator configuration, as shown in Fig. 7(a). Fig. 7(b) reveals the equivalent tank model for both primary (i.e., cross-couple) and FSNR tanks. The combined oscillation frequency can be analyzed using the procedure described by the fourth-order LC tank in Fig. 5. Its overall frequency is boosted higher than the primary tank resonant frequency $\sqrt{1/L_{\rm tank} C_{\rm tank}}$ and the FSNR tank resonant frequency $\sqrt{1/L_g C_{\rm gs}}$.

The major advantages of the proposed THz structure are as follows.

- Combining a FSNR with the primary tank boosts the resonant frequency higher than either of the individual tank resonant frequencies. This allows for a larger inductance values of $L_{\rm tank}$ and L_g, which not only generates a larger tank impedance for higher gain, but also renders on-chip inductor design more flexible and producible than typical super-small inductors in the THz frequency regime.
- The FSNR tank provides negative resistance at the desired high resonant frequency, which ensures a high operating frequency. The additional negative resistance also relaxes a high transconductance g_m requirement of the core circuit device, which allows a smaller device size to further boost the operation frequency and reduce the power consumption.
- A vertical stacking structure allows a higher supply voltage without reliability concerns and increases the signal swing. It also offers current sharing to save the DC power consumption.

After raising the fundamental oscillation frequency by using FSNR, we can further push for higher frequency generation by utilizing higher (fourth) order harmonics through a double push-pull structure, as shown in Fig. 8. The proposed circuit couples two differential oscillators into quadrature phases to

$$\omega_1 = \pm\sqrt{\frac{L_{\rm tank}C_{\rm tank} + L_g C_{\rm gs} + L_{\rm tank}C_{\rm gs} - \sqrt{(L_{\rm tank}C_{\rm tank} + L_g C_{\rm gs} + L_{\rm tank}C_{\rm gs})^2 - 4L_{\rm tank}C_{\rm tank}L_g C_{\rm gs}}}{2L_{\rm tank}C_{\rm tank}L_g C_{\rm gs}}} \tag{7}$$

$$\omega_2 = \pm\sqrt{\frac{\mathrm{L_{tank}C_{tank} + L_g C_{gs} + L_{tank}C_{gs}} + \sqrt{(\mathrm{L_{tank}C_{tank} + L_g C_{gs} + L_{tank}C_{gs}})^2 - 4\mathrm{L_{tank}C_{tank}L_g C_{gs}}}}{2\mathrm{L_{tank}C_{tank}L_g C_{gs}}}} \tag{8}$$

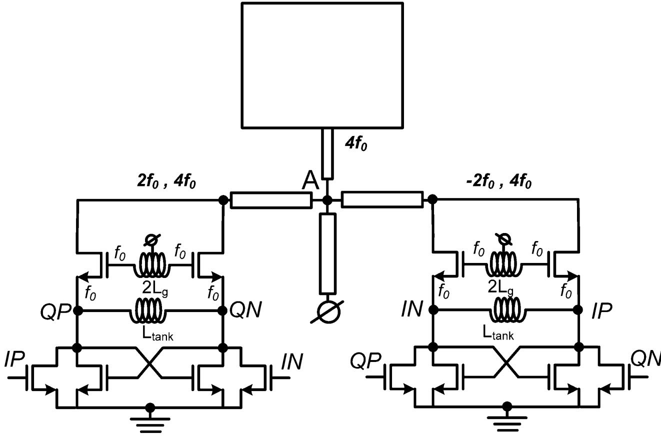


Fig. 8. Proposed fourth-order harmonic boosted oscillator structure with FSNR tank.

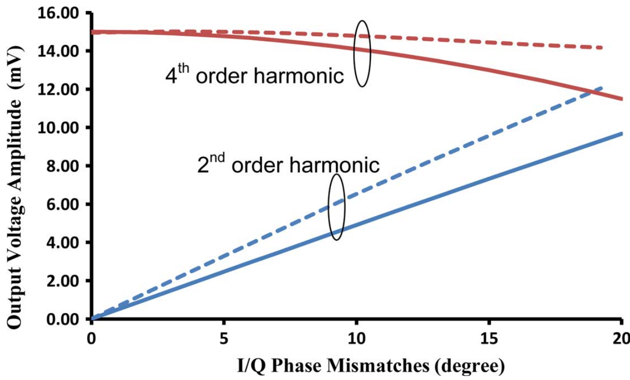


Fig. 9. Output voltage amplitude versus IQ phase mismatches from both analytical (solid lines) and simulation results (dot lines).

form I/Q paths. The gate and source of the cascode device have large signal swings at the fundamental frequency f_0. The cascode devices concurrently provide both frequency selective negative resistances and mixing functions to generate output signals at the drain, where the large signal operation induces circuit nonlinearity to generate higher order harmonic terms: $2\mathrm{f}_0, 3\mathrm{f}_0, 4\mathrm{f}_0$.

Theoretically, only the fourth-order harmonic is constructed at the common-mode output node A. However, due to mismatches, especially I/Q mismatches, the second-order harmonic cannot be suppressed completely and will reduce the fourth-order harmonic output. Fig. 9 compares the output voltage amplitude at node A for both second- and fourth-order harmonics versus I/Q phase mismatches from both simulated and analyzed results based on (1)–(4). The two results agree well. The small discrepancy between the two comes mostly from the amplitude mismatch that is automatically taken into account by simulations, but not included analytically for simplicity.

IV. Design Considerations

THz operation imposes stringent constraints on design and device size options. To simplify the analysis, we focus on the higher resonant frequency operation, where the FSNR can be represented by L_{eq} in parallel with the negative resistance $2(1-\omega^2 L_g C_{\mathrm{gs}})/(g_m)$, similar to that shown in Fig. 4(b). Thus, the ultimate resonant frequency, $1/\sqrt{(L_{\mathrm{eq}}//L_{\mathrm{tank}})C_{\mathrm{tank}}}$, determines the size of the bottom cross-coupled active devices ($\mathrm{M_b}$), which must meet the requirements

$$\frac{w_b l C_{\mathrm{ox}}}{2} + C_p = C_{\mathbf{tank}} = \frac{1}{\omega_N^2 (L_{\mathrm{eq}}//L_{\mathbf{tank}})}$$
$$\frac{w_b l C_{\mathrm{ox}}}{2} < \frac{1}{\omega_N^2 (L_{\mathrm{eq}}//L_{\mathbf{tank}})} \tag{9}$$

where w_b is the bottom device width, l is the channel length, which is the feature size for all the core active devices; ω_N is the target operation frequency, C_{ox} is the unit gate oxide capacitance and C_p stands for the parasitic capacitance inside the tank. The bottom cross-coupled devices need to generate sufficient negative resistance. Its equivalent transconductance g_{m_b} must be large enough to provide gain higher than one, i.e., $g_{m_b}/2 > (1/R_p)$. The transistor g_{m_b} at high frequencies can be approximately modeled as $g_{m_b0} - j\omega C_{\mathrm{gd}}$ [19], where g_{m_b0} stands for the transistor transconductance at low frequencies and C_{gd} is the device gate to drain capacitance. Because only the real part contributes the required negative impedance to support oscillation, we can derive the following equation to address the bottom device sizing with the first order CMOS square law model

$$(w_b/l) = \frac{g_{m_b}^2}{2I\mu_n C_{\mathrm{ox}}} > \frac{4}{2R_p^2 I \mu_n C_{\mathrm{ox}}} \tag{10}$$

whereR_p is the primary tank parallel impedance, I is the bias current and $\mu_n$is the device mobility.

By combining (9) and (10), the bottom device width w_b has to meet the requirements

$$\frac{4l}{2R_p^2 I\mu_n C_{\mathrm{ox}}} < w_b < \frac{2}{\omega_N^2 (L_{\mathrm{eq}}//L_{\mathrm{tank}}) l C_{\mathrm{ox}}}. \tag{11}$$

The constraints on the top cascode device in the FSNR tank can be interpreted in a similar approach. First, to facilitate oscillation, it is necessary that $\omega_N > \sqrt{1/(L_g C_{\mathrm{gs_t}})}$ for negative resistance from the FSNR tank, therefore

$$w_t l C_{\mathrm{ox}} > 1\big/\big(\omega_N^2 L_g\big) \tag{12}$$

where w_t is the top cascode device width and L_g is half of the gate inductance. To achieve high frequency operation, the device must be sized to provide sufficient negative impedance to boost oscillation gain, or

$$\left|2\frac{1 - C_{\mathrm{gs_t}} L_g \omega_N^2}{g_{m_t}}\right| < \left|-2\frac{C_{\mathrm{gs_t}} L_g \omega_N^2}{g_{m_t}}\right| < R_p. \tag{13}$$

By combining (12) and (13), the top cascode device width w_t has to satisfy

$$\frac{1}{(\omega_N^2 L_g)\, l C_{\mathrm{ox}}} < w_t < \left(\frac{R_p}{\omega_N^2 L_g}\sqrt{\frac{I\mu_n}{2l^3 C_{\mathrm{ox}}}}\right)^2. \tag{14}$$

Equations (11) and (14) provide design insights in sizing the bottom and top devices. Equations (9) and (12) constrain the device size based on overall tank resonant frequency and FSNR tank negative resistance frequency requirement. We apply the lumped model analysis since the wavelength at 200 GHz (about

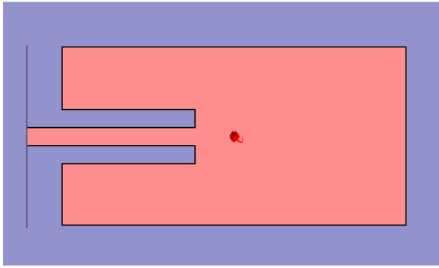


Fig. 10. On-chip half wavelength patch antenna.

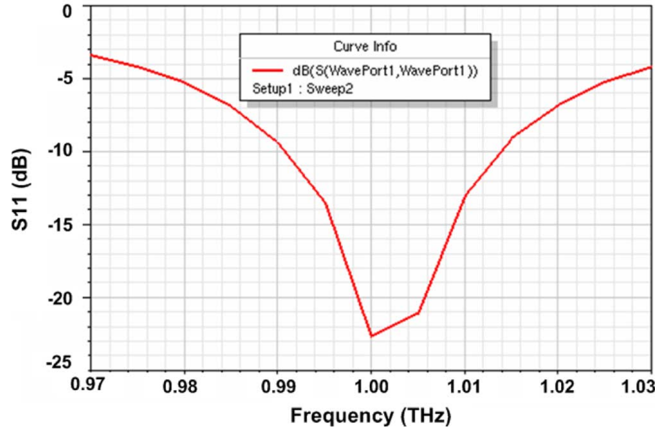


Fig. 11. Simulated antenna −3 dB bandwidth of 60 GHz, from 0.97 THz to 1.03 THz.

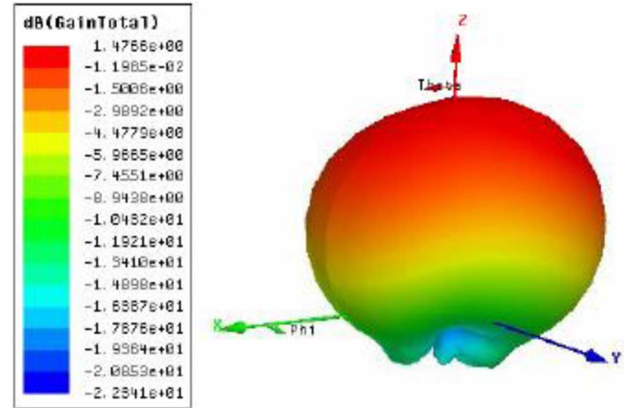


Fig. 12. Simulated antenna far field radiation pattern.

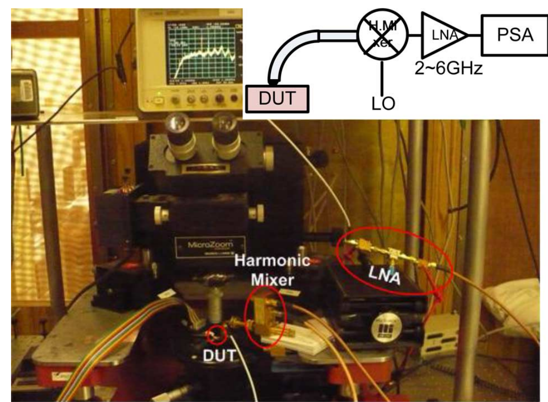


Fig. 13. Setup to identify fundamental signal frequency with an external high-order harmonic mixer.

600 μm on silicon) is still one order larger than the passive device size (on the order of 10 μm). Equations (10) and (13) are derived based on oscillation gain requirement, which are approximations based upon a simple model at such high frequencies. This only provides a first order estimation to size the transistor initially and we do need to rely on simulation tools to take into account higher order effects and parasitics at such high operation frequencies for more accurate circuit optimization.

V. Antenna Design

A compact and efficient on-chip antenna structure is preferred in THz design to avoid complicated packaging and assembly. Dipole antenna structures are adopted in [20] and [21], which are area-efficient with relative wide bandwidth. Normally, a dipole antenna must be directly fabricated on top of silicon without any metal underneath. However, coupling losses induced by a silicon substrate severely degrade the dipole antenna efficiency and effective radiation power, which may prevent on-chip dipole antennas from being practical. A microstrip patch antenna, another type of compact and conformal design, is adopted due to its suitable features. First, the lower ground metal can reduce the substrate coupling and loss. Second, the small wavelength at THz makes the patch size suitable for on-chip implementation. Third, the height of patch antenna to ground is a reasonable fraction of wavelength to provide a reasonable bandwidth. The half-wavelength patch antenna structure is shown in Fig. 10. The antenna size is 68 um$\times$45 μm, where the top metal is used to form the patch. The bottom two layers, M1 and M2, provide a low impedance ground to reduce current return loss. The full-wave simulation results from HFSS indicate an −3 dB bandwidth of 60 GHz at 1 THz, as shown in Fig. 11. Fig. 12 shows its 3D far-field radiation pattern with the 3 dB beamwidth of 80o and 92o, in the H- and E-planes, respectively. This antenna is designed to radiate out the generated THz signal with 1.5 dBi gain.

VI. Measurement Results

The designed THz generator was fabricated with TSMC 65 nm CMOS technology. To characterize its fundamental oscillation frequency, we built a separate differential oscillator test chip for wafer probe testing. Fig. 13 shows the setup to measure the fundamental oscillation frequency. By shifting the LO frequency and measuring the corresponding frequency shift at the IF, as shown in Fig. 14, we can calculate the fundamental oscillation frequency. As LO shifts by 5 MHz, the measured IF shifts by 105 MHz. This indicates that the LO's 21st harmonic (i.e., $21 \times 10.924 = 229.404$ GHz) has been utilized to downconvert the fundamental signal at 225.006 GHz to the IF at 4.398 GHz. Compared with the simulated 232 GHz oscillation frequency, the measurement shows a slightly lower oscillation frequency possibly introduced by inaccurate modeling of the inductors and device parasitic extractions.

Because of large losses, the measured signal from the spectrum analyzer is only about 4 dB higher than the noise floor, which hinders a reliable phase noise measurement. Instead, a simulated phase noise vs. offset frequency of the fundamental

Fig. 14. Fundamental oscillation frequency identified by using high-order (21st) harmonic mixing. 5 MHz shift of LO versus 105 MHz shift of mixer IF suggests the fundamental signal (225.006 GHz) being mixed by the 21st harmonic LO (229.404 GHz or 229.509 GHz) to generate the IF at 4.398 GHz or 4.503 GHz, respectively.

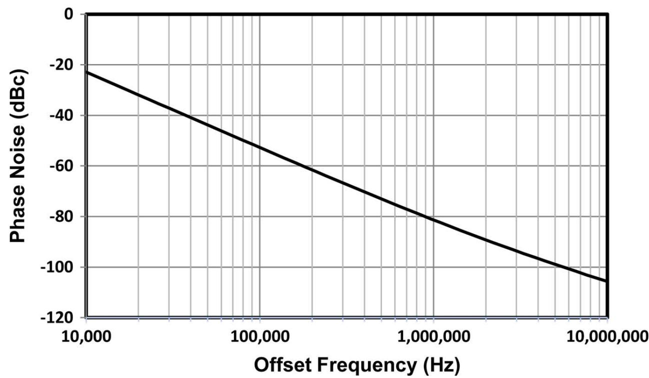


Fig. 15. Simulated fundamental frequency signal phase noise.

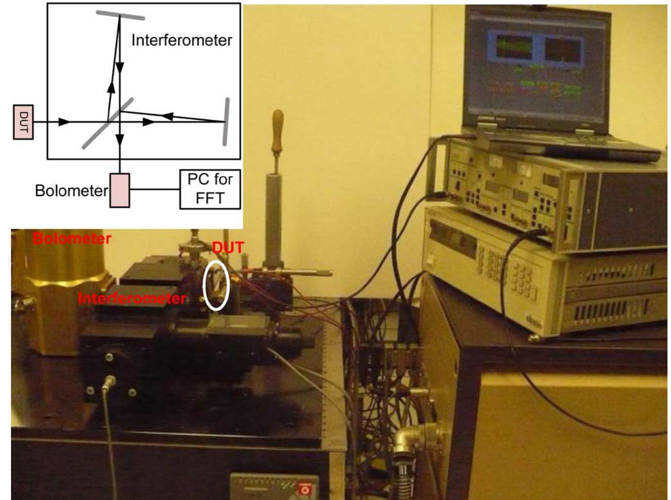


Fig. 16. Michelson interferometer to measure the THz oscillator.

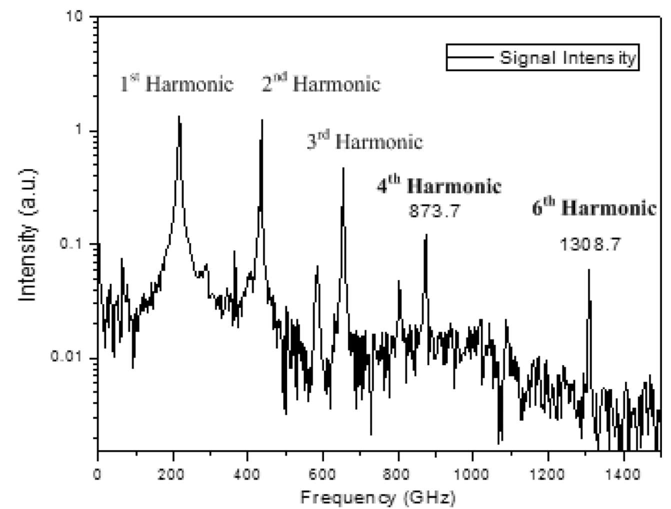


Fig. 17. Measured signal spectrum through Michelson interferometer.

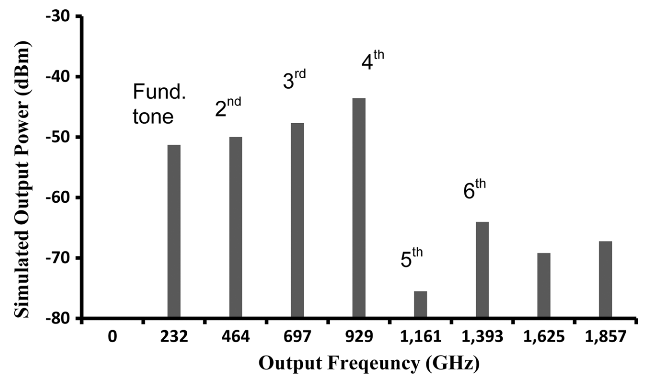


Fig. 18. Simulated output power versus different harmonics, which indicates noticeable differential and quadrature mismatches.

frequency signal is shown in Fig. 15, which shows a phase noise of about −81 dBc/Hz @ 1 MHz offset.

A conventional electronic apparatus is not suitable for identifying high order harmonic frequencies in the terahertz frequency range. To overcome this obstacle, a Michelson interferometer based quasi-optical measurement approach is adopted. As shown in Fig. 16, the output signal, radiating from the vertically mounted CMOS oscillator with an on-chip patch antenna, is detected through an interferometer, followed by a bolometer. The signal spectrum is then recovered through the FFT, as shown in Fig. 17. The measurement results were consistent for several chips.

In addition to the desired fourth-order harmonic, other harmonics are also present in the measured spectrum. The second- and sixth-order harmonics are introduced mainly due to the quadrature signal mismatches. The fundamental tone and third harmonic are observed, which may radiate from the oscillator inductor or be introduced by the differential phase and amplitude mismatches. Similar observations were revealed with post-layout simulation results, as shown in Fig. 18. The results indicate that ultrahigh frequency circuits, such as the intended one in THz frequency range, are extremely sensitive to device/circuit parameter mismatches.

It is worth noting that the power measurement results used an un-calibrated Michelson interferometer. Therefore, the strengths of higher harmonics (4th and 6th harmonics at 0.87 and 1.31 THz, respectively) may be substantially underestimated due to excessive water and oxygen absorption and setup losses. In order to achieve accurate power profiles at different

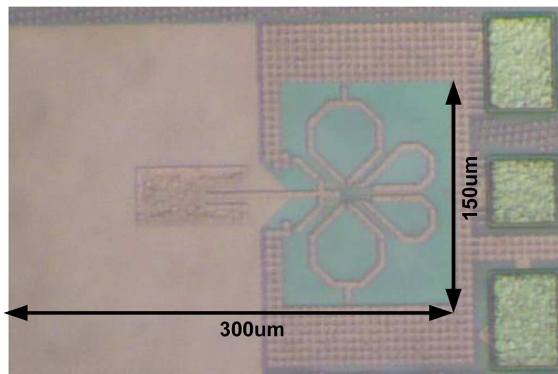


Fig. 19. Die photo of the proposed terahertz oscillator with on-chip antenna in 65 nm CMOS.

TABLE I
COMPARISON WITH STATE-OF-THE-ARTS CMOS MM/SUB-MM WAVE OSCILLATORS

	Huang [11], JSSC 2008	Seok [12], JSSC 2010	Razavi [13], JSSC 2011	This work
Technology	90nm CMOS	45nm CMOS	65nm CMOS	65nm CMOS
Fundamental Frequency	81 GHz	205 GHz	300 GHz	217 GHz
Output Frequency	4th order: 324 GHz	2nd order: 410 GHz	2nd order: 600 GHz	4th ode:r 0.87 THz, 6th order: 1.31 THz
Output Power	-46 dBm	-49 dBm	N/A	N/A
Power Consumption	19.2 mW**	16.5 mW*	3.5 mW*	16.8 mW**
On-Chip Antenna	No	Yes	No	Yes

* differential oscillator power consumption
** quadrature oscillator power consumption

frequencies, the blackbody-based calibration can be conducted. The oscillator draws 12 mA current from a 1.4 V power supply and occupies 0.045 mm^2 area. The die photo is shown in Fig. 19.

Table I compares recently reported mm/sub-mm wave oscillators in CMOS technologies. According to the table, we demonstrate the highest output frequency (1.31 THz) with integrated on-chip antenna.

VII. CONCLUSION

In summary, this paper has presented a new technique using FSNR tank to increase the output of circuits beyond the device cut-off frequencies. With the FSNR technique and double push pull structure, we have successfully demonstrated a CMOS THz oscillator, with the measured output signals at the 4th harmonic of 0.87 THz. With further circuit optimization and parasitic reduction, this new technique may produce useful outputs at frequencies above 1 THz.

ACKNOWLEDGMENT

The authors thank TSMC for its excellent 65 nm CMOS foundry support.

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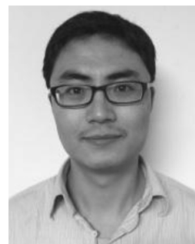

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pumping and Stark tuning of the two photon pumping of vibrational levels. In the field of detectors, he was a pioneer in the development of quasi-optical Schottky "corner cube" receivers and their local oscillators at submillimeter frequencies. This stimulated his participation in fields ranging from high frequency radio astronomy, frequency standards, plasma diagnostics, millimeter wave modeling to new high power, millimeter wave tubes. Since leaving Lincoln Laboratory, he has devoted his efforts to investigating new solid state devices. This includes FETs, HEMTs, HBTs, quantum well structures, and traveling-wave transistor structures. During this period he was one of the founders of the highly respected Millitech Corporation. In 1982, he joined the UCLA EE Department as a Professor and served as the first Director of the Center for High Frequency Electronics. As part of the Center, he initiated programs in monolithic millimeter wave devices, six port network analyzers for high frequency applications, and millimeter wave imaging with detector arrays. From 1986 to 1989, he was Associate Dean for Research in the School of Engineering, UCLA. During this period, he also became active in studying high temperature superconducting devices and millimeter wave phase conjugation using artificial Kerr materials. Currently, he has programs in investigating new millimeter wave device concepts and novel means of high frequency testing using laser techniques. He has concentrated on combining high frequency structures and systems with optical devices. These efforts include cw optical mixing experiments using three terminal devices, high speed polymer optical modulators and traveling wave photodetectors which are now being extended to over 200 GHz. Some of these devices have been incorporated into novel systems such as optically controlled phased array radars and more recently, new forms of optical A-to-Ds.

Dr. Fetterman is a Fellow of the Optical Society of America (OSA).