A D-Band Passive Imager in 65 nm CMOS

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***Abstract*—Adifferential D-band (140 GHz) passive imager has been demonstrated in a 65 nm CMOS technology. It achieves a minimum noise equivalent power of 26 $\mathrm{fW}/\sqrt{\mathrm{Hz}}$ with peak responsivity of 1.2 MV/W. The core circuit consumes chip area of $950 \times 240\ \mu\mathrm{m}^2$ with dc power consumption of 152 mW. This work further pushes imagers in CMOS technology working towards higher millimeter wave/sub millimeter wave frequencies.**

***Index Terms*—CMOS, d-band, detector, passive Imager.**

I. Introduction

THE millimeter/sub-millimeter wave signal is unique in its capability to penetrate fabric and detect concealed objects [1]. Passive imaging is particularly attractive due to its inherent advantages: it requires neither dedicated illumination sources nor compliance with FCC regulation.

Conventional III-V technology based mm/sub-mm wave systems may not be suitable for future small form factor systems due to their limited integration scale. On the contrary, silicon based approaches become more attractive due to their large-scale integration and powerful on-chip digital signal processing capabilities. A few W-band silicon-based passive imaging systems have been demonstrated [2]–[5]. To further advance the state of the art, we realize a D-band (140 GHz) passive imager in a 65 nm CMOS technology. Compared with our previous work at W-band [5], it not only provides better spatial and cross-range resolution, but also offers better performance including lower noise equivalent power (NEP) and higher responsivity. Accordingly, it renders the passive imager with a faster response time and finer noise equivalent temperature difference (NETD).

II. System Description

Passive imagers detect extremely small thermal noise level ($\sim \mathrm{KT}$) signals to construct images and require excellent detector sensitivity. There are two typical detector implementations, coherent and non-coherent detectors [6]. Coherent detection normally provides higher gain and faster response. However, it mandates sophisticated local oscillators (LO) generation, which is very challenging in ultra high frequency systems. To simplify the system, one non-coherent detection, total power detection is widely adopted in mm-wave passive imagers due to the elimination of LO generation. Since it only processes the input signal power level, the total power detection does not need the signal phase information. A typical approach is using square-law devices to measure the total power of input signals. Silicon square-law detectors can be built with normal active devices, such as MOS, bipolar, or diode [7]. However, the performances of silicon square-law detectors are normally poor, with the responsivity of $< 1\ \mathrm{KV/W}$ and the noise equivalent power NEP of $> 10\ \mathrm{pW/sqrt(Hz)}$ [7], [8]. To achieve a good responsivity and acceptable NEP necessitate slow noise amplifiers (LNA) in the front. Although LNA provides high gain and low noise figure performance, its gain often drifts due to device flicker (1/f) noise, environment and supply voltage changes. TheLNA gain variation may result in poor imager performance due to a long integration time for passive imagers, hence necessitates calibrations. Electronic Dicke switching and mechanical chopping are two typical calibration approaches. For a highly integrated and fast system, integrated electronic Dicke switching is preferred due to its faster response. In this letter, we present a differential non-coherent D-band passive imager with an integrated electronic Dicke switch in a 65 nm CMOS technology. The circuit architecture is shown in Fig. 1, consisting of an integrated Dicke switch, a balun, a D-band LNA, a detector and an on-chip first-order low pass filter.

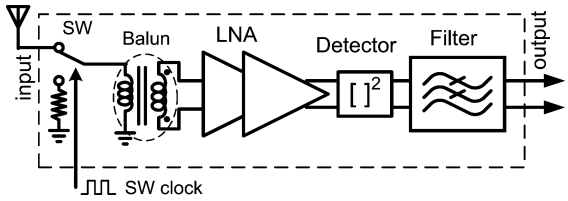

Fig. 1. D-band CMOS passive imaging structure.

III. Design Approaches

Since D-band frequency is approaching 65 nm CMOS device cutoff frequencies, it imposes great challenges on device design and optimization. Fig. 2(a) left shows the RF device layout provided by the foundry, which utilizes double gate connections. The corresponding RF device model is extracted from this layout. Fig. 2(a) right presents the simulated maximum available gain (MAG) and minimum noise figure (NF) of a NMOS device based on the foundry provided RF model. It also gives the performance comparison between the RF model and the digital model from the foundry without parasitics. The device size is $20\ \mu\mathrm{m}/60\ \mathrm{nm}$ for this simulation. When using digital model, simulation shows $\mathrm{MAG} = 8.8\ \mathrm{dB}$ and minimum $\mathrm{NF} = 1\ \mathrm{dB}$ at 140 GHz. When applying to the RF model, the device performances are degraded to $\mathrm{MAG} = 4\ \mathrm{dB}$ and minimum $\mathrm{NF} = 3.7\ \mathrm{dB}$, respectively. Such differences show significant device performance degradation from the RF model. This is most likely due to the high parasitics involved with double gate connections,

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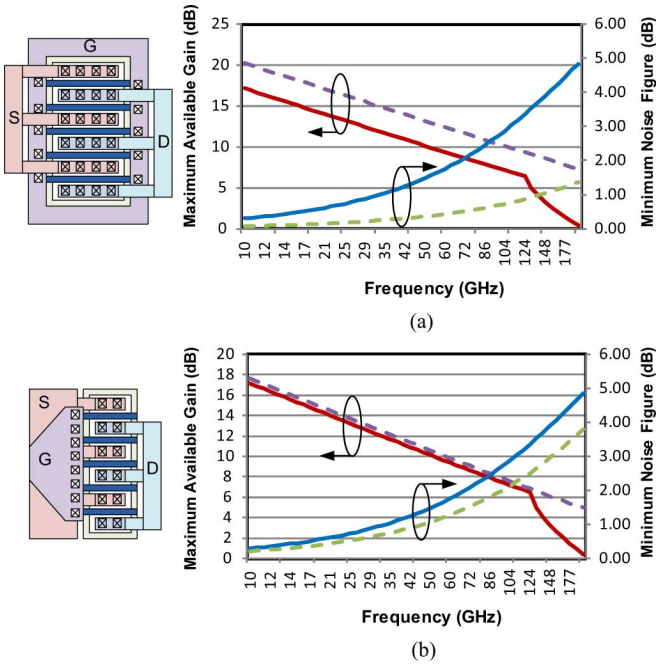


Fig. 2. (a) Simulated MAG and minimum NF for both core digital device (dash line) and RF device provided by foundry (solid line) (b) Simulated MAG and minimum NF for the layout-optimized device (dash line) in comparison with RF device from foundry (solid line).

such as Cgd and Cgs. And this type of RF device layout may not be optimized for D-band operations.

To improve performance, we customize the active device design by trading-off device channel width and finger number. Then, we extract the device interconnect parasitics by simulation with EM tools (both HFSS and ADS Momentum), and obtain the device gate and contact parasitics through extraction tools, e.g., Caliber. Subsequently, we incorporate these parasitics together with the digital model provided by the foundry to build the corresponding device model in D-band frequency. Simulation indicates single gate connection with smaller finger width may achieve better performance, which also simplifies interconnections, as shown in Fig. 2(b) left. Fig. 2(b) right presents the simulated MAG and minimum NF from the optimized NMOSdevice with an identical size and the comparison to the results of the foundry provided RF device. The customized device achieves 2.8 dB minimum NF at 140 GHz, about 1 dB better than that of the foundry provided RF device. Its MAG shows more improvement with the increase of frequency, e.g., MAG is 6.4 dB at 140 GHz and about 2.7 dB higher than that of the foundry provided RF device.

Besides active device optimization, differential circuit architecture is also crucial for higher immunity to supply/ground noises and undesired couplings, which will otherwise contaminate extremely weak blackbody radiation input signal. However, single ended I/Os are adopted to facilitate the testing, especially for the input side, because it is extremely challenging to obtain fully differential D-band signals. To achieve so, a balun is employed to interface with single-ended I/Os, and requires high coupling coefficient and low loss for low noise front-end. The 65 nm CMOS process we used has 6 metal layers with a nultra-thick top metal of $3.4\ \mu\mathrm{m}$ thickness. A lateral coupling, one layer balun using top ultra-thick metal with turns ratio of

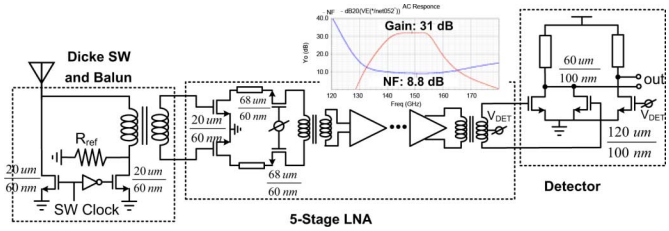


Fig. 3. D-band passive imager schematic in 65 nm CMOS technology and simulated LNA performance (inset).

about 1:1 proves to be a good option for a low-loss design. At 140 GHz, the simulated (by HFSS) coupling coefficient is about 0.5 and the insertion loss is around 1 dB. The balun is also incorporated for input impedance matching.

A 1:1 turns ratio also reduces input resistance of LNA by half, which helps to maintain LNA noise performance with less sensitivity to process variations [5], [9]. The D-band LNA is fully differential with 5 stages coupled through compact transformers, which are also based on lateral coupling structures similar to the input balun. The CMOS Dicke switch adopts similar structure in [5] by avoiding switches along the signal path to minimize insertion loss. The simulated insertion loss is about 1.2 dB at 140 GHz. The square law detector features pseudo-differential structure and is biased at the transition point of sub-threshold and saturation regions for maximum gain performance [5]. The passive imager front end schematic is shown in Fig. 3. The simulated LNA performance is presented in the inset with the gain of 31 dB and NF of 8.8 dB.

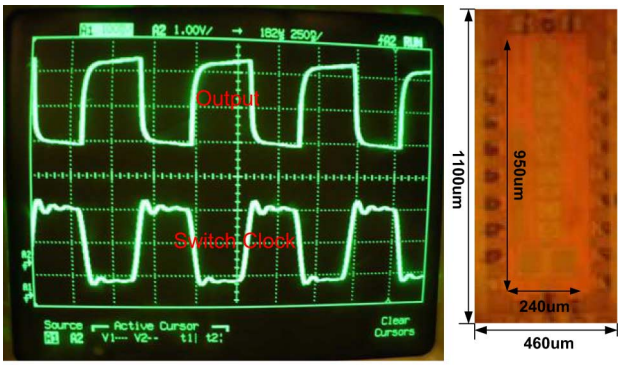
IV. Measurement Results

D-band measurement is challenging due to high frequency inputs. An active multiplier chain (AMC) from VDI generates a D-band signal, which passes through an external attenuator to feed into the chip. The attenuator provides 50 dB dynamic range and adjusts the input signal strength to facilitate the characterization. An oscilloscope is used to measure the D-band imager responsivity. A spectrum analyzer is then used to measure the imager output noise.

Fig. 4(a) presents the output and Dicke switch clock waveforms with the imager output on the top and the switch clock at the bottom. The switch clock troughs correspond to signal detection cycles, and the switch clock peaks align with reference calibration cycles. Fig. 4(b) shows the die photo, which occupies $0.506\ \mathrm{mm}^2$ and $0.228\ \mathrm{mm}^2$ chip area with and without pads, respectively. The overall power consumption is 152 mW with 2 V supply for LNA and 1 V supply for the rest of the circuits.

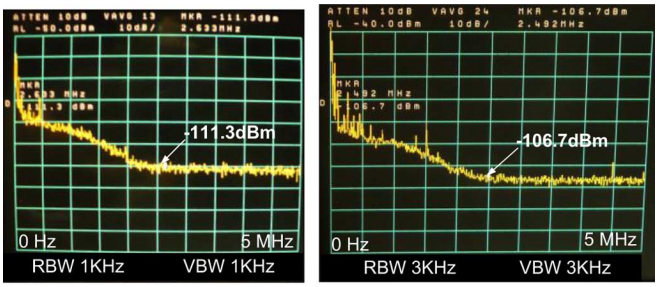
Fig. 5(a) and (b) present the measured output noise without and with Dicke switch, respectively. To calibrate most of the flicker noise, Dicke switch clock frequency must be higher than the flicker noise corner frequency. The subsequent low pass filter and DSP will process the signal and calibrate out the majority flicker noise. Measurement shows that when the frequency is higher than 2.5 MHz, the output noise is dominated by white noise. We measure the output noise at about 2.6 MHz. Based on Fig. 5, the measured output noises are equivalent to $27.2\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ and $27\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ for without and with Dicke switch cases.

Fig. 6 presents the measured responsivity and NEP with Dicke switch and compares them with simulated results.



(a) (b)

Fig. 4. (a) Measured output waveform together with dicke switch clock at 1.5 MHz (b) Die photo of the 140 GHz imager in 65 nm CMOS technology.



(a) (b)

Fig. 5. Measured output noise (a) Without Dicke switch, and (b) With Dicke switch.

$$NETD = 2 \times \frac{NEP}{kB\sqrt{2\tau}} \quad (1)$$

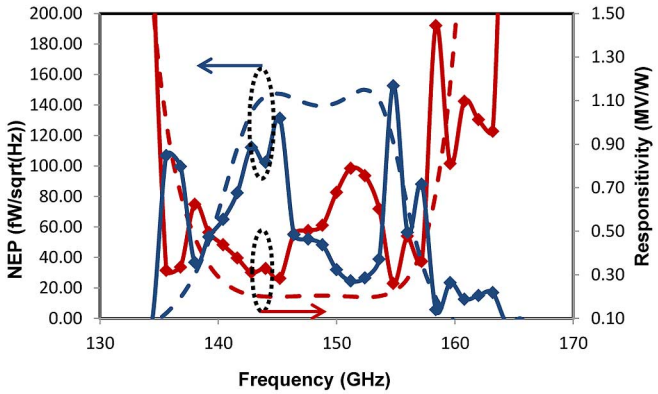


Fig. 6. Measured and simulated responsivity and NEP with dicke switch, where measurement results are indicated by solid lines and simulation results are represented by dash lines.

Simulation and measurement results agree with each other in the general trend. However, measurement results show much larger variations, which could be led by unexpected couplings among LNA stages. Measurement result demonstrates the peak responsivity of 1.2 MV/W, with responsivity larger than 300 KV/W over the frequency range from 136 to 157 GHz. The measured minimum NEP is 26 $\mathrm{fW}/\sqrt{\mathrm{Hz}}$. The average NEP is 53 $\mathrm{fW}/\sqrt{\mathrm{Hz}}$ over the frequency range from 136 to 157 GHz. From (1) [2], the equivalent NETD is about 1.5 K with 30 ms integration time which corresponds to a 33 Hz pixel frame rate

$$NETD = 2 \times \frac{NEP}{kB\sqrt{2\tau}}. \quad (1)$$

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART

	Ref.[2]	Ref.[3]	Ref.[4]	this work
Technology	0.12um SiGe	65nm CMOS	0.18um SiGe	65nm CMOS
Frequency (GHz)	90	90	94	140
NEP	21 fW/$\sqrt{HZ}$	111 fW/$\sqrt{HZ}$	N/A	53 fW/$\sqrt{HZ}$
Responsivity	2.5~5 MV/W	63 kV/M	63 kV/M	600 KV/W
NETD with τ=30ms	0.83 K	12.5 K	0.4 K	1.5 K
Power	35 mW	38 mW	200 mW	152 mW

Table I summarizes the demonstrated D-band passive imager performance and the comparison with state-of-the-art silicon based high frequency passive imagers.

V. CONCLUSION

This work has realized a CMOS D-band passive imager front-end with an integrated Dicke switch. Over the frequency range of 136 to 157 GHz, the measured minimum and average NEPs are 26 $\mathrm{fW}/\sqrt{\mathrm{Hz}}$ and 53 $\mathrm{fW}/\sqrt{\mathrm{Hz}}$, respectively. The measured peak/average responsivities are 1.2 MV/W and 600 KV/W, respectively. The corresponding NETD in 30 ms integration time is about 1.5 K. This work further pushes the applicability of CMOS technology for portable passive mm-wave imaging systems with small form-factor, high resolution and low power operation.

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