A CMOS Integrated W-band Passive Imager

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***Abstract*—This brief presents an integrated W-band passive imager, including a low-noise amplifier, a Dicke switch, a detector, a low-pass filter, a programmable-gain amplifier, and a 10-bit 20-MHz pipeline analog-to-digital converter (ADC). With digital outputs, the imager is ready to be interfaced with a digital signal processor to complete its system implementation. The chip is realized in a 65-nm CMOS technology. The measured average noise-equivalent power and responsivity are 32 fW/$\sqrt{\text{Hz}}$ and 103 MV/W, respectively, which represents a noise-equivalent temperature difference of 1.0 K with 30-ms integration time. The integrated imager occupies a silicon area of 1.17 mm^2 and burns 151 mW of power. To the authors' best knowledge, this is the first time that a millimeter-wave passive imager is integrated with an on-chip ADC to generate digital outputs.**

***Index Terms*—Analog-to-digital converter (ADC), CMOS, passive imager, W-band.**

I. Introduction

MILLIMETER-WAVE imaging provides high promises in many applications due to its unique capabilities of penetrating through obstacles, seeing through fog, etc. Passive millimeter-wave imaging is of particular importance because it does not need high-power sources/illuminators. Therefore, it not only simplifies system design without power-hungry millimeter-wave transmitters but also automatically complies with the Federal Communications Commission and other regulations to facilitate wide deployments. However, passive imagers often impose substantial challenges for high receiver (Rx) sensitivity to detect small blackbody radiation. Therefore, III–V processes are usually utilized for better Rx noise performance [1], [2], which however leads to relatively large form factors and high cost due to their discrete implementations.

To achieve high integration with a smaller form factor for cost-effective deployments, silicon-based processes are most desirable. Several silicon-based passive imagers at W-band have been demonstrated. In SiGe technologies, May and Rebeiz [3] and Gilreath *et al.* [4] have demonstrated W-band passive imagers with a noise-equivalent power (NEP) as low as several tens of fW/$\sqrt{\text{Hz}}$ and a noise-equivalent temperature difference (NETD) of less than 1 K with 30-ms integration time. Tomkins *et al.* [5] have demonstrated a W-band passive imager on a 65-nm CMOS technology with a performance comparable to those of the SiGe counterparts. A D-band passive imager has also been recently demonstrated in silicon processes [6]. With these advancements, now it is the time to investigate an integrated passive imager.

As the first step to realize a passive imager system-on-a-chip (SoC), we integrate a radio frequency (RF) and analog front end together with a 10-bit pipeline analog-to-digital converter (ADC) to generate digital outputs for subsequent digital signal processing. To the authors' best knowledge, this is the first time that an ADC has been integrated with a passive imager front end, which opens the door for comprehensive digital signal processing to further improve the imaging quality. This integrated imager is realized in a standard 65-nm bulk CMOS technology.

II. System Description

A. Passive Imager Architecture

Passive imagers aim to detect extremely weak blackbody radiation and therefore demand excellent sensitivity on the Rx. One of the most critical metrics of passive imagers is their NETD, which determines their temperature resolution and can be represented as [7]

$$\text{NETD}=\sqrt{\left(\frac{1}{B\tau}\right)T_{\text{SN}}^2+\left(T_{\text{SN}}\frac{\Delta G}{G}\right)^2+\left(\frac{\text{NEP}_{\text{det}}}{kGB}\right)^2\frac{1}{2\tau}} \tag{1}$$

where B and G are the bandwidth and gain of the RF front end, respectively, τ is the system integration time, ΔG is the front-end gain variation, T_{SN} is the system-noise-equivalent temperature, and NEP_{det} is the NEP of the detector following the front-end low-noise amplifier (LNA). To reduce the response time and integration time τ and improve the imaging temperature resolution, low noise and wide front-end bandwidth are two critical aspects of the Rx. Moreover, the gain variation ΔG is particularly crucial in CMOS technology due to its high flicker noise and sensitivity to the supply voltage and temperature. To minimize gain variation ΔG effects, a Dicke switch Rx [8] is often employed to cancel slow-changing gain variations. The Dicke switch builds two interleaved working cycles: the receiving cycle to sense the input signal from the antenna and the calibration cycle to sense a reference resistor. By subtracting the receiving cycle output from the calibration cycle output, the gain variation can be canceled theoretically. To achieve that, the Dicke switch clock should be faster than the speed of the gain variation, which is normally set by the device flicker noise

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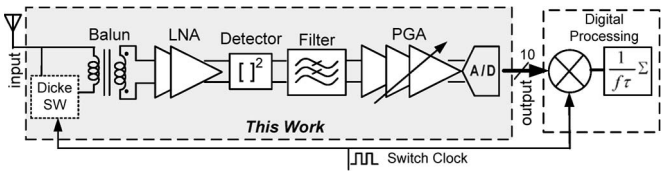

Fig. 1. Integrated W-band CMOS passive imaging with an integrated 10-bit ADC.

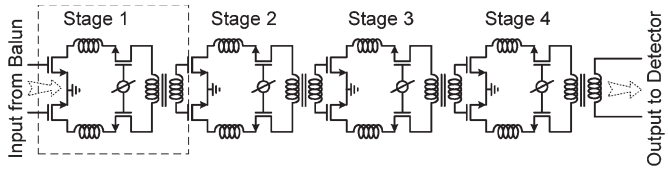

Fig. 2. LNA schematic.

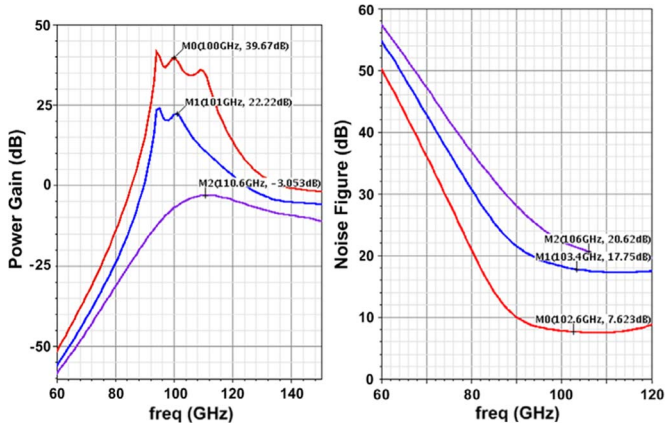

Fig. 3. Simulated LNA gain and noise figure with three different gain settings.

corner frequency. Another important and much more challenging requirement is to balance the resistance of the antenna input and the reference resistance. When there are mismatches between these two resistance values, the calibration residue of gain variation will exist [9]. Therefore, a fully integrated system with on-chip calibration is desired to ensure the match of the two resistance values, in which silicon-based processes hold the highest potential.

As for the imager architecture, there are two options. One is based on analog signal processing, which utilizes analog multipliers and integrators and has the advantage of simplicity. However, the noises, particularly the flicker noises from the analog processing blocks, the analog multiplier and integrator, and the ADC, cannot be calibrated and will limit the ultimate system performance. Therefore, we choose the second architecture, which is based on digital processing and shown in Fig. 1. It consists of an input balun, a differential LNA, a detector, an on-chip Dicke switch, a filter, a programmable-gain amplifier (PGA), and an ADC with the multiplier and integrator to be implemented in a digital fashion. This work has integrated the components up to the ADC. With all the analog and mixed-signal circuits included in the calibration loop, the flicker noises and gain variations can be dramatically suppressed. A digital signal is insensitive to noises; therefore, noises from multipliers and integrators have minimum effects on system performance. To suppress common-mode and supply noises, a fully differential architecture is adopted. The input balun serves as a device for converting single-ended to differential signals as well as an input-matching network.

Dicke-switch-based calibration, together with digital signal processing, such as digital multipliers and integrators, suppresses the gain variation ΔG significantly to be negligible. Therefore, NETD can be represented as [3]

$$\text{NETD} = 2 \times \frac{\text{NEP}}{kB\sqrt{2\tau}}. \tag{2}$$

The factor of two accounts for the fact that only half of the period is used to detect the signal.

The subsequent low-pass filter and PGA are responsible for filtering out the unwanted high-frequency signals and further magnifying the desired low-frequency signal, respectively. Such amplification is necessary to scale up the small blackbody radiation input together with circuit noise into a full-scale large signal to fully utilize the 1-V_{p-p} dynamic range of the following ADC. The ADC quantizes the amplified signal, in which the external blackbody radiation contributes a small portion and the imager circuit noise becomes dominant. The ADC sampling frequency is set about 20 MHz to acquire a wideband signal for digital signal processing to reduce the integration time. This CMOS passive imager chooses an $\sim$1-MHz chopping frequency to calibrate flicker noise and gain variation. After the ADC, the subsequent digital signal processor (DSP) conducts multiplication and integration. The reason for selecting a digital integration structure against an analog integration structure is to fully calibrate device flicker noise, because the flicker noise of analog multipliers and integrators cannot be calibrated. In this brief, we focus on the integrated imager RF/mixed-signal design while leaving out subsequent DSP circuitries.

B. Circuit Design Description

This passive imager adopts the same front-end circuit structure as in [10]. A high-gain four-stage LNA, as shown in Fig. 2, adopts a fully differential structure to facilitate SoC integration due to its high immunity to supply and common-mode noises. Transformer-based interstage coupling and matching lead to a compact implementation. A cascode structure benefits amplifier stability and input/output isolation. Series transmission line stubs serve as a device for intrastage matching of the bottom device and the cascode device to alleviate the parasitic capacitance effect to boost the gain at the cost of chip area. This LNA is designed with three different gain steps, with the simulated gain and noise figure shown in Fig. 3. The maximum gain is about 40 dB and the minimum noise figure is about 7.6 dB.

Before the LNA, an integrated electrical Dicke switch is designed to suppress CMOS flicker noises and gain variations. The Dicke switch consists of an input-matching balun, one reference resistor, and two switches formed by low-threshold voltage n-channel MOSFET transistors, as shown in Fig. 4. The switch demonstrates low insertion loss, about -1.57 dB at 110 GHz, because there are no inserted switches along the signal path. When the Dicke switch clock is low, the Rx detects signals from the outside target. When the Dicke switch clock is high, the Rx detects the equivalent noise from the reference resistor. An envelope detector follows the LNA for power detection. The envelope detector is biased at close to the subthreshold region and demonstrates around-1-kV/W responsivity.

Unlike most communication systems that need to trade off noise and linearity, passive imagers majorly emphasize on noise

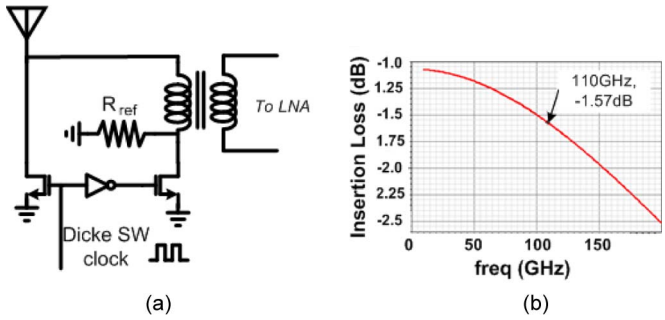

Fig. 4. (a) Dicke switch schematic and (b) simulated insertion loss.

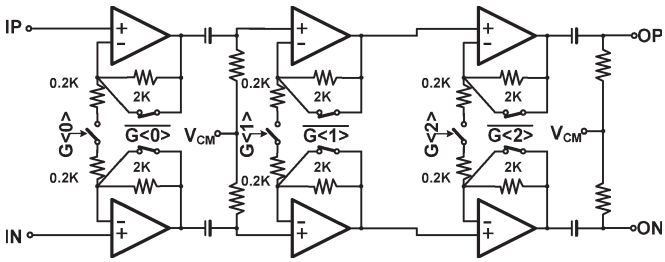

Fig. 5. Op-amp-based noninverting PGA schematic.

performance, which is the most critical circuit specification from the front end toward the end of the Rx chain due to the nature of the processed weak blackbody radiation signals. In addition, the gain variations must be minimized too. To achieve these design goals, an op-amp-based noninverting feedback amplifier architecture is adopted, as shown in Fig. 5. The amplifier has three stages to provide 0–60-dB gain with 20-dB gain step. The feedback architecture reduces the possible gain variation induced by the active devices through a fixed ratio of matched passive resistors. The noninverting structure provides high impedance to the previous envelope detector stage for minimum loading and reduces the input-referred noise at low-gain condition. The dc offset cancellation circuit, with 500-kHz 3-dB corner frequency, is utilized to remove the static dc offset of the amplifier and features a fast settling time for gain switching. Its cancellation corner frequency is lower than the system chopping frequency to not attenuate the desired signals. To reduce the circuit flicker noise corner frequency down to kilohertz, large-channel-length ($\sim 1\ \mu$m) CMOS devices are used in this PGA. Moreover, it is designed with signal bandwidth higher than 10 MHz to accommodate a high chopping clock frequency. The PGA also features differential implementation and consumes $\sim$6 mW, which includes the power consumption from an output buffer to drive the following ADC with about-1-pF input capacitance.

To quantize the output signal from the PGA and capture the small portion of blackbody radiation buried in the large circuit noise from the imager, a high-resolution ADC is needed. In addition, the ADC needs to have a sampling frequency much higher than the chopping frequency. Consequently, a 10-bit 20-MHz ADC is designed to be compatible with the envelope detector and the PGA's bandwidth of 10 MHz. A pipeline ADC is adopted, which integrates eight pipeline stages with 1.5 bits per stage and one 2-bit flash stage, as shown in Fig. 6. A two-stage gain-boosting amplifier with $>$ 75-dB low-frequency gain and $>$ 400-MHz gain bandwidth is utilized for the multiplying digital-to-analog converter (MDAC) core in each pipeline stage.

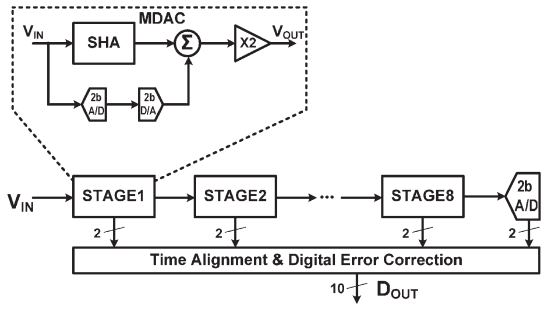

Fig. 6. Schematic of the pipeline ADC.

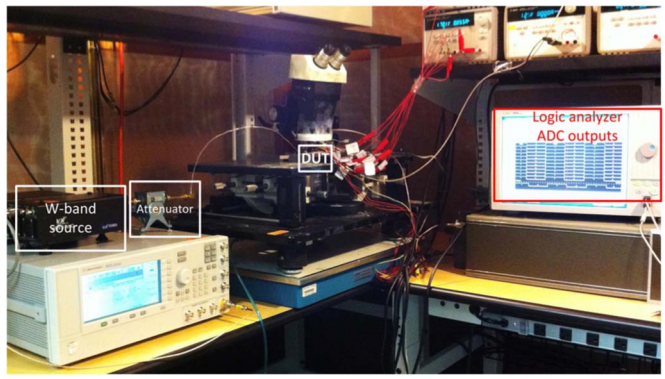

Fig. 7. Measurement setup.

It is worth noting that the flicker noise and low-frequency gain variations of the ADC will also be sampled and canceled by the chopping system to minimize their effects on imager performances.

The entire integrated passive imager has been designed with a compact structure and fabricated in 65-nm CMOS. It receives a signal from a single-ended input and outputs 10-bit digital signals representing the sum of the input signal and circuit internal noise.

III. Measurement Results

To characterize the chip performance, a monolithic multiplier chain generates a W-band signal, which passes through an external attenuator with 50-dB dynamic range to feed into the chip as the input. A logic analyzer detects and processes the ADC 10-bit outputs. The measurement setup is shown in Fig. 7.

The 10-bit digital outputs, together with the chop signal, represented in red, are displayed on the logic analyzer as shown in Fig. 8. The ADC outputs directly represent the input power level. Fig. 8(a) and (b) shows the ADC output codes at different input power levels. At 90 GHz, a $-$48-dBm input signal generates a full-scale output at the ADC by toggling between all "1" bits (summed decimal code of 1023) and all "0" bits (summed decimal code of 0), as shown in Fig. 8(a). All "1" bits correspond to the signal detection cycle by setting the chop clock at a low voltage level. All "0" bits correspond to the reference calibration cycle by setting the chop clock at a high voltage level. There is a delay between the chop signal and the ADC outputs due to nonidentical sampling. When the input power is reduced to $-$51 dBm, the ADC outputs scale down to about 540 (between a code around 230 during the reference calibration and a code around 770 during the signal detection), as shown in Fig. 8(b). There are some variations in

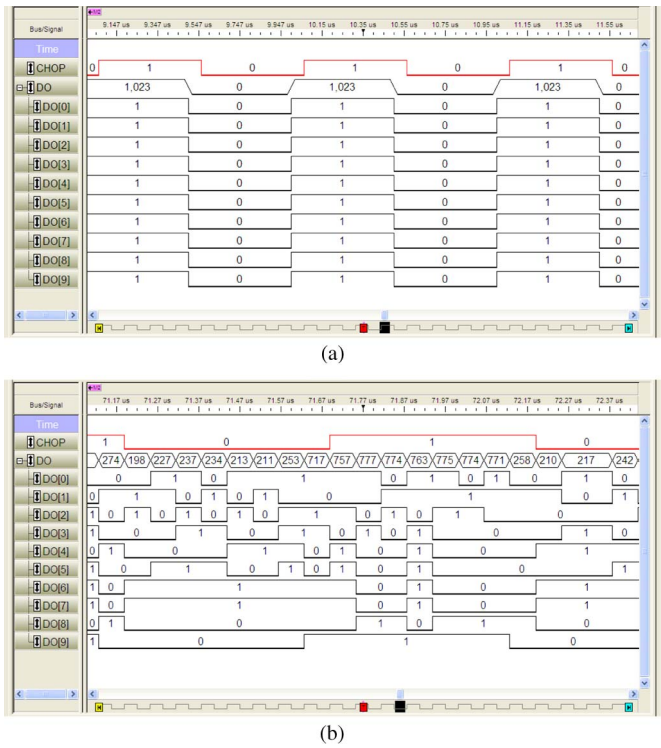

Fig. 8. Measured ADC outputs and chop signal at (a) a high input power and (b) a reduced input power.

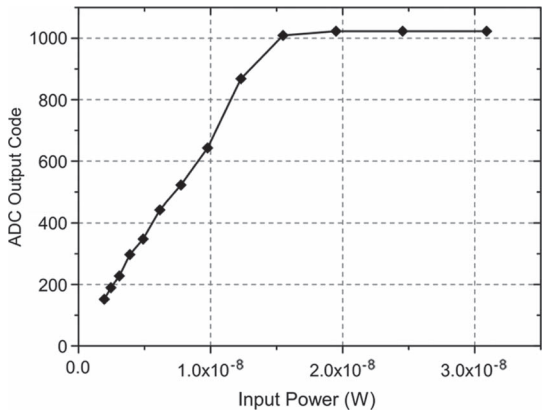

Fig. 9. Measured ADC output versus input signal power.

the code values because of circuit noise. Fig. 9 shows the ADC output code versus input power at 90-GHz input frequency. In this ADC design, one least significant bit corresponds to about 0.9 mV. The ADC realizes a fair linear responsivity until its saturation. The chain responsivity is estimated to be higher than 60 MV/W at an input frequency of 90 GHz.

Fig. 10 shows the ADC output without an input signal, which corresponds to circuit noise. It presents an rms noise voltage of 9.3 mV at the ADC output. A 16-MHz signal is used as the sampling clock to the ADC instead of the designed 20 MHz due to the insufficient driving capability of the digital output drivers in this design. By using the 16-MHz sampling clock, the noise voltage density at the ADC output is interpreted as $3.3/\sqrt{\text{Hz}}$.

Fig. 11 shows the overall passive imager responsivity and NEP versus input signal frequency, which suggests a front-end average bandwidth of 18.1 GHz and an average responsivity of 103 MV/W. Therefore, the average NEP is 32 $\text{fW}/\sqrt{\text{Hz}}$.

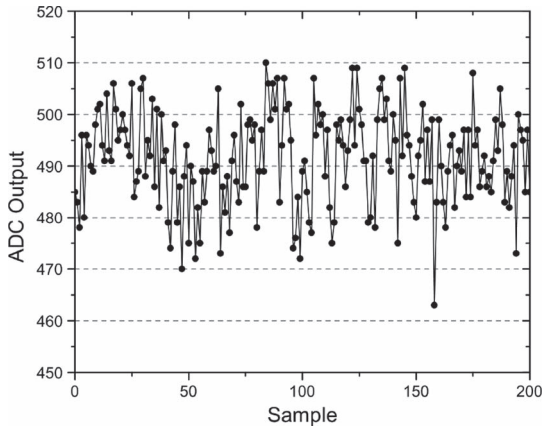

Fig. 10. Measured ADC output code without an input signal to indicate circuit noise level.

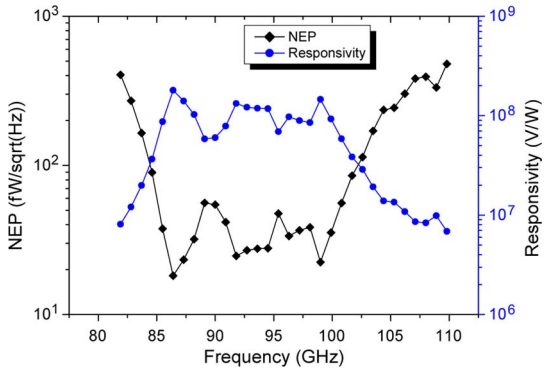

Fig. 11. Measured passive imager responsivity and NEP versus input signal frequency.

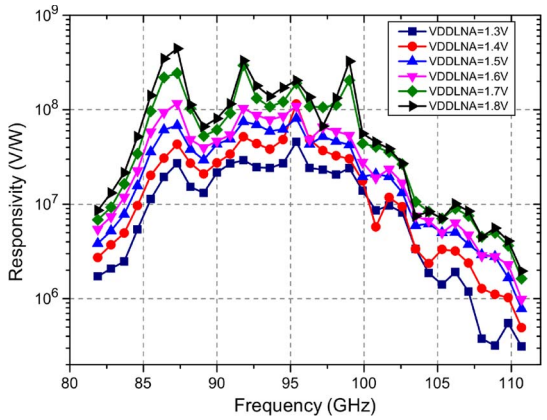

Fig. 12. Measured passive imager responsivity versus frequency with different LNA voltage supplies.

According to (2), the calculated NETD with 30-ms integration time is about 1.0 K.

Fig. 12 shows the passive imager responsivity at different LNA supply voltages, which demonstrates monotonic relationship with a higher supply voltage corresponding to a higher responsivity. At 1.3-V supply, the measured average responsivity is about 23.4 MV/W, which increases to beyond 100 MV/W for 1.8-V supply. The LNA is based on a cascode structure with the bulk of the cascode device biased at a high voltage (around 1 V). Therefore, it can tolerate high supply voltage up to 2 V without reliability concern.

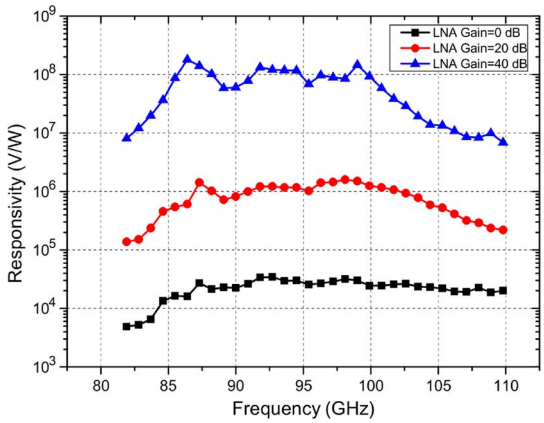

Fig. 13. Measured passive imager responsivity versus frequency with different LNA gain settings.

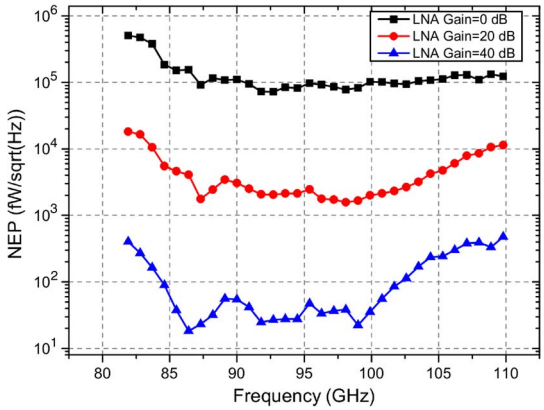

Fig. 14. Measured passive imager NEP versus frequency with different LNA gain settings.

Fig. 13 shows the measured overall imager responsivity and NEP across the frequency from 80 to 110 GHz at different LNA gain settings. The passive imager demonstrates an average responsivity of above 100 MV/W when the LNA is set at a high-gain mode. However, the average responsivity drops to 24 kV/W at LNA low-gain mode. It is notable that the measurement result demonstrates about-20-dB/step adjustability, which agrees well with the simulated LNA gain results, as shown in Fig. 3.

Fig. 14 shows the NEP at different LNA gain settings, with a high NEP corresponding to a low LNA gain and a low responsivity. This is mostly due to the increasing noise contribution of the subsequent detector at low-gain modes. Therefore, the overall output noise presents small changes at different LNA gain settings, from 2.48 $\mu\text{V}/\sqrt{\text{Hz}}$ at the lowest LNA gain to 3.28 $\mu\text{V}/\sqrt{\text{Hz}}$ at the highest LNA gain. At the highest LNA gain setting, the passive imager achieves the average NEP of 32 $\text{fW}/\sqrt{\text{Hz}}$.

Fig. 15 shows the chip photograph with a chip area of 1.17 mm^2 including pads. The overall power consumption is 151 mW. Table I summarizes the prototype imager performance and the performance comparison with those of state-of-the-art silicon-based implementations in W-band.

IV. Conclusion

This work realizes a highly integrated W-band passive imager by integrating a high-resolution ADC on chip. The measured average NEP is about 32 $\text{fW}/\sqrt{\text{Hz}}$ with an average responsivity of 103 MV/W and a bandwidth of 18.1 GHz. This corresponds to a NETD of 1.0 K with 30-ms integration time. This work further pushes the applicability of CMOS technology for portable passive millimeter-wave imaging systems.

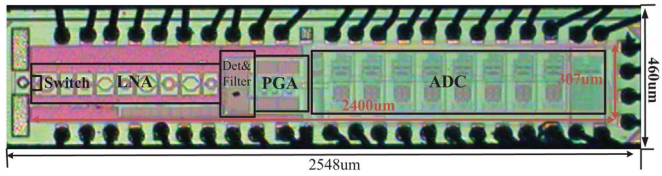

Fig. 15. Die photograph in 65-nm CMOS technology.

TABLE I
Performance Summary and Comparison With State-of-the-Art W-band Passive Imagers in Silicon Processes

	Ref.[3]	Ref.[4]	Ref.[5]	this work
Technology	0.12um SiGe	65nm CMOS	0.18um SiGe	65nm CMOS
Integration	LNA+Det.+SW	LNA+Det.+SW	LNA+Det.+SW+ analog baseband & integrator	LNA+Det.+SW+ analog baseband + ADC
NEP	21 fW/√Hz	111 fW/√Hz	N/A	32 fW/√Hz
Responsivity	2.5~5 MV/W	63 kV/M	63 kV/M	103 MV/W
NETD with τ=30ms	0.83 K	12.5 K	0.4 K	1.0 K
Power	35 mW	38 mW	200 mW	151 mW

Acknowledgment

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