A CMOS 135-150 GHz 0.4 dBm EIRP Transmitter with 5.1dB P1dB Extension Using IF Envelope Feed-Forward Gain Compensation

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Abstract — **A CMOS D-band 135-150 GHz transmitter is presented with integrated digital control and on-chip antenna. The proposed transmitter employs an IF feed-forward compensation scheme which improves the soft gain compression of the power amplifier by 5.1dB to provide an overall more linear AM-AM profile allowing reduced power back-off for modulation schemes with a high peak-to-average ratio. The proposed D-band transmitter consumes 255mW and occupies 2000 x 1500 um of silicon area. The proposed transmitter delivers a 0.4 dBm EIRP and a saturated power on chip of 13.2 dBm. The transmitter has a peak PAE of 8.2% with power delivered to the antenna and a peak PAE of 0.4% when considering radiated power.**

I. INTRODUCTION

Recent advances in silicon technology have enabled the possibility of CMOS based Gb/s rate mm-wave communication beyond the 100 GHz frequency range. While digital and mixed-signal techniques to support Gb/s communications are quite mature, design of RF front-ends beyond W-band is a relatively new topic. Design of power amplifiers that deliver enough output power to maintain the required link SNR become challenging, especially at frequencies approaching 150 GHz as the available device gain is low. One difficult challenge of mm-wave transmitters operating beyond 100 GHz is that amplifier compression is quite soft [1]. This means that the gain begins to compress at signal levels far below saturation. Power amplifier compression directly contributes to the transmitter's overall AM-AM characteristic, a major source of non-linearity and EVM degradation, especially when modulations with high peak-to-average ratios are used. While digital compensation techniques such as digital-pre-distortion (DPD) are common at lower frequencies the high symbol rate and wide channel bandwidth of Gb/s mm-wave communication makes their implementation increasingly difficult.

Fig. 1(a) shows the gain compression profile for a typical CMOS mm-wave transmitter chain as the power amplifier's static DC bias current is increased. While the saturated power does increase as the DC bias current is raised, the back-off point where the compression begins remains almost constant, and limits the linearity improvement that can be achieved. Instead of adjusting the bias to a fixed value we propose to construct the transmitter with the compression profile that is shown in Fig. 1(b). By intentionally removing some of the small-signal gain and then adjusting the bias dynamically based on the signal's power envelope the linear range of the power amplifier can be artificially increased, allowing operation to occur closer to the saturated power level.
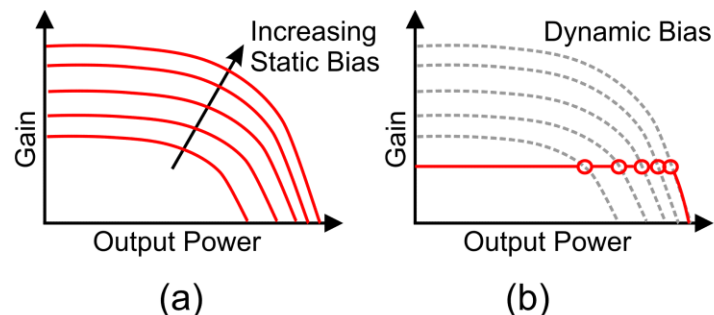

Fig. 1. (a) Typical gain compression profile for a CMOS mm-wave PA as static bias current is increased. (b) Proposed compression profile showing intentionally removed gain at small-signal levels and dynamic biasing.

One major challenge of mm-wave front-ends operating at frequencies beyond 100 GHz is that stage gain for power amplifiers is quite low [2,3], typically only 2-5 dB of gain per stage. This low gain makes the front-end extremely sensitive to the effects of temperature and process variation as a small change in the CMOS device parameters may drastically reduce or even altogether eliminate the front-end gain. For this reason it is necessary to have a calibration or adjustment scheme, which can optimize the small gain available in the front-end. For calibration a digital approach combined with software is highly preferred as analog calibration requires manual adjustment.

In this paper we propose a 135-150 GHz transmitter chain implemented in 65nm CMOS technology that contains compensation for the soft gain compression profile of the mm-wave power amplifier. The proposed gain compensation technique functions by first tracking the power envelope of the transmitted signal at the IF frequency. The detected power envelope is then subjected to simple analog signal processing (offset & amplitude adjustments) and used to modulate the bias of the power amplifier's output stage. The signal-processing coefficients, power amplifier biases, RF mixer biases and even LO settings are controlled by a series of calibration digital-to-analog converters (DACs) to provide a means to calibrate out the process and temperature variations. Additionally at D-band (140-170 GHz) it becomes feasible to integrate the antenna on-chip instead of relying on packaging technology to connect the transmitter to the outside world.
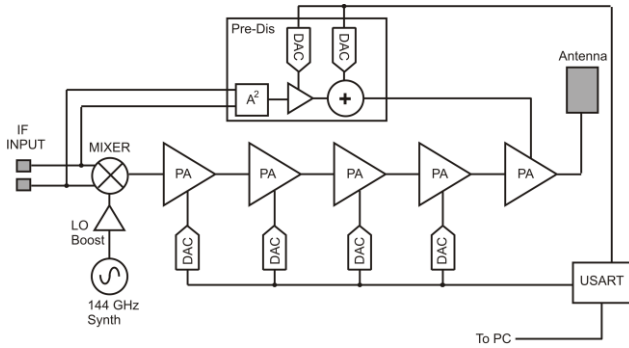
II. TRANSMITTER CHAIN

Fig. 2. Block diagram of the proposed 135-150 GHz mm-wave transmitter.

Fig 2. shows the block diagram of the proposed mm-wave transmitter chain. The IF can be fed in from an external source or the transmitter can be used for direct conversion DSB modulations. The mixer is driven by an LO which is generated on-chip by a 144 GHz frequency synthesizer. After the mixer, a 5-stage power amplifier brings the transmitted signal up to full power (~10 dBm) for transmission by the antenna. The first 4 stages of the power amplifier are controlled by calibration DACs which can set the bias current level of each stage. Each DAC is a simple R2R configuration with 8 bits of resolution. Since the DACs only provide DC control levels, the dynamic performance is not critical and the RC time constants can be made large to save power. The DACs are ultimately controlled by a small USART ASIC linking to a PC computer through an RS-232 interface. The IF feed-forward compensation block also connects to the input IF signal and contains two DACs, one for the offset adjustment and the other for the gain adjustment. The output of the compensation block provides the bias voltage for the 5th stage of the power amplifier.
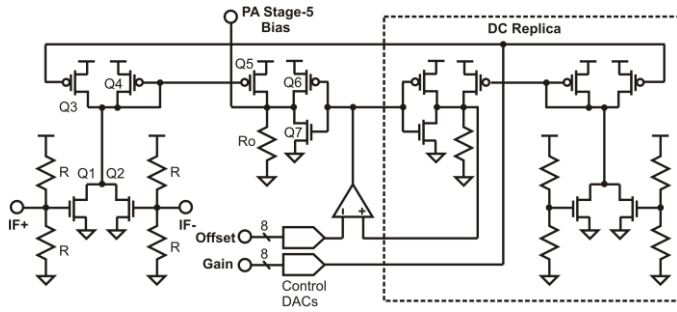

Fig. 3. Schematic diagram of the analog processing for the IF feed-forward gain compression compensation.

Fig 3. shows the circuit diagram for the IF feed-forward compensation used to cancel the soft compression of the power amplifier. The circuit first employs a simple resistive envelope detector composed of Q1 and Q2 and loaded by current mirror Q4-Q5 to extract the envelope of the IF signal. Device Q3 is controlled by the "Gain" DAC and steals a percentage of the

current away from the current mirror to provide gain control of the envelope signal. Since the output of the current mirror is single ended, the DC common mode cannot be extracted by conventional differential approaches, and using an RC filter would require large capacitor area for the time constants involved. Instead we use the replica circuit shown on the right of Fig. 3 that has a DC voltage tracked by the op-amp. The output stage of the op-amp is duplicated by Q6 and Q7 to set the DC voltage at the output of the circuit. The DC voltage is selected from the "offset" DAC by providing the tracking reference voltage to the opamp. With this approach the bias for the power-amplifier can be separated for large and small signals allowing the compression profile to be digitally tuned from the two DAC inputs. The envelope detection circuit and its replica must be symmetric in layout to obtain the necessary matching.
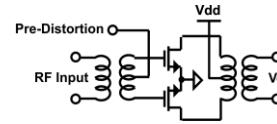

Fig. 4. Power amplifier output stage showing transformer coupling for RF connections and center-tap for IF feed-forward signal connections.

Fig. 4 shows the output stage of the mm-wave power amplifier in which all stages are transformer coupled. The compensation signals for the 5th stage of the PA (and DAC inputs on stages 1 to 4) are fed through the center-tap of the winding connected to the input. This allows modulation of the bias current without disturbing the differential-mode RF signals.

III. MEASUREMENTS

Fig. 5 shows the swept power response of the proposed transmitter with and without the feed-forward compensation enabled. The compressed equivalent isotropically radiated power (EIRP) is measured with the de-embedded path loss using a harmonic mixer and spectrum analyzer. The P1 compression point is marked on both curves showing that the technique improves the P1 point by 5.1 dB.
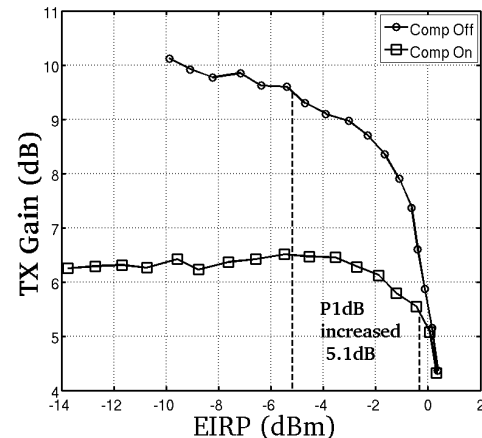

Fig. 5. Measured TX compression with and without the proposed IF feed-forward compensation scheme showing 5.1dB improvement in P1dB.
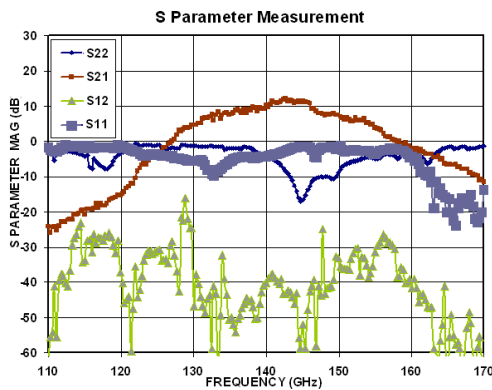
Fig. 6. S-Parameter measurements of the mm-wave power amplifier.

Fig 6. shows the s-parameter measurements of the power amplifier measured from a stand-alone PA chip. The amplifier provides approximately 11dB of gain and has a 3dB bandwidth of 15 GHz. The power amp bandwidth was found to be limiting block of the entire transmitter chain, as the other stages are not tuned. Fig 7. shows the testing setup for the compression and EIRP measurements using a harmonic mixer and a 15dBi D-band horn.
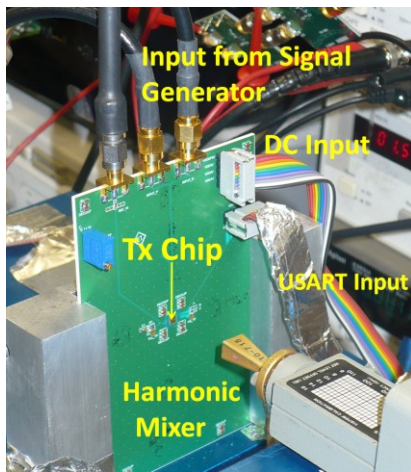

Fig.7. Testing setup for measurement of the effective isotropic radiated power and transmitter gain compression profile.

Since an antenna chamber capable of D-band measurements was not available, we instead show the simulated antenna gain of our integrated half-wave patch antenna in Fig. 8. The simulated gain is –6dBi in a direction approximately normal to the surface of the transmitter chip.
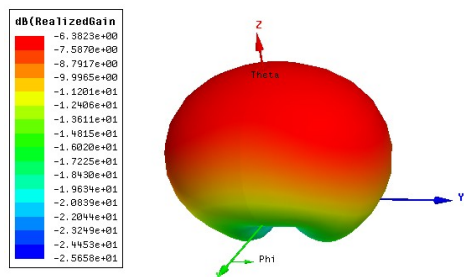

Fig.8. Simulated gain of the integrated 135-150 GHz antenna.

In measurement using the VDI power sensor we measured a saturated EIRP of 0.4 dBm using a calibrated path loss for a distance of 5.0 cm from the chip surface. The stand-alone PA test chip was measured to have a saturated power of 13.2 dBm when directly measured with a D-band probe.

IV. SUMMARY

The proposed feed-forward gain compensation transmitter was shown to improve gain compression and increased the P1 compression point by 5.1 dB when implemented in a 65nm CMOS technology. Also demonstrated was a digital technique for calibration of high-frequency mm-wave front-ends using 8-bit DACs to adjust bias currents for optimization of stage gain. The proposed transmitter offers 15 GHz of bandwidth centered between 135 and 150 GHz, with a saturated output power of 13.2 dBm and peak EIRP of 0.4 dBm. The entire transmitter consumes 255mW of DC power and occupies 2000um X 1500um of silicon area. When power delivered to the antenna is considered a peak PAE of 8.2% is achieved and when EIRP is considered the peak PAE is 0.4%. Fig. 9 shows a die photo of the proposed transmitter indicating the location of key blocks.
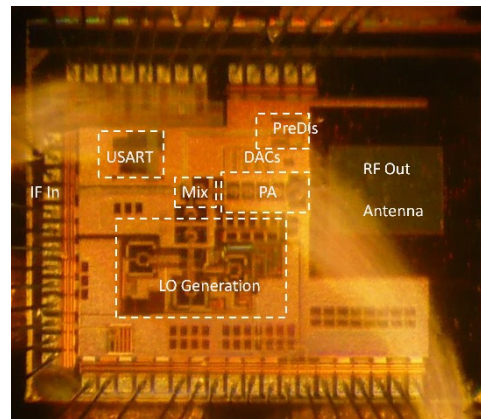

Fig.9. Die photo of the proposed mm-wave transmitter showing the location of key blocks and the on-chip antenna. Glare is from encapsulation coating.

V. ACKNOWLEDGEMENTS

REFERENCES

[1] Jenny Yi-Chun Liu, Adrian Tang, Ning-Yi Wang, Qun Jane Gu, Roc Berenguer, Hsieh-Hung Hsieh, Chewnpu Jou and Mau-Chung Frank Chang, "A V-band Self-Healing Power Amplifier with Adaptive Feedback Bias Control in 65 nm CMOS", IEEE RFIC Symp. 2011, June 2011.
[2] N. Deferm, P. Reynaert, "A 120GHz 10Gb/s phase-modulating transmitter in 65nm LP CMOS", IEEE ISSCC 2011, Feb 2011.
[3] Lei Zhou, Chun-Cheng Wang, Zhiming Chen, and Payam Heydari, "A W-band CMOS Receiver Chipset for Millimeter-Wave Radiometer Systems," IEEE J. Solid-State Circuits, vol. 45, Feb. 2011.