Self-Healing 4Giga-bit/sec Reconfigurable CMOS Radio-on-a-Chip

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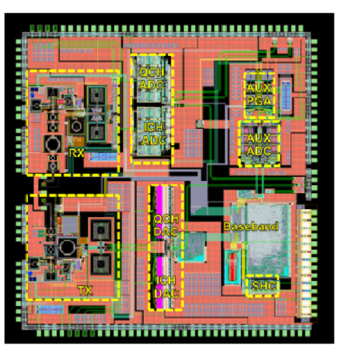
Abstract: *This paper summarizes the development of embedded self-diagnostic and self-healing algorithms and circuit-level techniques to maximize the performance yield of a reconfigurable CMOS Radio-on-a-Chip (RoC) with over-the-air data throughput of 4Gbps. The program requires such yield to be greater than 95% (with area overhead counted) from an individual wafer run that meet all pre-specified go/no-go performance metrics in the presence of extreme process and environmental changes and variations. Although the specific Reconfigurable RoC design is aimed for applications at 60GHz ISM band, its design methodology, sensing & control algorithm and circuit techniques can be scalable in technologies and equally effective in implementing any broadband or multi-band microwave and mm-Wave radios from 10-100GHz for both commercial and military wireless and wired communication systems.*

Keywords: self-diagnostic sensing/control/algorithm; self-healing sensing/control/algorithm; radio-on-a-chip; performance yield; scalable circuit design technique; wireless and wired communication systems; multi-band & broadband radio

Introduction

In the past, radio systems developed for such broad frequency range were made of discrete GaAs MMICs with relatively high component/system costs and long development times. Such systems can ideally be implemented by using the mainstream CMOS, which offers cost-effective manufacturing with the highest integration for both digital and mixed signal circuits. However, the deep-scaled CMOS has its own set of advantages: 1) low supply voltage (<1.2V) with constrained signal dynamic range and linearity; 2) decreasing effective gain due to ever-lowering output impedance; 3) low-Q passives caused by high substrate and metal losses; 4) low circuit yield owing to aforementioned operational constraints and increasing device mismatches and process/temperature variations.

Our analysis, based on foundry-provided 3-sigma process variations in terms of V_{th}, gate lengths, and many other process parameters, indicates that the yield of each of the building block circuits, including the transmitter, receiver, synthesizer, data converters and digital baseband, can be limited to 43-76%. Such yield calculation is also supported by our observed building block chip test results, and thus the composite yield for an integrated *RoC* (Fig.1) would diminish. It is therefore timely for us to assemble a team with combined expertise in RF/mixed-signal CMOS circuit design, sensing/control algorithms, and radio systems to boost the *RoC* yield. Our unique on-chip self-healing approach is completely different from conventional practices based on offline calibrations, which are typically non-optimal and do not address environmental variations and aging. Our approach focuses on developing the right types of process/environment sensors, robust parameter estimators, and intelligent real-time control strategies to eliminate or minimize the effects of process/environmental variations on circuit performance. Our goals are to develop and demonstrate robust self-healing circuit methods that enable the demonstration of a high yield (>97.6% due to self-healing die area increase), fully integrated *4Gbps Radio-on-a-chip* with clearly defined performance yield requirements, summarized in DARPA HEALICS program's go/no-go metrics (Table I).



Feature	Value
Size	4.0 x 4.0 mm
Pads	145
On-Chip Cap	285 pF
Power Domains	44
RF Control	255
RF Frequency	57-65 GHz
BB Clock	2.0 GHz

Figure 1. 60GHz Radio-on-a-Chip (RoC) implemented in 65nm CMOS technology, with integrated Tx, Rx, Synthesizer, I/Q ADC/DAC, digital baseband and on-chip sensors, knobs, parameter estimator to perform self-healing functions to boost the performance yield based on go/no-go performance metrics indicated in Table I. The *RoC* contains roughly 2.4 million CMOS transistors and can communicate at 4Gbps over the air within short distance (<10meter).

Table 1 Go/No-Go Metrics

Go/No-Go Metrics	Phase I: Mixed-Signal-Core (60GHz Transceiver including I/Q ADC)	Phase II: Reconfigurable Radio-on-a-chip *(RoC)*
Receiver (RX)		
NF	6dB	6dB
Output bandwidth	1.2 GHz	1.2 GHz
OIM2 and OIM3	-40dBc	-40dBc
EVM		-25dB
Transmitter (TX)		
P1dB	10dBm	10dBm
TX OIM3	-40dBc	-40dBc
EVM		-30dB[1]
Synthesizer		
Phase Noise	-90dBc@1MHz	-90dBc@1MHz
Channel Frequency	HRP: 58.32 + n × 2.16GHz n=0 . . . 3	HRP: 58.32 + n×2.16GHz n=0 . . . 3
Channel Switch Time	10us	10us
LO distribution IQ mismatch	-40dBc	-40dBc
ADC	ENOB>5.5bit	ENOB>5.5bit
Performance Yield	33 of tested 40 die from one Foundry shuttle run meet all performance metrics	39 of tested 40 die from one Foundry shuttle run meet all performance metrics
Power/Area Consumption Overhead	< 10% over baseline transceiver	<5% over baseline *RoC*

Despite the present choice of implementing the integrated transceiver (i.e. the mixed-signal core) in 65nm CMOS, it is our goal to ensure that the developed self-healing methods and control algorithms are generic and scalable to future generations of CMOS tech nodes. We will also produce self-healing IP core libraries (including design algorithms, schematics, circuit net-list, and related software control codes for the complete self-healing *RoC*) and make them available to DARPA-designated *DoD* designers.

Self-healing architecture and algorithms

The self-healing RoC architecture is shown in Fig. 2a. Sensors are implemented throughout the RF transceiver to detect variation in circuit performance and temperature near circuits that are highly sensitive to temperature. The sensor outputs are digitized by the Aux ADCs and input to the PE which provides robust estimation of the temperature and power that are used by the SHC to determine the gain setting on the transmitter for power control, the backoff required by the transmitter to meet certain linearity requirement, or to determine the setting required on the tuned tank at the output of the PA for optimum output matching. The transmitter output also couples to an auxiliary front-end consisting of a capacitor/varactor tuned tank followed by an LNA. This coupled path enables the transmitter to transmit a probe signal synthesized by the digital modulator and to loopback the probe signal back through the receiver. The probe signal picks up transmitter/receiver impairments which can then be estimated by the parameter estimator and used by the SHC to 1) control the capacitor/varactor tuned tank at the input of the LNA for optimal noise match, 2) control the biasing of the LNA to optimize noise/linearity performance, to control the capacitor/varactor tuned tank of the synthesizer local oscillator (LO) output for optimal IQ matching, and 3) control the loop filter and charge pump parameters to optimize the phase noise. To achieve the aforementioned optimizations, the SHC receives parameter estimates, pi, from the PE and controls the various knobs in the RF transceiver circuits to meet a set of specifications subject to a given cost function, an example of which is shown below

$$C = E\left\{\sum_i \lambda_i \left(s_i - f(\mathbf{x},\mathbf{y})\right)^2\right\} \qquad (1)$$

where λ_i is the weighting of the i^{th} RF transceiver specification s_i being optimized, **x** is a vector of states in the RF transceiver, **y** is a vector of the observed outputs from the RF transceiver, and $f(\cdot)$ is a function that maps the observed output vector and state vector to the actual achieved RF transceiver specification. A larger weighting value can be applied to specifications that contribute more significantly to the overall RF transceiver performance. E{} represents the expectation over the random variables **x** and **y** and can be estimated with a sample average. The cost, *C*, can be minimized or set to a certain target value and tolerance.

To achieve optimal control given the random nature of **x** and **y** due to process variation and noise process inherent in the RF transceiver circuits, the SHC implements a suite of adaptive control methods to determine the optimal control signal **u** that meets a given cost function. The adaptive methods are based on dual control concept whereby the SHC not only determines the controls to the RF transceiver to achieve the desired cost but also sends probe signals to the RF transceiver and the parameter estimator to improve the reliability of the parameter **p** estimated by the PE as shown in Fig. 2a.

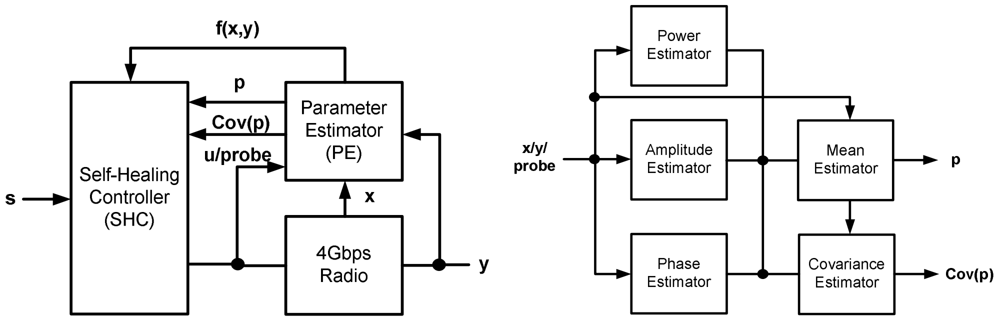


Figure 2. a) Self-healing control architecture **b)** Parameter estimation architecture

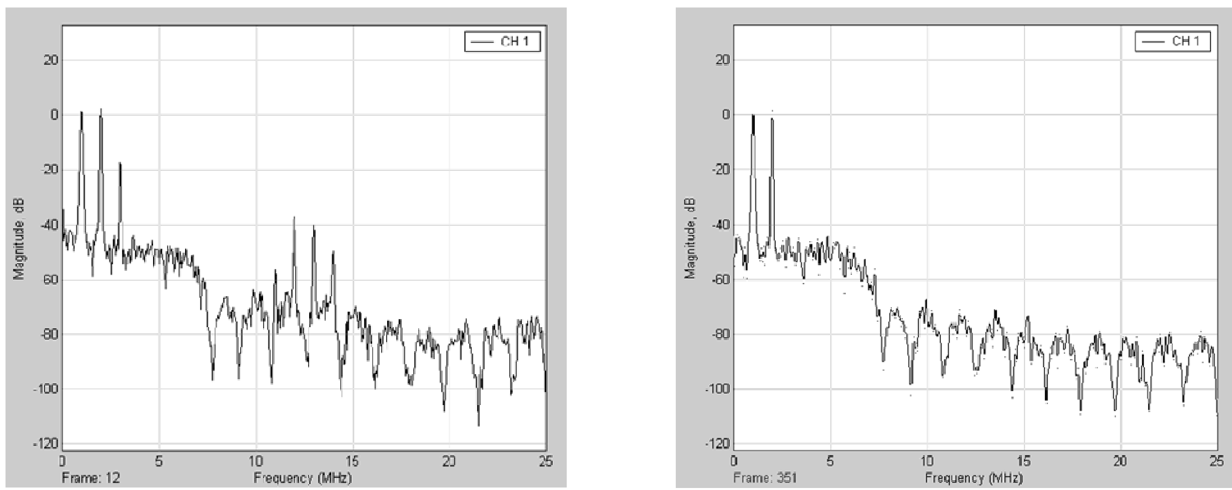


Figure 3. a) Receiver OIM3 before healing **b)** Receiver OIM3 after healing

The reliability information is provided by the PE in the form of a covariance matrix **Cov(p)**, which is employed to intelligently control the RF transceiver states **x** and outputs **y**. For instance, the controller can adjust **x** and **y** more cautiously when the **Cov(p)** has large non-zero elements indicating unreliable RF transceiver parameter estimation. In this case, the SHC can reduce the amount of control applied at each step so that **x** and **y** are adjusted more gradually. On the other hand, when **Cov(p)** has near zero elements, the RF transceiver parameters are more reliable and the estimates are close to its expectation or mean value. The controller can take advantage of the reliable parameter estimates and more aggressively control **x** and **y** for faster convergence. Fig. 3a & b show the self-healing of the receiver OIM3 from -20dBc to -40dBc, satisfying the Go/No-Go metric. The OIM3 has been healed from 20dBc to below -40dBc in the presence of a fairly high noise floor showing the robustness of the control algorithm.

Besides informing SHC on the reliability of **p**, the PE also maps **x** and **y** to the specification being optimized so that the SHC can compute the cost associated for a given control signal **u**. Fig. 2b shows the architecture of the PE which contains a power estimator, an amplitude estimator, and a phase estimator as well as basic statistical estimators for the mean and covariance. The complexity of the estimators must be minimized to achieve low area and power overhead, which are defined as the excess area/power required for self-healing compared to the area/power required without self-healing present. The trade-off can be achieved via time-sharing and algorithm simplification of the estimators when the probe signal is based on a single complex tone. For instance, a single-bin Fast Fourier Transform (FFT) may be used instead of an N-bin FFT for the power, amplitude, and phase estimation.

Self Healing Transceiver Implementation

The implemented self healing transceiver contains a high-performance 60 GHz mm-wave front-end configured in a 2-step heterodyne architecture with LO frequencies of 12 and 48 GHz. The mm-wave transmitter, receiver and synthesizer contain many control points called healing knobs which adjust a variety of parameters including bandwidth, bias, current, linearity and gain. The knobs are centrally controlled from an on chip self-healing system to achieve the desired performance. The self-healing system itself employs a variety of sensors throughout the transceiver to track key performance parameters. The first of these is an envelope sensor that is coupled to the transmitter and returns information about the transmitter LO leakage, IQ mismatch, and distortion.

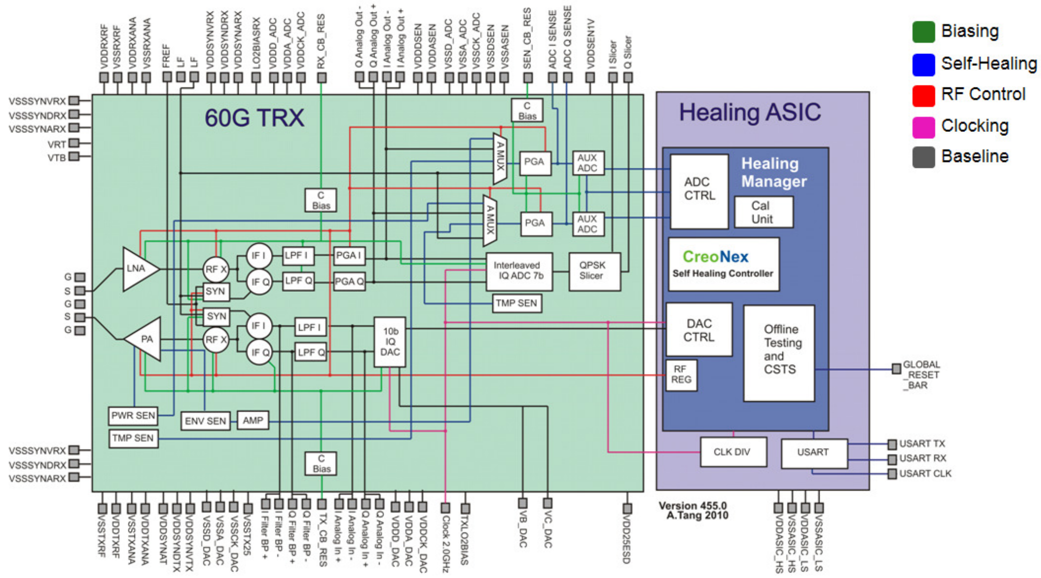


Figure 4. System diagram of the 60GHz Radio-on-a-Chip (RoC) showing integrated Tx, Rx, Synthesizer, I/Q ADC/DAC, digital baseband and on-chip sensors, knobs, and self healing controller.

Using this information, the self-healing controller can make adjustments to the gain and linearity of the transmit chain through the healing knobs. A power sensor placed at the transmitter output is used to track the transmitter power allowing the self healing controller to track and adjust the power delivered by the power amplifier. This sensor is also used to perform power sweeps to collect additional distortion and linearity data about the transmit chain. A temperature sensor is used to estimate the thermal noise floor and combined with an instrumentation ADC placed at the receiver output, these values can provide the self-healing controller an estimate of the receive chain noise figure. The self-healing controller can then make adjustments to the healing knobs of the low-noise amplifier to achieve the required noise performance.

To aid the self healing controller, several additional sub-modules are contained within the healing ASIC including a cal unit which provides one-time calibration for absolute values such as absolute power and absolute temperature, and a DAC control unit which can generate test patterns for single and two-tone test modes. Additionally, there is a USART block which directly interfaces with a PC's USB port so the healing can be monitored.

Finally, for standard radio operation, the self-healing transceiver contains a set of high performance data converters and a modem for single-carrier QPSK modulation. The converter set operates with a 2.0 GS/s sample rate and offers 34 dB of spur free dynamic range.

Summary

We have developed a holistic self-diagnostic and self-healing algorithm and on-chip sensors and knobs to boost the yield of a reconfigurable CMOS Radio-on-a-Chip (RoC) according a set of targeted go/no-go performance metrics. Our phase I target is to reach 85% of the performance yield including the added self-healing circuit area/power overhead. Although the specific circuit/system design is based on 65nm CMOS technology and aimed for radio applications at 60GHz ISM band, its design methodology and circuit implementation techniques can be scalable to future generation technologies and will be equally effective to apply to any broadband (multi-band) microwave and mm-Wave communication systems from 10-100GHz for both commercial and military wireless and wired communication systems.

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