Millimeter Wave and Sub-millimeter Wave Circuits for Integrated System-On-a-Chip

[1]Qun Jane Gu, [2]Zhiwei Xu and [3]Mau-Chung Frank Chang
[1]Electrical and Computer Engineering Department, University of Florida, Gainesville, FL 32611, USA
[2]HRL Laboratories LLC, Malibu, CA 90265, USA
[3]Electrical Engineering Department, University of California, Los Angeles, CA 90095, USA
[1]qgu@ece.ufl.edu [2]zaxu@hrl.com [3]mfchang@ee.ucla.edu

***Abstract* — Deep-scaled CMOS technologies have provided ultra-high speed devices for implementing integrated millimeter wave and sub-millimeter wave system-on-a-chip (SoC). Achieving SoC necessitates key mm-wave/sub-mm-wave circuits, including signal generators and amplifiers. The paper will exemplify some of the key circuits in CMOS technologies, including a terahertz oscillator, a 450 GHz voltage controlled oscillator (VCO), a 200 GHz frequency divider, and a 200 GHz amplifier. With the availability of key building blocks, mm-wave/sub-mm-wave SoC will be realized in the near future.**

Index Terms - amplifier, frequency divider, millimeter-wave, oscillator, sub-millimeter wave, terahertz, VCO

I. INTRODUCTION

Millimeter wave and sub-millimeter wave circuits and systems are attracting more interest due to their high potential in various applications, such as wireless sensing and imaging, high speed wireless communications, and all-weather radars [1]. Conventional electronic approaches are based on discrete components by using III-V technologies [2, 3]. These technologies are not suitable for very large scale integration (VLSI) digital signal processing, which are normally necessary in electronic systems. Therefore, III-V technology based mm-wave/sub-mm-wave systems normally demand multi-chip approaches and therefore are not the best candidates for small form factor integrated solutions.

Silicon based processes have high promise due to their high integration capability. Today's advanced technologies provide high speed devices to make the silicon based solutions possible and therefore attract lots of research interest. For example, Momeni demonstrated 0.16 mW output power at 480 GHz in a 65 nm CMOS technology [4]. Ojefors presented -17dBm output power at 820 GHz in a 0.25 um SiGe process [5]. Recently, several silicon based mm-wave imaging systems have been demonstrated [6-10]. All these researches aim to enable integrated mm-wave/sub-mm-wave systems.

To achieve the goal of integrated mm-wave/sub-mm-wave SoC, several key building blocks with low power and small form factor are prerequisite, including mm-wave/sub-mm-wave signal generators and amplifiers. This paper will present some of these key CMOS circuits and validate circuit design techniques with low power consumption and small form factor. The circuits include a terahertz (THz) oscillator, a 450 GHz VCO, a 200 GHz frequency divider, and a 200 GHz amplifier all in CMOS technologies.

II. CMOS TECHNOLOGY LIMITS

CMOS's well-known constraints and drawbacks limit their applications in high performance mm-wave/sub-mm-wave circuits and systems. For operating frequencies, though deep scaled technologies provide high intrinsic speed devices, they suffer from large parasitics due to closer physical locations. Simulation analysis proves that external parasitics account for over 50% of device intrinsic capacitance. These large parasitics will drop device cut-off frequencies by more than 20%. For output power, CMOS technologies' low supply and breakdown voltages limit the output power delivery. Low voltage limit requires ultra-small output impedance from power amplifier (PA), which decreases the power conversion efficiency of the impedance matching network. As for other circuit performances, such as gain, noise, and power efficiency, CMOS high lossy mechanisms impose great design challenges. Lossy mechanisms include large contact resistance, lossy substrate, and high frequency skin effects. These losses increase circuit noise, degrade circuit gain performance and waste extra power to result in low power efficiency. To overcome aforementioned limitations of silicon processes, new and creative design ideas are needed.

III. MILLIMETER AND SUBMILLIMETER WAVE CIRCUITS

A. *CMOS Terahertz Oscillators*

CMOS circuits' highest operation speeds are normally limited by device cut-off frequencies, which are often up to 1/5 of the device cut-off frequencies. To break through the speed limitation, we proposed a new oscillator architecture which utilizes a Frequency Selective Negative Resistance (FSNR) tank in parallel with a conventional tank to boost both operation frequency and loop gain to generate a fundamental oscillation frequency higher than the device f_T [11], as shown in Fig. 1. To further push the operation frequency higher, double push-pull structure is adopted by coupling I and Q channels [12, 13]. The output will be sensed at the common mode node and radiate through an on-chip patch antenna. This method will boost the higher (4^{th}) order harmonic and suppress lower order harmonics.

The oscillator consists of a primary tank with $L_{\tan k}$ shunt between the drains of the bottom cross coupled pair (blue

dash circle) and a parallel FSNR tank with L_g shunt between cascode devices (pink solid circle). This architecture not only allows large L_{tank} and L_g inductances, but also combines them via cascode circuit to form a hybrid tank with a low overall inductance for terahertz operation. Second, the FSNR tank also boosts the overall stacking resonator impedance, which eases the demand on the cross coupled device's g_m to permit smaller devices for further higher oscillation frequency. Finally, the added FSNR tank vertically shares the same current with the conventional tank and thus does not consume additional power.

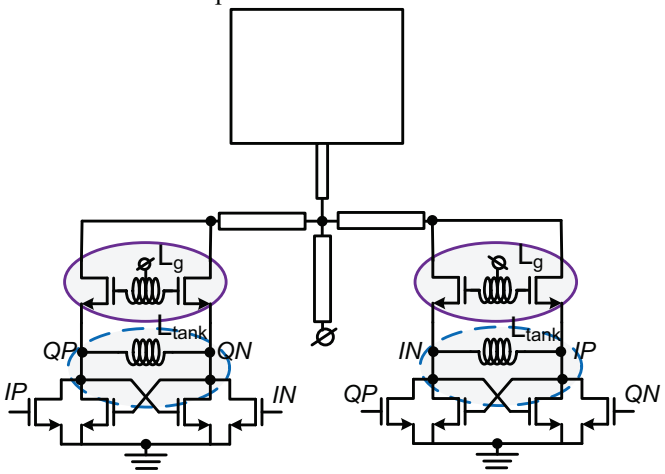

Figure 1. Proposed 4th order harmonic boosted oscillator structure with FSNR tank (pink solid circle) in parallel with conventional tank (blue dash circle).

Interferometer-based quasi-optical approaches are adopted for measurement. As shown in Fig. 2(a), the signal, radiating from the vertically mounted oscillator on-chip antenna, passes through the interferometer and then is detected by a bolometer. The output signal spectrum, recovered through FFT, is shown in Fig. 2(b). The 4th order at about 870 GHz and 6th order at about 1.3 THz are clearly verified. Figure 2(c) shows the chip photo with the core area 300 um x 150 um. The oscillator draws 12 mA current from a 1.4 V power supply.

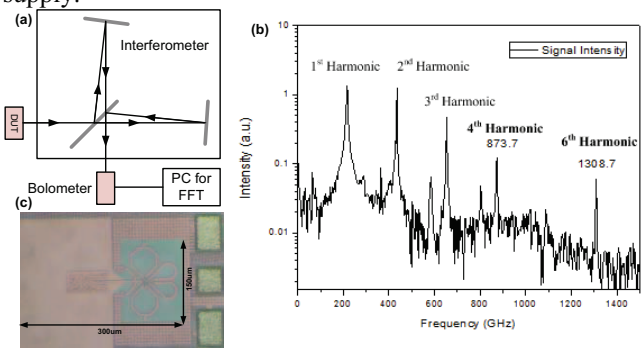

Figure 2. (a) Michelson interferometer based quasi-optical measurement setup for THz oscillator, (b) measured output spectrum, and (c) the die photo of the THz oscillator.

To realize frequency tuning, a small size varactor is inserted. A differential VCO with a 0.74um x 0.06 um varactor is demonstrated. The schematic is shown in Fig. 3(a). An on-chip patch antenna is also integrated to facilitate testing. Figure 3(b) presents the tuning range at the fundamental frequency, which is from 225 GHz to 226.7 GHz with 1.7 GHz tuning range. This is equivalent to 3.4 GHz for the 2nd order harmonic output signal. This VCO draws 5mA current from 1.4V power supply. The die photo is shown in Fig. 3(c) with the chip area 350 um x 280 um.

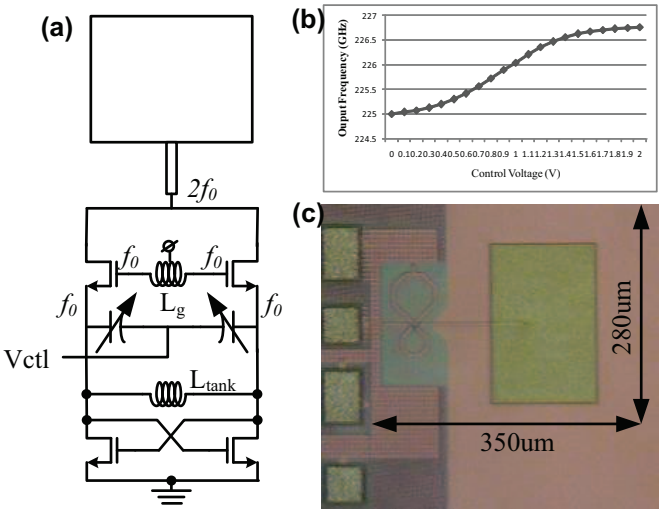

Figure 3. Differential 2nd order harmonic push-pull VCO, (a) schematic, (b) measured 1.7 GHz tuning range for the fundamental tone, and (c) the die photo in 65 nm CMOS.

B. *200 GHz Frequency Divider*

To realize stable and controllable signal generation, closed loop synthesizers are needed. In synthesizer circuitries, the first frequency divider after an oscillator is one of the most challenging blocks due to the requirements of both high operating frequency and wide locking range.

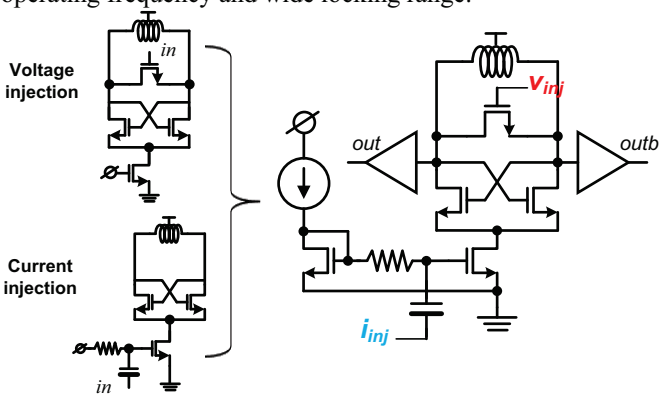

Figure 4. Proposed time-interleaved injection locking scheme based prescaler topology to boost locking range

To achieve simultaneously high operating frequency and wide locking range, we create a new time-interleaved injection locking frequency divider [14]. As illustrated in Fig. 4, the input signal is injected to both the top voltage mixing device and the bottom current source device, to attain extended

injection angles that can lead to simultaneously higher oscillation frequency and wider locking range.

Voltage and current injection methods integrated by this time-interleaved scheme complement each other through working at different time periods, as shown in Fig. 5. For voltage injection, the input signal Vin is injected at the gate of a NMOS mixer that shunts outputs of the crossing couple. As the injection voltage increases and the V_{gs} starts to exceed the device threshold, the mixer turns on and introduces a low impedance path to pull its source and drain (or the cross-coupled outputs) voltages closer. As a result, when voltage injection occurs at an instance outside of the output crossing time period of the prescaler, the voltage injection tends to pull outputs toward each other. If the prescaler's natural oscillation frequency is close to half of the injection frequency, such an effect will ultimately align the prescaler's output frequency and its phase with the voltage injection signal, as shown by the orange area in Fig. 5 with the defined injection angle of θ_1 . On the other hand, a current signal I_{inj} is injected via the current source of the crossing couple pair. During the positive (or negative) current injection cycle, the increased (or decreased) source current would split unequally to the resonant tank and increase (or decrease) the voltage difference between prescaler outputs. Provided the prescaler's natural oscillation frequency is close to half of the current injection frequency, the prescaler's output maximum (or minimum) points will be synchronized with effective current injection time zones, represented by the current injection angle θ_2, blue area in Fig. 5.

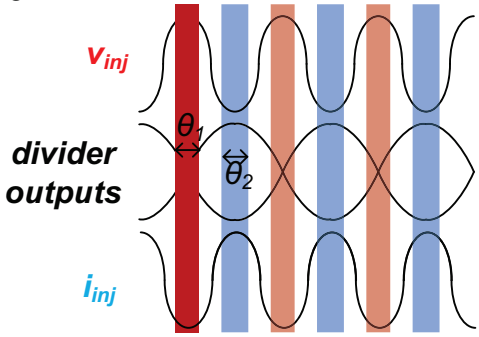

Figure 5. The illustration of boosted injection angles of the time-interleaved injection locking frequency divider

With this novel dual-injection locking scheme, the overall injection strength is boosted by two means. First is the added injection strength due to both voltage and current injections. Second, and more importantly, the interleaving injection renders smaller current during voltage injection period that is equivalent to lower the oscillator current I_{osc}, thus increasing the I_{inj}/I_{osc} ratio for extended locking range. Using factor γ to stand for the phase relationship between the voltage injection and current injection, the time-interleaving locking range can be elaborated as

$$\Delta\omega \approx \frac{\omega_o}{2Q}\left(\frac{I_{inj\_v}}{\gamma \times I_{osc}} + \frac{\alpha \times I_{inj\_i}}{I_{osc}}\right) \quad (1)$$

As γ reaches its minimum when voltage and current injections are 180 degree out of phase, the prescaler has the maximum locking range. When the phase difference deviates from 180 degree, the factor γ gets larger and injection efficiency decreases.

Two prescalers with different inductor values (about 120pH and 150pH, respectively) are implemented in 65 nm CMOS technology. The measured input sensitivities of both prescalers are elucidated by drawing the minimum input power versus the input frequency, shown in Fig. 6(a). The demonstrated locking ranges are over 37GHz (158GHz~195GHz, or 21%) with < 0dBm input power and 27GHz (181GHz~208GHz, or 14%) with < -1dBm input power, respectively. A chip photo is shown in Fig. 6(b) with the core chip area 0.12mm x 0.09mm and the power consumption of 2.4 mW.

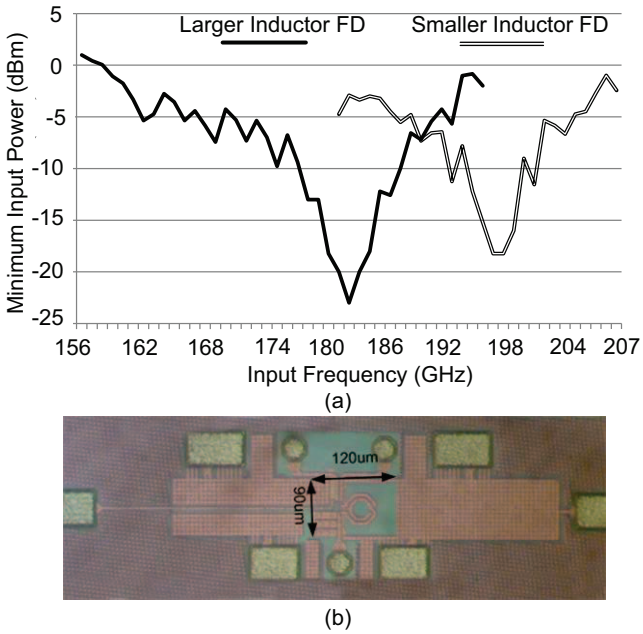

Figure 6. (a) Measured input sensitivities of the two prescalers, (b) die photo of the proposed CMOS prescaler in 65 nm CMOS

C. *200 GHz Amplifier*

Front end amplifiers are also challenging components in mm-wave and sub-mm wave systems, including low noise amplifiers at the receiver side and high output power amplifiers at the transmitter side. On-chip integration demands high noise immunity, thus prefers a differential structure. Therefore, a pseudo-differential 200 GHz amplifier with cascode configuration is adopted [15]. The schematic is shown in Fig. 7. It features five-stage amplification. Transformers T1, T2, T3 and T4 serve as inter-stage matching networks. On-chip baluns not only transfer the input single ended signal to differential on-chip signals to facilitate testing, but also serve as 50ohm matching networks. Each stage's gate and drain biases are set through the transformer/balun center taps separately for independent optimization.

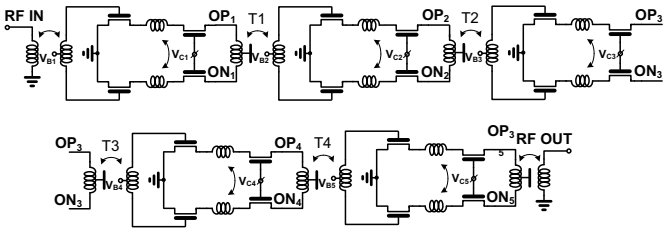

Figure 7. The 200 GHz fully differential CMOS amplifier schematic

Cascode amplifier improves stability by increasing the reverse isolation. Unfortunately, it creates a short path to ground through the stray capacitors from the amplification device drain, cascode device source and interconnect parasitic between them. It becomes significant in sub-mm wave frequencies and forms a lossy path, which degrades amplifier gain and power efficiency. A series inductor is then inserted between stages to construct into a π matching network together with the device stray capacitors for higher gain and power efficiency.

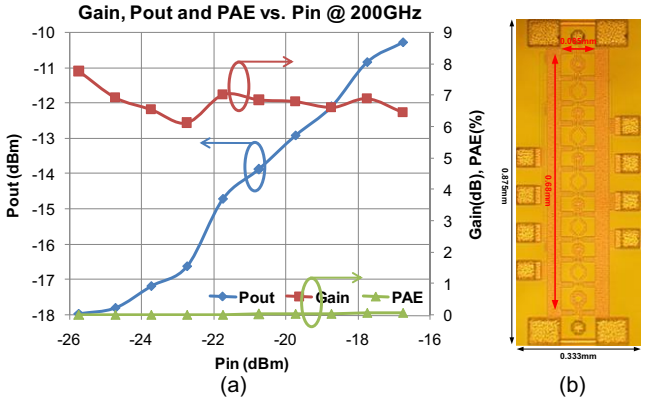

Figure 8. (a) Measured 200 GHz amplifier large signal characteristics, and (b) its die photo

The amplifier characterization in such high frequencies is a major challenge due to delicacy of test setup and lacking of instruments. We use a frequency multiplier chain to generate a 200 GHz signal and a power sensor to detect signal strength. A linearly adjustable attenuator is used to sweep the input power. Figure 8(a) shows the measured output power versus input signal after de-embedding the setup loss. It achieves about 8 dB amplifier gain, the Psat and OP1dB are > -10.3 dBm under 2V supply, mainly limited by the small input power signal source and large setup losses. The S-parameters are measured through a G-band VNA and show consistent measurement results with large signal characterization methods. Figure 8(b) shows the die photo of this 200GHz pseudo differential CMOS amplifier. It is fabricated in 65 nm CMOS technology and the amplifier occupies 0.875 X 0.333 mm^2 and 0.68 X 0.085 mm^2 with and without pads. It draws 54 mA from a 2 V supply.

IV. CONLCUSIONS

This paper presents several key mm-wave/sub-mm-wave building block circuits in CMOS technologies. With the demonstration of these key components, integrated mm-wave/sub-mm-wave SoC solutions will materialize in the near future.

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