A W-band Current Combined Power Amplifier with 14.8dBm P_{sat} and 9.4% Maximum PAE in 65nm CMOS

Zhiwei Xu[1], Qun Jane Gu[2] and Mau-Chung Frank Chang[3]

[1]HRL Laboratories, Malibu, CA 90265, USA
[2]Univeristy of Florida, Gainesville, FL 32611, USA
[3]Univeristy of California, Los Angeles, CA 90095, USA

***Abstract* — We present a 101-117GHz power amplifier (PA) using two way current power combiner in 65nm bulk CMOS. It delivers up to 14.8dBm saturated output power with over 14dB power gain and better than 9.4% power added efficiency (PAE), which also achieves better than 11.6dBm output P_{1dB}. The PA features three stage transformer coupled differential architecture with integrated input and output baluns. To ensure the stability and improve efficiency, the PA first two stages adopt cascode structure and the last stage utilizes common source structure. A current power combiner is employed to combine the power from two separate PAs. The entire PA core occupies 0.106 mm^2 chip area and dissipates about 200mW.**

***Index Terms* — Adaptive Bias, CMOS, PAE, Power Amplifier, Power Combiner, Saturated Output Power, W-band.**

I. Introduction

CMOS power amplifier is the last Holy Grail in the quest for portable single chip wireless communication systems, especially in mm-Wave/sub-mm-Wave frequencies where phase arrays, formed by multiple power amplifiers (PA), are necessary to boost the antenna directivity and transmission efficiency. Deep-submicron CMOS technology enables the mm-Wave transceiver development with high f_T and f_{MAX}. But shrinking supply and device breakdown voltages impose significant constraints on PA in output power (P_{out}), power-added efficiency (PAE), gain, stability and reliability. Many research works have been devoted to 60GHz CMOS PA development for V-band links [1-5]. Radio imaging also demands high Pout and PAE sources at mm-Wave/sub-mm-Wave frequencies [6].

II. Power Amplifier Design

Fig. 1 presents the proposed current combined PA schematic. Transformer coupling, used between stages, tends to pass the signal more effectively compared with capacitive coupling. It can also provide positive voltage gain by choosing proper turn ratios and naturally separate DC biases between stages for individual optimization. All baluns, transformers and power combiners are implemented by stacking the thick (>3μm) top metal with combined second and third top metals (0.9 and 0.22μm). The primary and secondary coils are stacked with offset instead of directly vertical to maximize mutual magnetic coupling with >0.7 coupling coefficient and boost its self-resonant frequency by minimizing the capacitive coupling. The coil turn ratio is designed to provide a larger voltage swing to the next stage input while keeping a smaller swing in its own output to keep PA driver stages away from early saturation for high linearity. A relatively narrow metal width (3-5um) is used to form transformers with reduced coupling capacitance between coils and high enough current (>15mA) handling capability. The transformer self-resonant frequency is designed to be >200GHz to accommodate active device load and parasitics of interconnects.

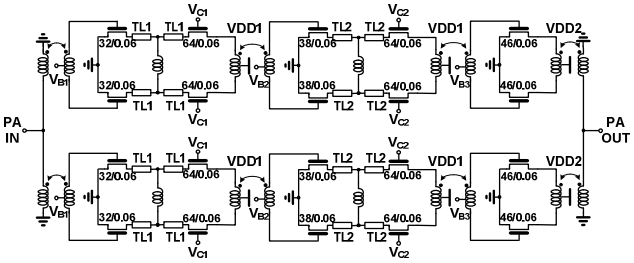


Fig. 1 Schematic of the current combined PA

Cascode pre-amplifier is used to enhance signal gain and reverse isolation. However, such structure creates low impedance paths from cascode nodes to ground through stray capacitance of the devices and interconnects. At sub mm-Wave frequencies, this path significantly wastes power and degrades PAE. A *T*-Network is then inserted at the cascode node to achieve wideband matching between CS and CG devices (Fig. 2). A transmission line stub is used first to transform the impedance from capacitive node A of the CS device drain to node B. A shunt inductor and another transmission line stub are used afterwards to transform the impedance to inductive node C then fulfill the conjugate match. This network mitigates the lossy path and consequently improves the amplifier gain and PAE. It however slightly degrades the amplifier linearity by 0.7dB owing to the increased cascode node impedance.

978-1-4244-8292-4/11/$26.00 ©2011 IEEE

According to our simulations, the proposed *T*-Network improves cascode amplifier's gain by >4dB and reduces amplifier's DC power consumption by 50% for the same amplification gain. Compared with simple inductor shunting and inductor/transmission line series matching, this T network could fulfill conjugate matching with minimum loss.

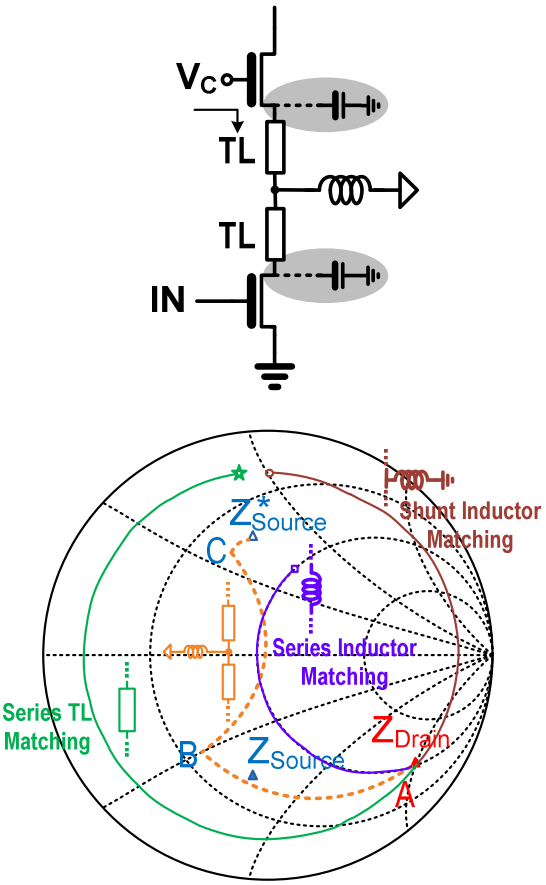


Fig. 2 PA Inter-stage T-matching network

Power combiner merges the output power from two physically separated PAs for higher output power, as shown in Fig. 1, which also serves input/output impedance matching. We choose a two-way current power combiner, shown in Fig. 3, for its higher isolation and lower loss between ports compared with that of voltage power combiner or Wilkinson combiner. Since the current power combiner creates higher on-chip output impedance under matched conditions than its counterparts, it results in higher gain but lower linear output power. To mitigate lower linear power issue, the power combiner turn ratio is chosen to be 1:2 instead of 1:1 to offset the output impedance increase as illustrated by Fig. 3. In an actual design, the output impedance is tuned to be <30ohm. The dimensions of the input power divider and output power combiner are 26400μm^2/22000μm^2, respectively. They achieve better than -10.6dB isolation between ports and about 2dB loss across the entire 101-117GHz band. Good port balance is also insured through layout symmetry, only exhibiting 0.08dB or 8^0 differential imbalance toward each PA unit possibly due to extra capacitance coupling.

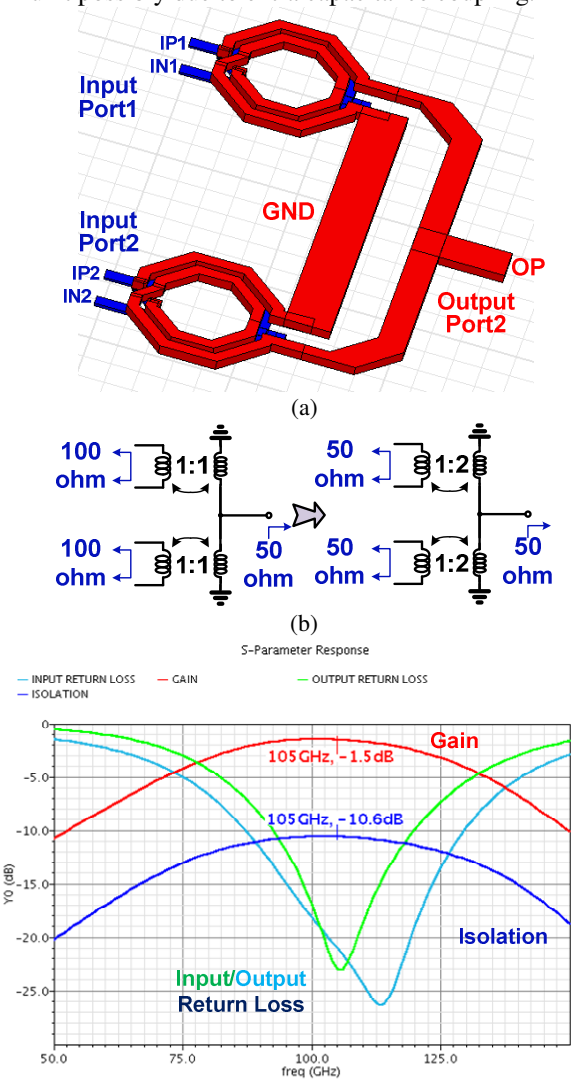


Fig. 3 (a) Animation of power divider/combiner (b) its equivalent model (c) simulated S-parameters

III. Measurement Results

The current combined PA has been fabricated in 65nm bulk CMOS. Fig. 4 shows the PA chip photo, which occupies 0.70mmX0.46mm and 0.48mmX0.22mm with and without pads, respectively. The input power divider and output power combiner use similar architecture but with different sizes, which can be clearly shown in the figure. The input and output PADs are also modeled and

incorporated into the simulation to achieve the optimum matching.

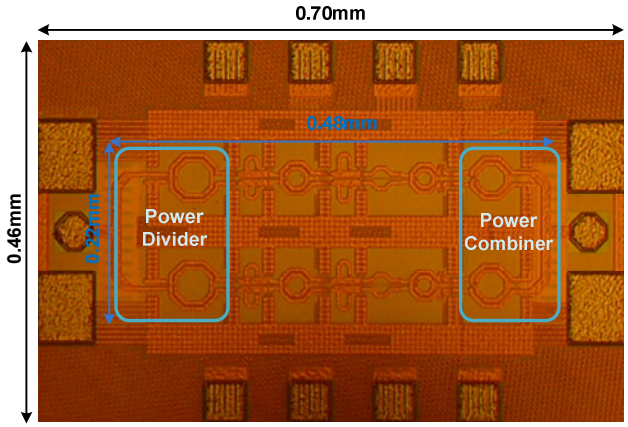


Fig. 4 101-117GHz W-band PA die photo in 65nm CMOS

Harmonic mixer is used to sweep the power amplifier gain quickly first, then a power sensor is used to characterize the amplifier output power, linearity and power added efficiency. The power source consists of a W-band power source provided by Virginia Diode Inc. (VDI) and a tunable attenuator with 50dB dynamic range. Fig. 5 shows the employed measurement setup.

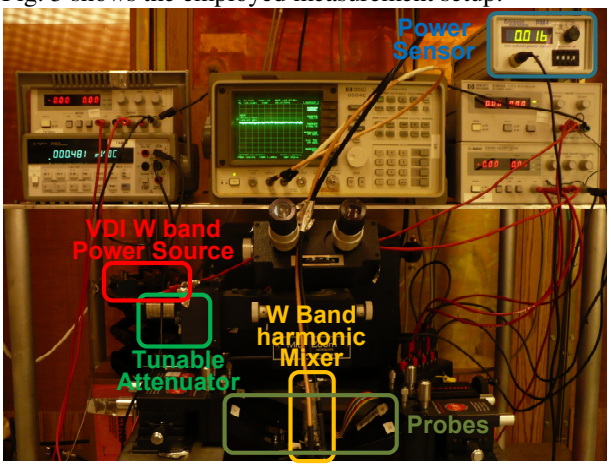


Fig. 5 W-band PA measurement setup

Fig. 6 presents the power amplifier gain versus input signal frequency measured from 4 dies with harmonic mixer. Fig. 6(a) shows measured results with pre-amplifier biased at VDD1=1.4V and the last stage at VDD2=1.0V. Fig. 6(b) shows measured results with pre-amplifier biased at VDD1=2.0V and the last stage at VDD2=1.2V. The PA delivers average 3dB more gain when biased at higher supply conditions due to larger device trans-conductance. Under higher supply setup, the PA delivers >15dB maximum power gain and provides >10dB gain over 20GHz bandwidth (98GHz~108GHz). The test results also validate the wide band matching characteristics of both transformers and power combiner.

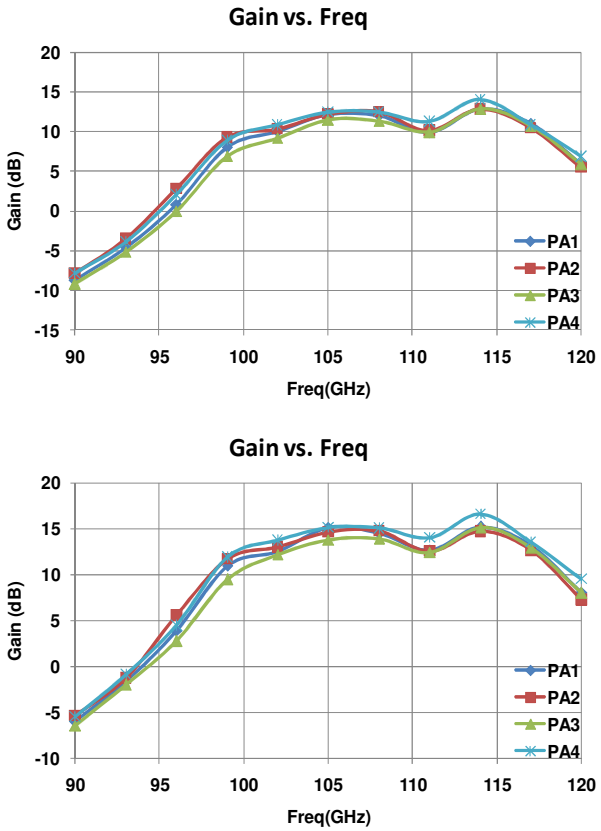
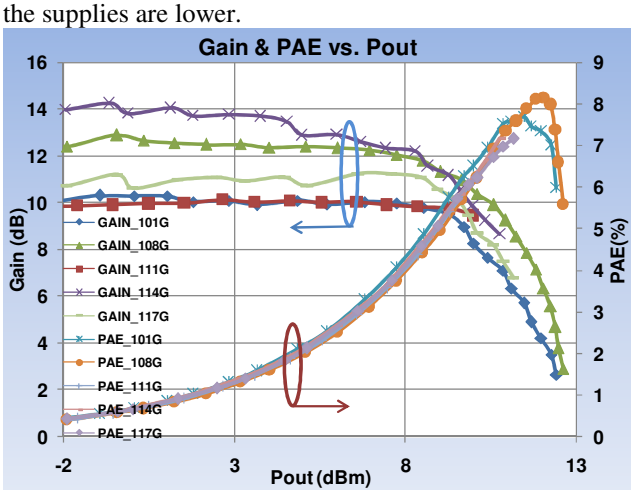
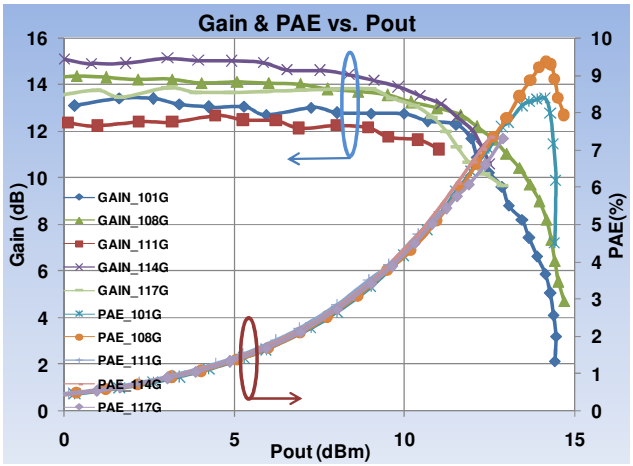


Fig. 6 Measured W-band PA gain under (a) VDD1=1.4V, VDD2=1V (b) VDD1=2V, VDD2=1.2V

Fig. 7 shows the measured power amplifier gain and PAE versus output power under two different supply conditions. The output power at 111GHz is not high enough to measure the OP1dB due to the lower output power of the VDI power source at that specific frequency. The PA OP1dB is about 11.6dBm when VDD1=2V/ VDD2=1.2V, 2.2dB higher than the OP1dB 9.6dBm when the supplies are lower.



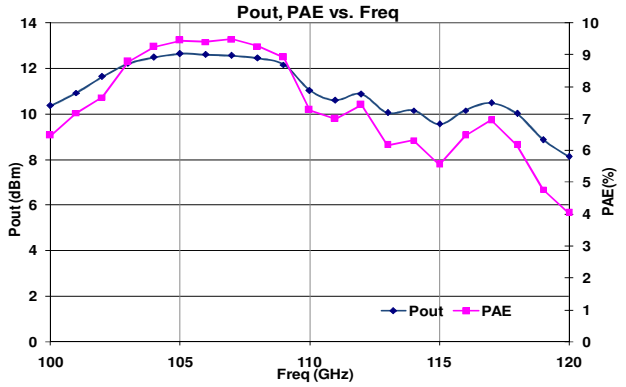
(a)



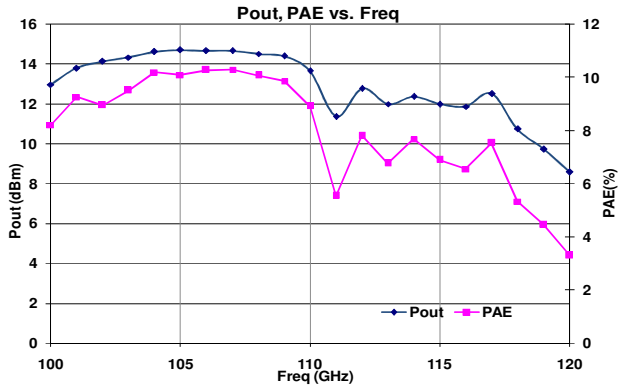
(b)

Fig. 7 Measured W-band PA gain and PAE vs. Pout at 101GHz, 108GHz, 111GHz, 114GHz and 117GHz under (a) VDD1=1.4V, VDD2=1V (b) VDD1=2V, VDD2=1.2V

Fig. 8 shows the measured PA saturated output power and PAE across the frequency from 100GHz to 120GHz. The low saturated output power beyond 111GHz is mainly due to the low source power and a lower PA gain, so as the PAE.



(a)



(b)

Fig. 8 Measured W-band PA saturated output power and PAE across frequency under (a) VDD1=1.4V, VDD2=1V (b) VDD1=2V, VDD2=1.2V

Table I summarizes this current-combined PA performance, and compares its performance with prior arts. Among all, this proposed PA delivers the highest output power with 9.4% PAE beyond 100GHz.

TABLE I. PERFORMANCE SUMMARY AND COMPARISONS

PA technology	Working Frequency	Gain (dB)	Psat (dBm)	Peak PAE (%)	P1dB (dBm)	Core Area(mm2)
This work (VDD1=1.4V, VDD2=1V)	101-117GHz	12.2	12.9	8.2	9.6	0.106
This work (VDD1=2V, VDD2=1.2V)	101-117GHz	14.1	14.8	9.4	11.6	0.106
[1] 90nm CMOS	48-65GHz	7	12.3	8.8	9	0.25 (wi PAD)
[2] 90nm CMOS	58-66GHz	20.6	19.9	14.2	18.2	1.665 (wi PAD)
[3] 65nm CMOS	57-65GHz	18.9/19.2	16.8/17.7	10.8/11.1	13.0/15.1	0.83
[4] 65nm CMOS	57-64GHz	15.8	11.5	11	2.5	0.053
[6] 65nm CMOS	75-95GHz	8.5	6.6	N/A	2.2	N/A

IV. CONCLUSION

A current-combined 101-117GHz W-band CMOS PA has been demonstrated in 65nm CMOS. It achieves 14.8dBm saturated output power with better than 9.4% PAE and larger than 10dB power gain across the frequency band of interest. It further extends the technology frontier and paves the way for future integrated sub-mm-wave high data rate wireless communications and active imaging applications in CMOS technology.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance and support of TSMC for chip fabrication.

REFERENCES

[1]. D. Chowdhury, P. Reynaert, A.M. Niknejad, “A 60GHz 1V +12.3dBm transformer coupled wideband PA in 90nm CMOS,” ISSCC Dig. Tech. Papers, pp.560-561, Feb. 2008

[2]. C. Y. Law, A.-V. Pham, “A high gain 60GHz power amplifier with 20dBm output power in 90nm CMOS,” ISSCC Dig. Tech. Papers, pp. 426-427, Feb. 2010

[3]. J.-W. Lai, A. Valdes-Garcia, “A 1V 17.9dBm 60GHz power amplifier in standard 65nm CMOS,” ISSCC Dig. Tech. Papers, pp. 424-425, Feb. 2010

[4]. W.L. Chan, J.R. Long, M. Spirito, J.J. Pekarik, “A 60GHz band 1V 11.5dBm power amplifier with 11% PAE in 65nm CMOS,” ISSCC Dig. Tech. Papers, pp. 380-381, Feb. 2010

[5]. M. Bohsali, A.M. Niknejad, “Currrent combining 60GHz CMOS power amplifiers,” RFIC Symposium, pp. 31-34, May 2009

[6]. D. Dandstrom, M. Varonen, M. Karkkainen, K. A.I. Halonen, “A W-band 65nm CMOS transmitter front-end with 8GHz IF bandwidth and 20dB IR-ratio,” ISSCC Dig. Tech. Papers, pp. 418-419, Feb. 2010