A 70–78-GHz Integrated CMOS Frequency Synthesizer for W-Band Satellite Communications

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***Abstract*—A 70–78-GHz integrated frequency synthesizer is implemented in 65-nm CMOS. It has been integrated in a two-step zero-IF millimeter-wave transceiver for emerging applications, such as 81–86-GHz satellite communication, short-distance high-speed wireless link, as well as imaging and radar. The transceiver utilizes synthesizer voltage-controlled oscillator (VCO) output as the first $\mathrm{LO_{RF}}$ and 1/8 of $\mathrm{LO_{RF}}$ as the second $\mathrm{LO_{IF}}$ to cover the desired frequency band. The proposed synthesizer adopts integer-N architecture with 50-MHz reference. It also features coarse phase rotation to provide beam-forming capability for the intended transceiver. The synthesizer phase noise (PN) has been measured at 1/8 of the VCO frequency, about -102.2 dBc/Hz @ 1-MHz offset, and the measured reference spur for $\mathrm{LO_{IF}}$ is less than -49 dBc. Thus, the extrapolated PN performance is better than -84 dBc/Hz @ 1 MHz at 70–78 GHz $\mathrm{LO_{RF}}$. The embedded frequency synthesizer occupies 0.16-mm^2 chip area, including the angular rotator and buffers, and consumes 65 mW under 1-V supply.**

***Index Terms*—Frequency synthesizer, injection-locked buffer, millimeter-wave transceiver, multimodulus divider (MMD), phase noise (PN), phase rotation, satellite communication.**

I. Introduction

THE W-band of the electromagnetic (EM) spectrum, ranging from 75 to 110 GHz, has been widely used for millimeter-wave weather radar systems, military targeting, and tracking interferometers and high data-rate wireless links. Its 71–76- and 81–86-GHz segments have been allocated by the International Telecommunication Union (ITU) for satellite services due to orbit congestion at lower frequencies [1]–[3]. Its unique capability to penetrate through fog, cloud, smoke, and dust enables its high potential for radar and imaging applications under poor visibility conditions [4]. Recent research in the 60-GHz wireless personal area network (WPAN) also motivates silicon-based W-band communication system research due to its potential longer range (1–5 km) and higher data-rate ($>$ 10 Gb/s) capabilities, which are suitable for fiber replacement and backhaul applications [5].

Traditional W-band implementations, based upon discrete III–V compound semiconductor components [6]–[8], are bulky and expensive, which greatly limit the cost/weight-effective deployment for emerging applications. On the other hand, CMOS technology has dominated system-on-a-chip (SoC) implementations in a variety of applications: from Bluetooth and wireless local area network (WLAN) to cellular phones [9]–[11]. It has also gained presence in V-band indoor wireless communication systems specified by IEEE 802.15.3c [12]. Recent advancements in deep-scaled CMOS technology have already made it feasible to realize $\sim$ 100-GHz millimeter-wave integrated circuits [13]–[16], such as fixed division ratio phase-locked loops (PLLs) based on $>$ 180 GHz f_T devices. The unsurpassed CMOS integration capability allows incorporation of various functions into a single chip and enables digital assisted design to boost the system performance and reliability. Consequently, CMOS technology can fulfill the quest for low-cost, low-power, and lightweight W-band communication systems.

In this paper, we present a 70–78-GHz frequency synthesizer inserted in a two-step zero IF direct conversion transceiver for W-band satellite communications. Section II describes the architecture of the intended W-band satellite communication transceiver and Section III presents the details of the associated frequency plan and proposed synthesizer architecture. Section IV discusses the synthesizer building blocks circuit design details, as well as the loop optimization. Section V summarizes the experimental results of the synthesizer and some preliminary test data of the transceiver, which is followed by a conclusion in Section VI.

II. W-Band Satellite Communication Transceiver

Direct conversion architecture proves to be very successful in low-frequency CMOS radio SoC [17]. It eliminates the surface acoustic wave (SAW) filter, which otherwise exists in the heterodyne receiver, and realizes compact and low-power radios. However, it is hard to harness in the millimeter-wave frequency range even with digital calibration. One of the key reasons is the excessive quadrature mismatch introduced by the local oscillators (LOs) and up/down conversion mixers, where mutual couplings, including both electric and magnetic, play more detrimental roles compared to its lower frequency counterparts. Two-step zero IF conversion architecture may be a better option by shifting the quadrature modulation/de-modulation to

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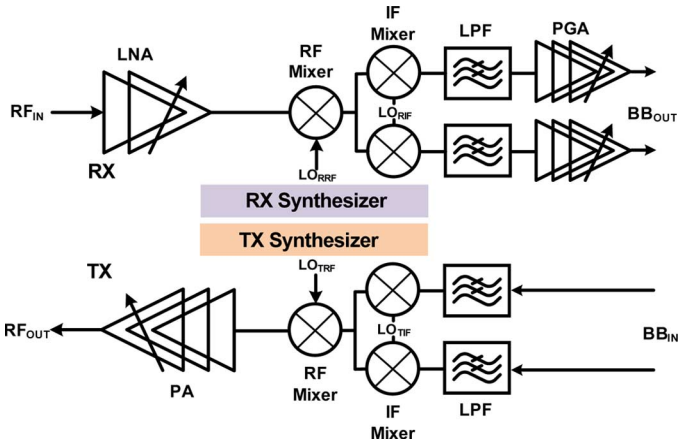

Fig. 1. Block diagram of the proposed two step zero-IF W-band transceiver.

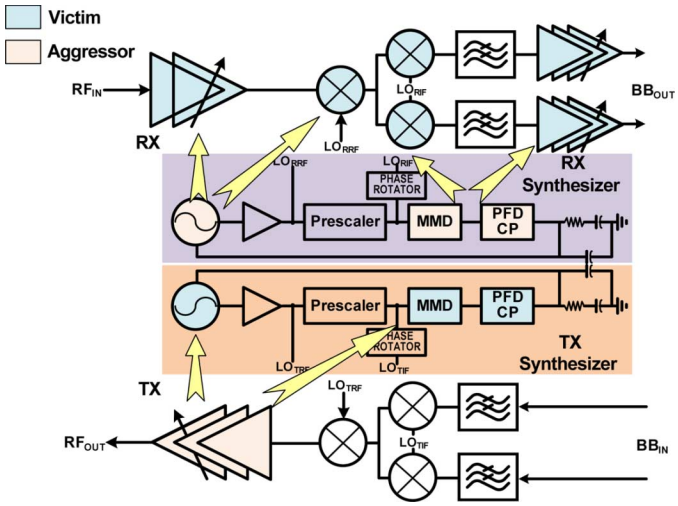

Fig. 2. Transceiver spur generation and coupling map.

a lower IF frequency to alleviate in-phase/quadrature (I/Q) mismatches. However, the IF cannot be too low, which otherwise induces a serious image issue. Fig. 1 shows a block diagram of the proposed two-step zero-IF conversion transceiver architecture for W-band satellite communications. It consists of an RF transmitter (Tx), an RF receiver (Rx), and two frequency synthesizers to drive Tx/Rx separately. An off-chip RF frontend module could support bandpass filtering and Tx/Rx switching between the transceiver and antenna.

During signal receiving, a two-stage low-noise amplifier (LNA) amplifies the incoming 81–86-GHz signal, which is mixed down to a $\sim$ 9-GHz IF by the 70–78-GHz $\mathrm{LO_{RF}}$. The IF signal is then filtered, amplified, and down-converted to an I/Q baseband signal by the quadrature $\mathrm{LO_{IF}}s$. Two low-pass filters with from 1 GHz to $-$3-dB bandwidth, featuring a passive implementation, accomplish low power channel filtering. A baseband programmable gain amplifier (PGA) with 30-dB dynamic range and 6-dB gain step, which employs a Cherry–Hooper amplifier architecture, then amplifies the signal to the full scale of the subsequent ADC. The transmitter processes the signals in the opposite direction. To achieve multigigabit wireless communication in W-band, the LO needs to provide less than 6° integrated root mean square (rms) phase noise (PN) to support a high-quality link with binary phase-shift keying (BPSK)/quadrature phase-shift keying (QPSK) modulations, which can be converted into a PN of -82.5 dBc/Hz at 1-MHz offset frequency with a 1-MHz synthesizer loop bandwidth.

The integrated synthesizer performance can be seriously deteriorated due to the inevitable crosstalk among blocks through shared substrate, common supply/ground, or magnetic/capacitive coupling. Inside the transceiver, each function block can be categorized to be an aggressor or a victim from the spur generation and reception viewpoint, and the building blocks might play opposite roles under different working modes. For example, the frequency synthesizer generates most of the spurs inside the transceiver during receiving and is, therefore, the major aggressor. The voltage-controlled oscillator (VCO) could especially emit as large as $-$30-dBm output at its oscillation frequency. The programmable divider and phase frequency detector (PFD) also generate spurs at harmonics of the reference frequency. All these spurs and their mixing products could deteriorate the receiver signal-to-noise ratio (SNR) once perceived by the receiver chain, as illustrated by Fig. 2.

However, the roles alternate at the transmission mode. Since the on-chip power amplifier delivers as large as 10-dBm output power, it imposes a strong pulling force to other circuit blocks, such as the VCO. To avoid such pulling, an offset frequency plan is desired. Moreover, the strong power amplifier output signal could leak into the supplies of the programmable divider and PFD then stimulate additional in-band spurs due to nonlinear mixing. They could degrade the LO signal quality. Several offset frequency plans have been evaluated. A $2+1$ offset frequency plan can reduce the required VCO frequency. It is, however, hard to deliver accurate quadrature phases at half of the VCO frequency since a small amount of circuit parameter mismatches can produce large quadrature mismatches in such high frequencies. Moreover, inductors might not be avoidable in such a high-frequency divider, which further exacerbates the mismatch due to inevitable magnetic coupling. The large transmitter output can also couple into the synthesizer loop and intermodulate with the harmonics of the (MMD)'s clock and degrade LO PN/spur performance. A $4+1$ offset frequency plan can alleviate the quadrature mismatch by using a resistor load divider at 1/4 VCO frequency, but it requires large power consumption to deliver large enough $\mathrm{LO_{IF}}$ to the IF mixer because the frequency is still beyond 10 GHz. To further reduce $\mathrm{LO_{IF}}$ frequency, we adopted an $8+1$ offset frequency plan, which can provide less LO quadrature mismatch and offer better spur suppression by setting $\mathrm{LO_{IF}}$ to 1/9 of PA output frequency compared with the aforementioned schemes. Fig. 2 elaborates the role of each circuit building block inside the transceiver.

Besides careful frequency planning, several design techniques are utilized to minimize synthesizer spur generation and improve its spur immunity. For instance, differential circuit architecture can greatly reduce its spur generation by more than 6 dB and improve the circuit's immunity to common mode noises. Asynchronous implementation of the digital circuit usually generates much lower spurs compared with its synchronous counterpart due to its less switching activities.

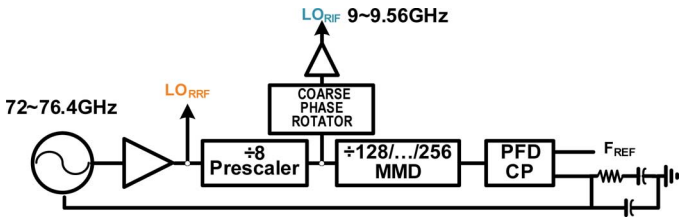

Fig. 3. W-band frequency synthesizer block diagram.

Gated clock in digital implementation is favorable to remove unnecessary spur generations, and physical level optimizations are also viable means, such as deep N-well, double rings, and clean ground isolation, to further isolate various building blocks inside the SoC.

III. Frequency Synthesizer Architecture

Fig. 3 presents the embedded frequency synthesizer detail block diagram, which adopts a third-order type-II integer-N PLL architecture. The synthesizer consists of one differential VCO, covering 70–78 GHz, one LO buffer to drive the following divider and the up/down conversion mixers, a prescaler chain to divide down the frequency to around 9 GHz, an MMD, PFD, charge pump (CP), and an on-chip loop filter. As discussed in Section II, the synthesizer features an $8+1$ offset frequency plan for LO generation. The second LOs are generated through the prescaler and an angular rotator, which not only offers multiple phase options but also serves as $\mathrm{LO_{IF}}$ buffers to ensure enough LO signal strength for the subsequent IF mixers.

The millimeter-wave LO's driving presents another challenge to the integrated synthesizers, which could deteriorate signal integrity and quadrature matching. If a single frequency synthesizer is used to support both the transmitter and receiver, the LO lines could stretch over a long distance ($\sim$ several hundred micrometers) due to the large physical dimension of the transceiver front end. Such long lines not only introduce loss that degrades the LO signal strength, but also result in serious LO mismatches and leakage due to couplings among LO lines and frontend. Moreover, sharing one frequency synthesizer leads to a heavy load to the high-frequency LO buffer and would consume high power to achieve the required LO strength. The alternative solution is to use separate frequency synthesizer to drive the transmitter and receiver individually. This approach drastically shortens the LO driving lines and divides the load, hereby simplifying the LO buffer design and saving power consumption. The power and area cost with two synthesizers can be offset by the savings due to the shortened LO driving lines. Most importantly, this scheme provides a robust LO driving and ensures its signal quality.

IV. Synthesizer Building Blocks

In this section, we describe the design of synthesizer building blocks. First, a wideband VCO is introduced, and the associated isolation schemes are also discussed. Second, a high-frequency LO buffer and its design tradeoffs are analyzed with its demonstrated strong drivability. An angular rotator to support multiple phase LOs is then depicted followed by a description of the pseudodifferential PFD and CP. After that, an asynchronous fully differential implementation of an MMD is detailed to improve the spur generation and immunity. Lastly, we discuss the synthesizer loop optimization.

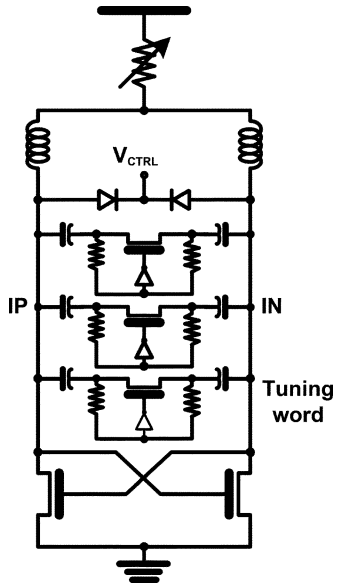

Fig. 4. Wideband VCO schematic.

A. Wideband VCO

The VCO, shown in Fig. 4, needs to support 70–78-GHz oscillation frequency to cover 81–86-GHz satellite communication band. An *LC* cross-coupled architecture with an nMOS only switching pair is utilized instead of complementary pairs [18]. It is because nMOS has higher f_T compared to pMOS transistor and can initialize oscillation with smaller devices [19] that present less capacitance load to the tank for a wide tuning range. Moreover, it allows a larger tank inductor that leads to better PN performance and lower power consumption.

Tank quality is essential to VCO performance. In RF frequency, it is often determined by the on-chip inductor Q, about 6–10 due to the metal series resistance and lossy substrate. The inductor quality factor improves with the increased operation frequency and could achieve $Q > 20$ in the millimeter-wave regime due to the large reactance at high frequencies [20]. To further improve its quality factor, a slow wave technique [21] has been applied to reduce the inductor dimension and series resistance.

The capacitive components are utilized for continuous and discrete frequency tuning. They often have a high Q in low frequencies, which drops dramatically with increasing frequency and could limit VCO tank quality in millimeter-wave frequencies. To achieve a high Q, accumulation-mode nMOS varactors are normally used for continuous frequency tuning [22], [23]. Fig. 5(a) depicts the cross section of a MOS varactor with parasitic components, and Fig. 5(b) exemplifies the MOS varactor implementation. The varactor can be optimized based upon the tradeoffs among the MOS varactor's channel length and width, source/drain resistance, gate resistance, and varactor capacitance to achieve a high Q and maintain a decent $C_{\mathrm{MAX}}/C_{\mathrm{MIN}}$ ratio for VCO tuning [24]. In this VCO, we use

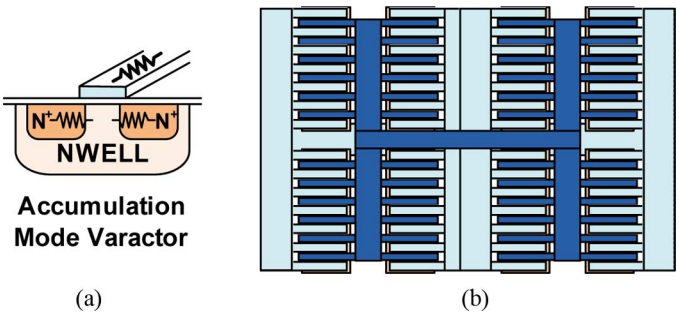

Fig. 5. Varactor. (a) Cross-section figure. (b) Multifinger realization.

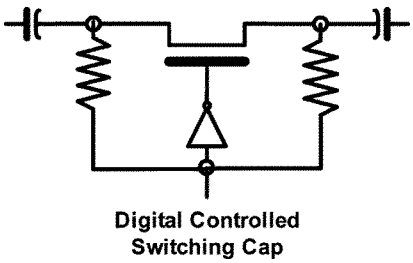

Fig. 6. Digital switch cap schematic.

$16 \times 0.65\ \mu$m/0.06-μm accumulation mode MOS varactors that achieve around $Q = 7$ and $C_{\rm MAX}/C_{\rm MIN} = 1.8$ by simulations.

Digital switch capacitor banks are used to further extend the VCO tuning range and lower the $K_{\rm VCO}$ for better PN. Compared to a single-ended MOS switch capacitor, a differential MOS switch capacitor has a higher Q by reducing the switch series resistance by half. However, it suffers from the issues such as unwanted differential MOS transistor turn-on during the off state and possible device punch-through to degrade the switching cap quality factor [25]. To mitigate these problems, two carefully sized high-value resistors are used to bias the MOS transistor, as shown in Fig. 6. When the switch cap is on, the bias voltage sets to zero to ensure the MOS transistor is on effectively; when the switch cap is off, the bias voltage sets to VDD so that the active MOS switch has a VDD + 1 threshold voltage margin to be turned on, which is hard to reach by the ac coupled signals from VCO outputs. It is preferable to use passive resistors for biasing than active devices because the parasitic diodes in active bias circuitry could limit the VCO output swing and degrade the PN.

3-bit digital switch capacitors are used to extend the VCO tuning range to $\pm 6.7\%$ to cover the required 70–78 GHz. Fig. 7(a) shows the simulated VCO tuning curve that covers 70–82 GHz with 4.1 GHz/V $K_{\rm VCO}$, which agrees well with the measurement results, as shown in Fig. 7(b) with 69–78-GHz tuning range and 3.72-GHz/V $K_{\rm VCO}$. The slightly narrower tuning range and lower $K_{\rm VCO}$ is possibly due to inaccurate device modeling and higher than expected parasitic capacitance.

In addition, we use a digital switched resistor bias network in the VCO core to eliminate possible flicker noise contribution from active bias circuits [26]. It also enhances its high-frequency supply rejection ratio due to smaller coupling capacitance across the resistor between the supply and VCO core. The

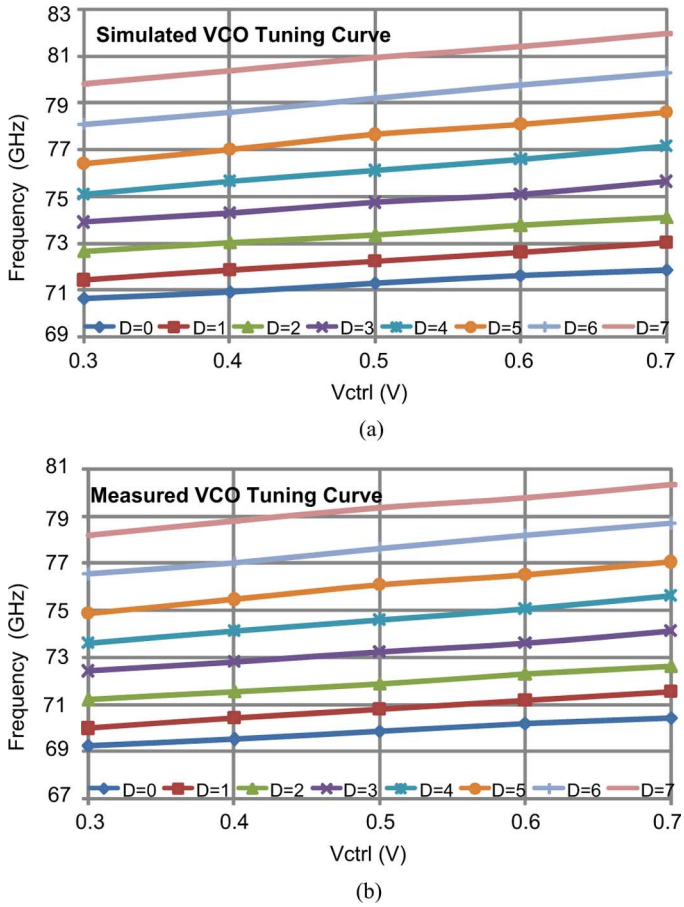

Fig. 7. (a) Simulated and (b) measured VCO tuning curves.

VCO inductor is enclosed by a ground ring to improve the modeling accuracy and an interdigitated switching transistor layout is adopted to reduce their mismatches and associated PN contribution. The simulated VCO PN is from the measurement at 1/8 VCO frequency with -96 dBc/Hz @ 1-MHz offset. It is about 3 dB better than the derived PN performance from the measurement at 1/8 VCO frequency with -111.15 dBc/Hz @ 1 MHz.

B. Injection-Locked Buffer

The VCO can hardly drive the subsequent prescaler and up/down conversion mixers due to tuning range and PN requirement. It necessitates a buffer to isolate the VCO to reduce the capacitance load and mitigate the kickback noise. A differential amplifier, shown in Fig. 8(a), is normally used to buffer the high-frequency signal and isolate the VCO. The cascode stage is inserted to reduce the capacitance load and improve isolation by mitigating the Miller effect. However, this approach requires high power consumption to support desired signal strength in millimeter-wave frequencies and still presents significant load to the VCO. Fig. 8(b) shows the proposed injection-locked buffer. Different from the traditional direct buffer, it purposely adopts negative impedance generated by two cross-coupled transistors to boost the tank Q and the signal strength [27]. When the negative impedance is small and cannot offset the tank real impedance, it serves as a Q booster and enhances the equivalent tank resistance to allow

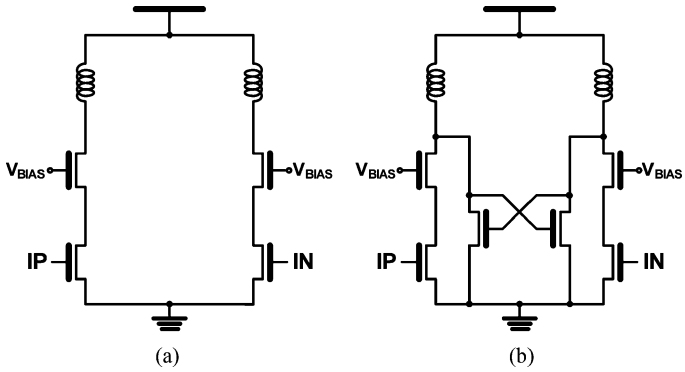

Fig. 8. Schematics of: (a) direct and (b) injection-locked buffers.

a small amplification stage. When the negative impedance is sufficiently large to offset the tank real resistance, it combines with the tank load to form an oscillator and can be injection locked to the desired frequency.

Assuming the tank is formed by the parallel L, C, and R_p [27], where L is the tank inductance, C is the tank capacitance, and R_p is the tank parallel impedance at its resonant frequency, the direct differential buffer's gain G can be expressed as (1). The buffer output signal amplitude $V_{\rm amp}$ is determined by the amplifier bias current $I_{\rm Bias}$ and tank impedance product. Both follow the tank impedance profile

$$G = \sqrt{\frac{I_{\rm Bias} W_{\rm amp} C_{\rm ox}\mu}{2L_{\rm amp}}} \frac{j\omega R_p L}{R_p - \omega^2 R_p LC + j\omega L}$$
$$V_{\rm amp} = \frac{I_{\rm Bias}}{2} \frac{j\omega R_p L}{R_p - \omega^2 R_p LC + j\omega L} \quad (1)$$

where $W_{\rm amp}$ and $L_{\rm amp}$ are the buffer input device's width and length.

When the Q booster is inserted as the cross-couple transistors in Fig. 8(b), it generates negative impedance $-\sqrt{2L_{\rm neg}/I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}$, where $I_{\rm neg}$ is the Q booster bias current, $W_{\rm neg}$ and $L_{\rm neg}$ are the Q booster devices' width and length. It offsets the tank resistance loss and enhances its impedance up to

$$\frac{j\omega L R_p \sqrt{\frac{2L_{\rm neg}}{I_{\rm neg}W_{\rm neg}C_{\rm ox}\ \mu}}}{(1-\omega^2 LC)R_p\sqrt{\frac{2L_{\rm neg}}{I_{\rm neg}W_{\rm neg}C_{\rm ox}\ \mu}} + j\omega L\left(\sqrt{\frac{2L_{\rm neg}}{I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}} - R_p\right)}.$$

When $\sqrt{2L_{\rm neg}/I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu} > R_p$, it presents as an LC tank with inductor quality of

$$Q = R_p \frac{\sqrt{\frac{2L_{\rm neg}}{I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}}}{\left(\sqrt{\frac{2L_{\rm neg}}{I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}} - R_p\right)}\omega L.$$

With the boosted quality factor of

$$Q = \frac{\sqrt{\frac{2L_{\rm neg}}{I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}}}{\left(\sqrt{\frac{2L_{\rm neg}}{I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}} - R_p\right)}.$$

In other words, to achieve identical peak amplitude and gain, the bias current can be reduced to $\left(1 - R_p \Big/ \sqrt{2L_{\rm neg}/I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}\right) I_{\rm Bias}$, and the amplification nMOS channel width can also be reduced to $\left(1 - R_p \Big/ \sqrt{2L_{\rm neg}/I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}\right) W_{\rm amp}$ given identical device channel length $L_{\rm amp}$. It implies the equivalent input capacitance is decreased $1/\left(1 - R_p \Big/ \sqrt{2L_{\rm neg}/I_{\rm neg}W_{\rm neg}C_{\rm ox}\mu}\right)$ times.

When the generated negative impedance overly offsets the tank resistance, the tank evolves into an oscillator. If its self-oscillation frequency is close to the VCOs, it can be injection locked and serve as a high-frequency buffer with large output swing. The buffer working range can be defined by the injection-locking range expressed by (2) [28], [29]

$$\Delta\omega_m = 2 \times \frac{\omega_0}{Q_{\rm tank}} \sqrt{\frac{P_{\rm inj}}{P_0}} = \frac{\omega_0 I_{\rm inj}}{Q_{\rm tank} I_{\rm neg}} \quad (2)$$

where $Q_{\tan k}$ refers to the passive LC tank quality and equals to $R_p/\omega L$, and $I_{\rm inj}$ stands for the injection signal strength that is determined by $\sqrt{I_{\rm Bias}W_{\rm amp}C_{\rm ox}\mu/2L_{\rm amp}}V_{\rm vco}$, where $V_{\rm vco}$ is the VCO output signal amplitude. $V_{\rm vco}$ is normally large enough to drive the injection device fully on/off so $I_{\rm inj}$ approximately equals to $I_{\rm Bias}$. Thereby, the injection-locking range is determined by the bias current ratio of the injection stage and the negative impedance generation stage, and because only injection current affects the locking range, the injection stage transistor can be small with large injection voltage signals to reduce the loading to the VCO.

Due to the frequency difference between the VCO and the injection locked buffer self-oscillation, it induces a phase discrepancy between their outputs as described by (3) [28], [29]

$$\Delta\varphi = \sin^{-1}\left(2 \times \frac{\omega_{\rm vco} - \omega_0}{\Delta\omega_m}\right). \quad (3)$$

The final output amplitude is the vector sum of the injection signal and self-oscillation signal at the injection frequency, which can be expressed as (4) and is equivalent to the multiplication of the tank impedance with the vector sum of the injection current and the negative impedance generation current

$$V_{\rm out} = \sqrt{\frac{\left(i_{\rm Bias}^2 + i_{\rm neg}^2 + 2i_{\rm Bias}i_{\rm neg}{\rm Cos}\left(\Delta\varphi\right)\right)}{1 + Q^2\left(1 - \frac{\omega^2}{\omega_0^2}\right)^2}} \times R_p. \quad (4)$$

It suggests the profile of the injection-locked buffer output amplitude is inconsistent with that of the tank impedance. Fig. 9(a) draws the predicted direct differential buffer and injection-locked buffer amplitude profile based upon (1) and (4). Fig. 9(b) presents the simulated amplitude profiles of both buffers, whose amplitudes are saturated in the frequencies around 75 GHz due to the limited supply voltage. This introduces the difference between the analytical and simulated amplitude profiles, and both results show the direct buffer has a wider frequency range than the injection-locked one. It is because the injection-locked buffer has a higher equivalent tank Q due to the inserted Q booster circuit. However, the injection-locked buffer's input stage transistor size is only one-third of its direct differential buffer counterpart, which renders smaller capacitance load for the VCO to increase the

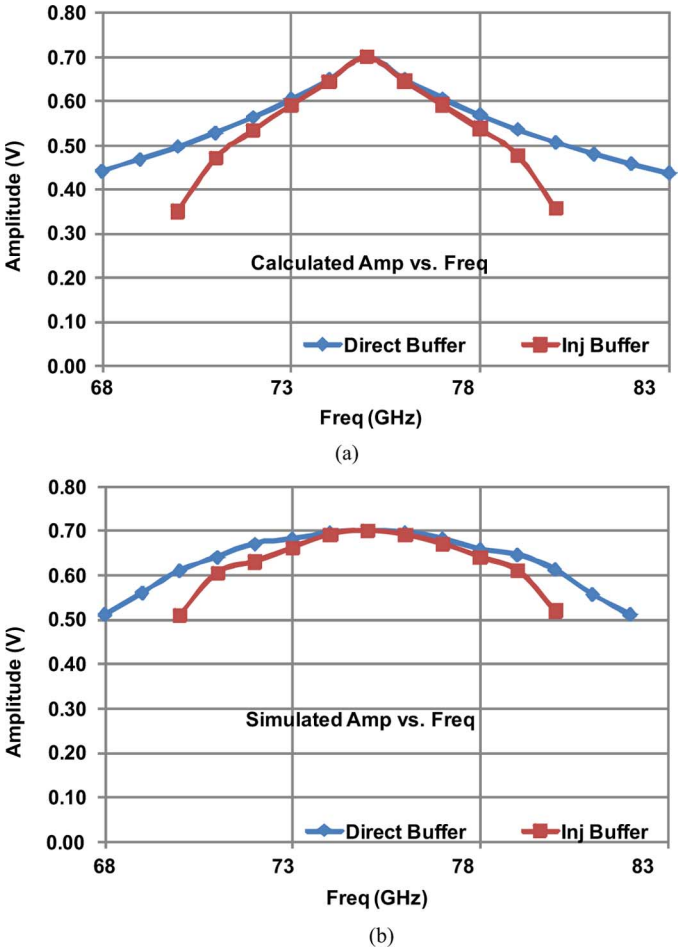

Fig. 9. (a) Calculated and (b) simulated output amplitudes of the direct buffer and the injection-locked buffer.

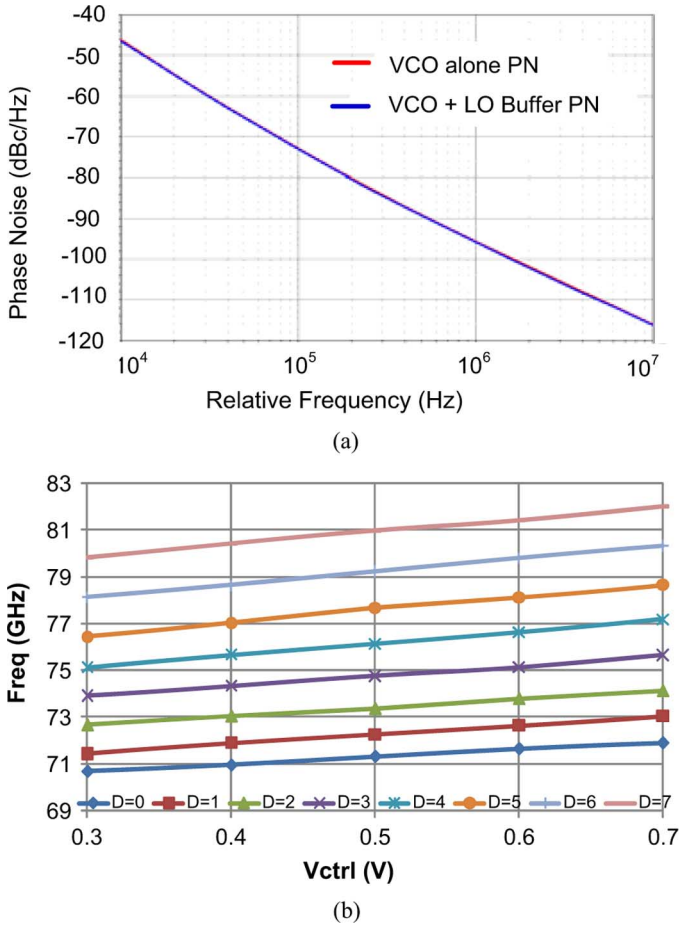

Fig. 10. (a) Simulated PNs of VCO alone and VCO plus buffer. (b) Simulated tuning curves of VCO plus injection-locked buffer.

tank inductance and further improve PN. As to the power consumption, the injection-locked buffer does not have advantages over the direct differential buffer since both need to deliver large output swing through the identical lossy *LC* tank. In our design, the injection-locked buffer burns 1-mA ($\sim 10\%$) more current to provide the wide locking range and sufficiently large LO signals.

To ensure the synthesizer function properly, a 3-bit digital switch capacitor bank is also incorporated into the proposed injection-locked buffer to increase the effective injection locking range. It covers the VCO tuning range by more than $\pm 15\%$. Since the buffer is injection locked, it introduces negligible PN degradation, which can be verified from simulation results, shown in Fig. 10(a). This figure presents and compares the simulated PN performance of the VCO alone and the VCO together with the buffer. Fig. 10(b) shows the simulated tuning curve of the VCO and injection-locked buffer with a mixer load and equivalent parasitic, which demonstrates enough frequency cover range and LO signal amplitude.

C. Prescaler and Phase Rotator

One of the biggest challenges in a millimeter-wave frequency synthesizer is the high-frequency division after the VCO. Since the CMOS static divider cannot function properly at such a high frequency, the division generally involves a cascaded injection-locked divider chain. It takes significant effort to optimize each divider to securely cover the desired frequency with a safe margin such as $\pm 15\%$. Reference [30] covers wide bandwidth of $>$ 29 GHz, but it consumes more than 60-mW dc power. Reference [31] requires multiple inductors with the cost of a large chip area. In this synthesizer, the 70–78-GHz VCO signal is first divided by eight, through an injection-locking method, into 8.75–9.75-GHz signals that are further divided down to the reference frequency by a static programmable divider for optimum power consumption and chip area tradeoffs. Traditional injection-locked dividers, as shown in Fig. 11(a), do not fully utilize the differential inputs. It not only requires a dummy block to provide a symmetrical load to the previous stage, which otherwise degrades its locking range and supply rejection ratio, but it also has a smaller injection signal that decreases locking range [32]. To improve injection-locking efficiency with fully differential implementation, a complementary injection-locking scheme is adopted, as shown in Fig. 11(b), where both pMOS and nMOS use identical dimension for symmetry. It equivalently increases the injected signal voltage swing by 30% due to smaller pMOS mobility. All the dividers adopt digitally controlled bias to adjust the output signal strength across frequency band and process-voltage-temperature corners.

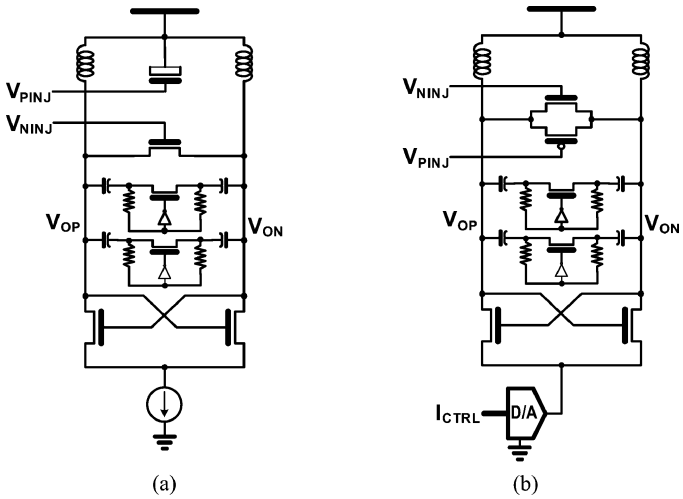

Fig. 11. Schematics of: (a) single nMOS injection-locked divider and (b) complementary injection-locked divider.

To accurately design the frequency range of each injection-locked divider is not trivial. It mandates accurate modeling of the passive components, parasitic interconnects, and the active devices. Unfortunately, foundries seldom support component models for the operation beyond 40 GHz. To obtain a good match between design and actual circuit, and reduce the design iterations, a rigorous design flow is followed. The raw active device models from the foundry are used as the core. Its connection parasitics and interconnects are then extracted by EM simulation tools, such as Ansoft HFSS or ADS momentum, to complement the active device modeling, and all passive components are also simulated by these EM tools. The dividers are then designed and optimized by including all these parasitic. To further ensure design accuracy, the passive components of the entire divider chain are put together to model the cross coupling effect with EM simulations.

A phase rotator is integrated in this synthesizer for the potential phase-array application. It also serves as the buffer delivering a large $\mathrm{LO_{IF}}$ signal to the subsequent up/down IF conversion mixers. An ideal phase rotator needs to synthesize many phase combinations to support a very fine phase array beam steering. Fig. 12(a) demonstrates one realization to support continuous phase rotation with quadrature LO inputs. To maintain a flat output amplitude, the quadrature bias currents need to satisfy $\sqrt{I_{I\mathrm{bias}}^2 + I_{Q\mathrm{bias}}^2} = I_0$, where I_0 is a constant current that determines the output $(\mathrm{LO_{IF}})$ swing. Fig. 12(b) shows the simulated phase tuning curve and the corresponding $\mathrm{LO_{IF}}$ amplitude, which can provide many different output phases. In the actual transceiver design, the continuous control has been simplified into 2-bit digital control that renders a coarse phase rotation with four options.

D. PFD and Charge-Pump Circuits

A fully differential PFD is preferred to reduce spur generation and improve its immunity to supply and substrate noises. However, the fully differential current mode logic configuration tends to degrade PN performance due to a limited signal swing.

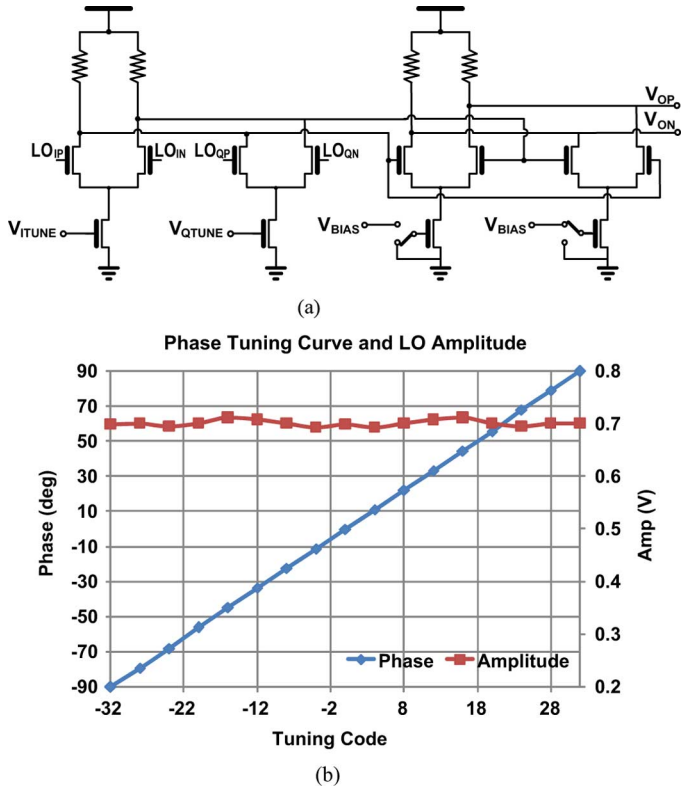

Fig. 12. (a) Schematic of the phase rotator and (b) simulated phase and amplitude tuning curves.

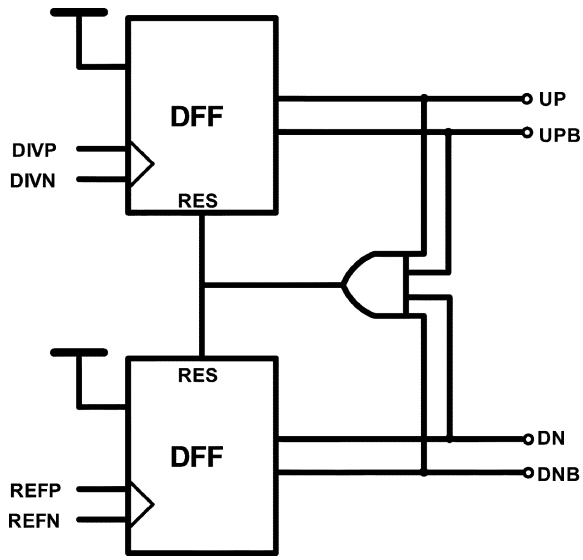

Fig. 13. Diagram of the pseudodifferential PFD.

Therefore, a pseudodifferential architecture is applied instead. It has the similar signal swing as the single-ended approach [25] to deliver comparable PN performance. Furthermore, the generated current spikes are complementary and cancel each other in the first order to alleviate the spur generation. Fig. 13 depicts the PFD diagram, which doubles conventional PFD circuitry to improve the spur cancellation. A small series resistor is also inserted in the supply to further damp the generated and coupled high-frequency spurs.

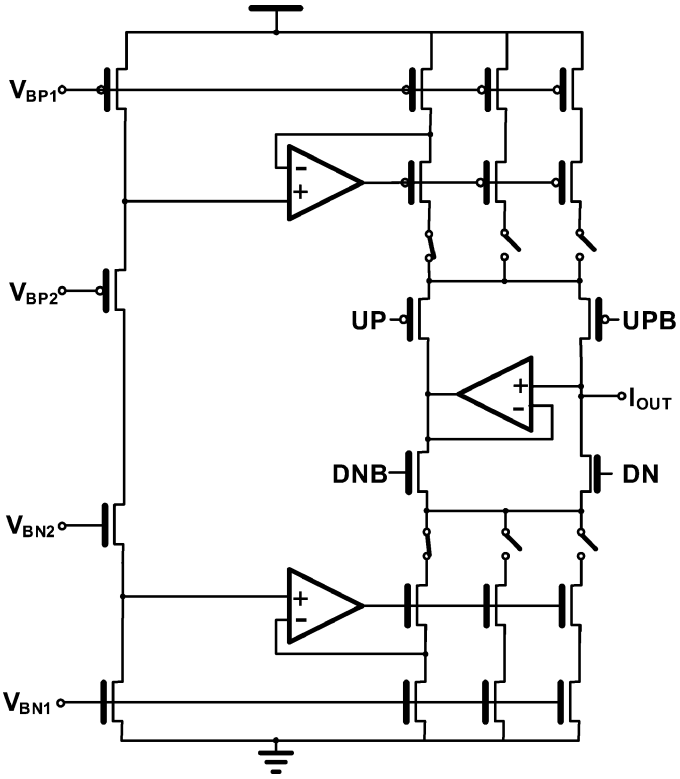

Fig. 14. Differential CP schematic.

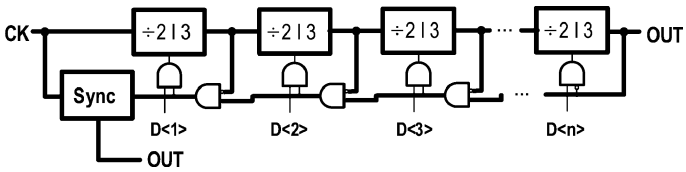

Fig. 15. MMD diagram.

Fig. 14 shows the differential CP schematic, three op-amps are used to match the charge and discharge current so as to reduce reference spurs [33]. On top of that, 3-bit digital control is incorporated to adjust CP current from 100 to 800 μA to optimize synthesizer loop bandwidth and integrated PN performance. To reduce chip pin outs and system form factor, the synthesizer integrates a third-order on-chip loop filter, where multiple-bit digital-controlled resistors and capacitors are used to calibrate process variations.

E. MMD

The programmable counter needs to divide the prescaler output from 8.75–9.75 GHz down to a reference frequency of 50 MHz, which is a large division ratio. To save power, reduce circuit scale and lower generated spur level, an asynchronous MMD architecture is employed, as shown in Fig. 15. However, asynchronous realization tends to accumulate the jitter along the divider chain and degrades PN performance. To mitigate the jitter accumulation for better signal quality, a re-synchronization block with duty cycle adjustment function is added. It ensures the output signal PN improvement by around 6 dB for each divide-by-2.

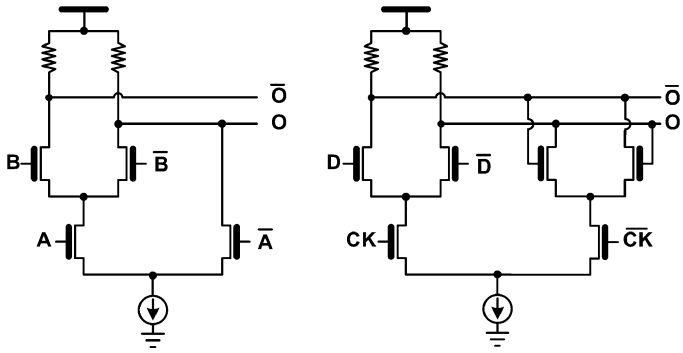

Fig. 16. Differential implementations of nand2 and latch.

Since the MMD is one of the largest spur generators inside the frequency synthesizer and the re-synchronization block is very sensitive to high-frequency spurs that could deteriorate the divided signal PN, a fully differential realization is preferred. Fig. 16 shows the implementation examples of two differential unit cells of the divider: nand2 and latch. The other cells adopt the same differential configuration. This fully differential MMD, including the re-synchronization block, occupies a 0.06-mm^2 active area and consumes 19-mA current from a 1-V supply.

F. Loop Optimizations

Due to a large division ratio ($\sim$ 1500), this frequency synthesizer has more than 60-dB gain to amplify the noises generated by the reference, PFD, and dividers. Unlike synthesizers with small division ratio, where the VCO dominates the PN performance, this synthesizer PN is determined by more than one noise source and it necessitates careful loop design. Moreover, these noises, contributed by different function blocks, experience different noise transfer functions. It leads to a sophisticated optimization of the synthesizer loop bandwidth to trade off each block's noise contribution. To accomplish such optimization, an S-domain model is generated to estimate the PN performance accurately to derive the optimal loop filter with an intended phase margin of 60°. Fig. 17 exemplifies the optimization based upon the simulated PNs of all synthesizer components and partitions the noise contribution from each function block. It reveals that the reference and the CP, together with the loop filter, are the major noise contributors to the -87 dBc/Hz @ 1-MHz offset PN with 700-kHz loop bandwidth. To further improve this synthesizer PN, we can either improve PN of each major noise contributor and/or use a high-frequency reference to reduce the division ratio for a moderate loop gain.

V. Integration and Experiment Results

The synthesizer has been integrated into a W-band communication transceiver. To facilitate physical design, the transceiver can be floor-planned based upon the function block and placed regularly as shown in Fig. 18(a). Such a floor-plan clearly partitions each physical block and conveniently constructs the entire transceiver. However, it might not deliver optimum performance due to the long LO driving lines induced by this regular floor-plan, which not only imposes significant loss to the

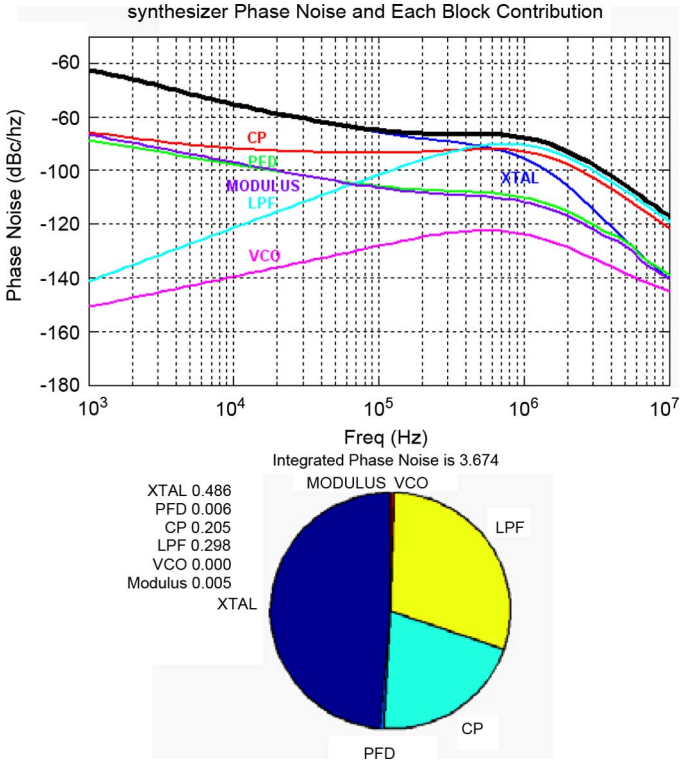

Fig. 17. Simulated synthesizer PN and contribution partitions.

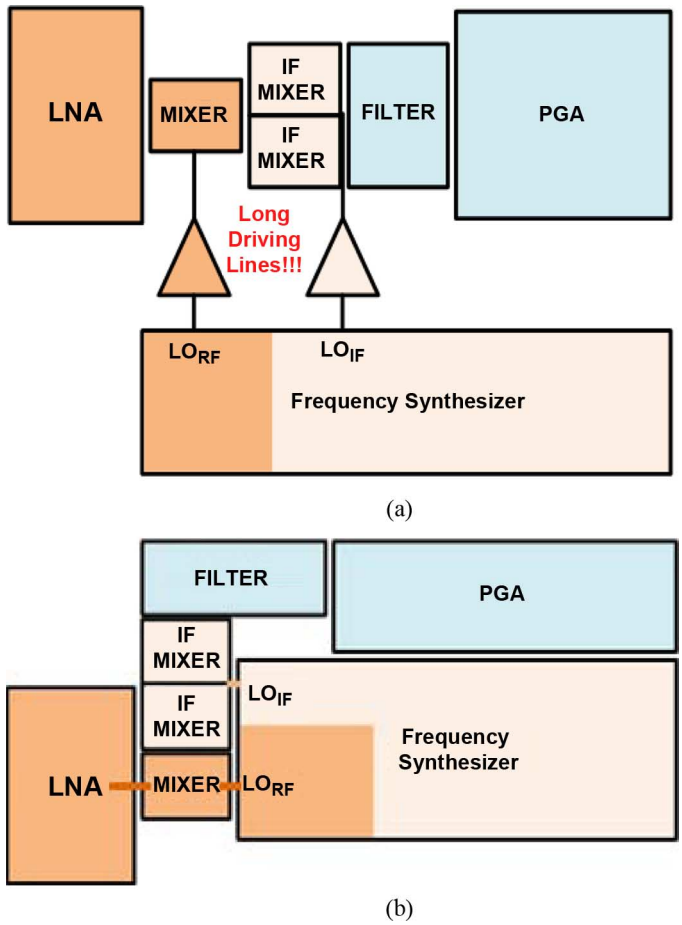

Fig. 18. (a) Traditional transceiver floor-plan. (b) RF/LO centric floor-plan.

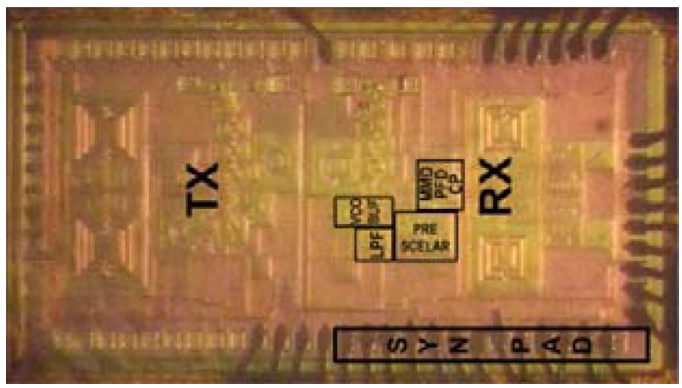

Fig. 19. Die photograph.

LO signals, but also deteriorates the LO matching due to a non-identical environment for them. Such a configuration also introduces complicated cross-coupling among them. Simulation shows long LO driving lines ($\sim$ 500 μm) can introduce more than 3-dB signal loss and the asymmetrical coupling among them can induce more than 10° phase mismatches. Therefore, we propose to implement a signal driven floor-plan for the transceiver, called the RF/LO centric layout. The placement of each block caters to signal stream instead of function, in the priority from high frequency to low frequency. As shown in Fig. 18(b), the connections from the LNA to the mixer and the LO buffer to the RF mixer have the highest priority, hereby with the minimum connection length. The connection from $\mathrm{LO_{IF}}$ to the IF mixer needs to be shortened as much as possible. Finally, the low-frequency analog baseband should be reshaped to accommodate the above interconnects and facilitate a regular transceiver floor-plan. By doing so, we can reduce the LO driving lines to be less than 100 μm. The short lines also decrease the equivalent loading to the buffers and result in more than 40% saving in the buffer power consumption indicated by simulations.

The proposed transceiver has been designed and fabricated in 65-nm CMOS. Fig. 19 shows a die photograph. Since it adopts a signal driven floor-plan, each functional block layout is irregular, but it does achieve the shortest connection for RF and LO signals for optimum performance. The chip occupies a 2.3 $\times$ 1.2 mm^2 chip area including PADs and the embedded synthesizer area is 0.4 $\times$ 0.4 mm^s. To characterize the integrated synthesizer, we use a W-band signal generator to generate desired millimeter-wave signal for the receiver, a spectrum analyzer together with a V-band harmonic mixer (due to lack of W-band harmonic mixer in our laboratory) to measure the generated transmitter output tones, and several low-noise power supplies and batteries.

The synthesizer consumes 65 mW of dc power from a 1-V supply. The power consumption is partitioned as: 8 mW from VCO, 34 mW from perscaler and LO buffers, 3 mW from the CP and PFD, and 20 mW from the MMD and other circuitries. To validate the embedded frequency synthesizer function, a 50-MHz baseband signal has been injected into the transmitter low-pass filter with from 1 GHz to $-$3-dB bandwidth. A continuous wave (CW) tone can be observed from transmitter

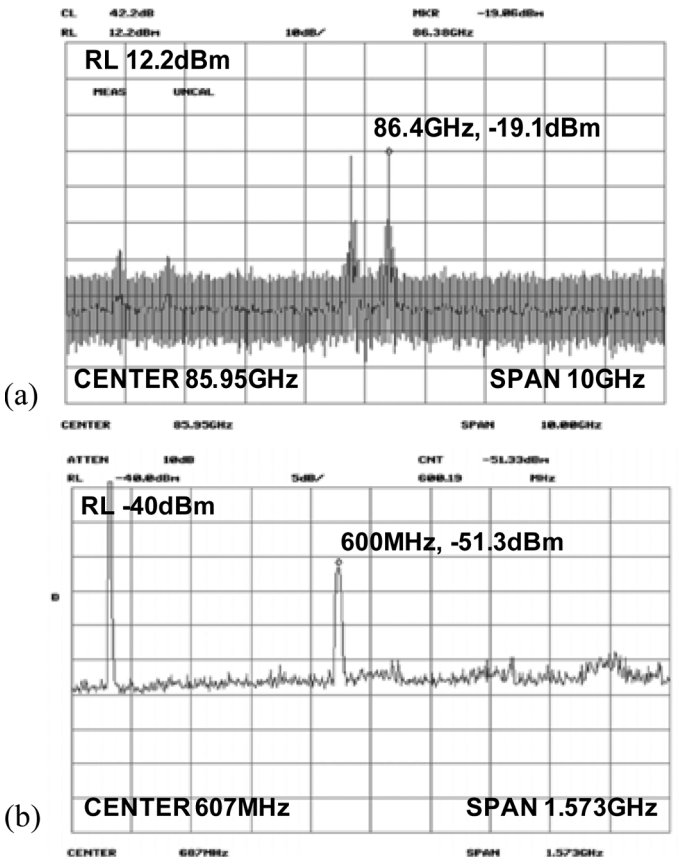

Fig. 20. Measured: (a) TX output tone at 86 GHz and (b) RX baseband (BB) signal at 600 MHz with 85.8-GHz input signal.

output and it can cover the entire 81–86-GHz band. Fig. 20(a) demonstrates the transmitted 86-GHz signal with −19.1-dBm uncalibrated output power reading when the synthesizer RF LO is set at 76.8 GHz. Since we use a harmonic mixer to measure the transmitter output, there are images to its left due to harmonic mixing. A similar measurement is also conducted in the receiver. A high-frequency CW tone, generated by the W-band signal generator, is applied to the LNA directly. The corresponding baseband signal is observed from the PGA output. Fig. 20(b) confirms the demodulated 600-MHz tone with an applied 85.8-GHz signal when the synthesizer is set at 76.8 GHz.

The PN performance has been measured through $\mathrm{LO_{IF}}$ instead of TX output due to excessive setup losses that render a low output power W-band tone with a high noise floor. $\mathrm{LO_{IF}}$ locates at 1/8 of the synthesizer VCO frequency. Fig. 21(a) shows the measured PN of −102 dBc/Hz at 1-MHz offset. Fig. 21(b) shows the PN curve from 10 kHz to 10 MHz with 0.6° integrated rms PN and around 1-MHz loop bandwidth. When the synthesizer loop bandwidth has been shrunk to 100 kHz, the measured PN at 1 MHz is −111.1 dBc/Hz, as shown in Fig. 21(c). It implies the VCO PN is not the dominant factor in this synthesizer, which is consistent with our analysis. To derive the transmitter output PN, which is nine times the measured $\mathrm{LO_{IF}}$ at 8.75–10 GHz, $20 * \log 9 = 19$ dB should be added to represent the worst case $\mathrm{LO_{IF}}$ PN. It derives the transmitter output PN is better than −83 dBc/Hz at 1-MHz offset. Fig. 21(d) shows the

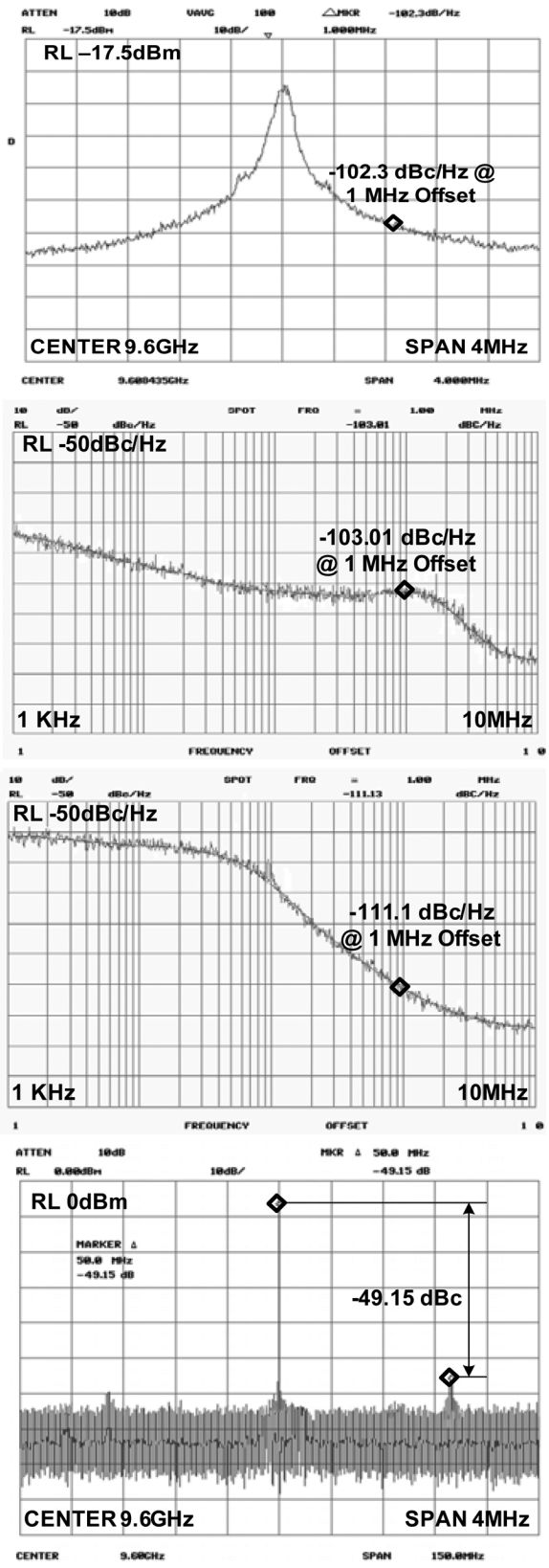

Fig. 21. Measured: (a) spot PN @1 MHz, (b) PN with 1-MHz loop bandwidth, (c) PN with 100-kHz loop bandwidth, and (d) reference spur from $\mathrm{LO_{IF}}$.

measured reference spur of $\mathrm{LO_{IF}}$ is less than −49 dBc. Fig. 22 shows the measured LO frequencies from the transmitter output and the corresponding digital control word for the VCO. It also

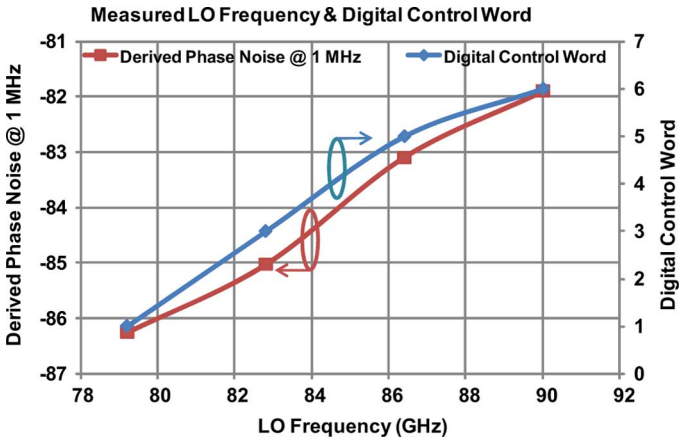

Fig. 22. Measured LO frequencies from the transmitter output and the corresponding digital control word for the VCO and the derived PN @ 1-MHz offset.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Divisions	256	256/258/260/262	512~8184	***1024~1984***
Phase Noise (dBc/Hz)	-75.9dBc/Hz @1MHz	-75.3dBc/Hz @1MHz	-75dBc/Hz @1MHz	***-83dBc/Hz @1MHz***
Reference Spurs (dBc)	-51.8	-46	-42	***-49***
Supply (V)	1.2	1.5	1.1	***1***
Power (mW)	43.7	105	76	***65***
Area (mm^2) (core)	0.7 (Wpad)	0.56 (core), 1.69(Wpad)	0.82 (Wpad)	***0.16***
Technology	65nm CMOS	0.13um CMOS	45nm CMOS	***65nm CMOS***

shows the derived PN at 1-MHz frequency offset according to the measured PN at LO_{IF}.

VI. CONCLUSION

An integrated frequency synthesizer, which drives the transceiver operating at 81–86 GHz for satellite communications, is realized in TSMC 65-nm general-purpose (GP) CMOS technology. Table I summarizes measured performance versus those of prior developments in a similar frequency range [15], [34], [35] based on deep-scaled CMOS technologies. This frequency synthesizer clearly demonstrates its performance advantages in a wider frequency range, better PN, and more compact design to facilitate the transceiver SoC solutions for various applications, including satellite communications, high-speed wireless data link, imaging, and radar, etc. Its slightly higher power consumption than that of [15] is primarily due to its much wider frequency coverage and extra integration of phase rotators and Tx/Rx LO buffers.

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power amplifier and front-end module markets (currently exceeding one billion units/year). Throughout his career, his research has primarily focused on the development of high-speed semiconductor devices and integrated circuits for RF and mixed-signal communication and imaging system applications. He was the Principal Investigator with the Rockwell Science Center, leading the Defense Advanced Research Projects Agency (DARPA)'s ultrahigh-speed ADC/DAC development for direct conversion transceiver (DCT) and digital radar receiver (DRR) systems. He was the inventor of multiband reconfigurable RF-interconnects, based on FDMA and CDMA multiple access algorithms, for ChipMulti-Processor (CMP) inter-core communications and inter-chip CPU-to-memory communications. He also pioneered the development of the world's first multigigabit/s ADC, DAC, and DDS in both GaAs HBT and Si CMOS technologies; the first 60-GHz radio transceiver front-end based on transformer-folded-cascode (Origami) high-linearity circuit topology; and the low phase-noise CMOS VCO ($\mathrm{F.O.M.} < -200\,\mathrm{dBc/Hz}$) with a digitally controlled on-chip artificial dielectric (DiCAD). He was also the first to demonstrate CMOS oscillators in the terahertz frequency spectrum (1.3 THz) and the first to demonstrate a CMOS active imager at the sub-millimeter-wave spectra (180 GHz) based on a time-encoded digital regenerative receiver. He was also the founder of the RF design company G-Plus (now SST and Microchip) to commercialize WiFi 11b/g/a/n power amplifiers, front-end modules, and CMOS transceivers.

Dr. Chang was elected to the U.S. National Academy of Engineering in 2008 for the development and commercialization of GaAs power amplifiers and integrated circuits. He was the recipient of the IEEE David Sarnoff Award in 2006 for developing and commercializing HBT power amplifiers for modern wireless communication systems. He was the recipient of the 2008 Pan Wen Yuan Foundation Award and 2009 CESASC Career Achievement Award for his fundamental contributions in developing AlGaAs/GaAs HBTs. His recent paper "CMP Network-on-chip Overlaid with Multiband RF-Interconnect" was selected for the Best Paper Award of the 2008 IEEE International Symposium on High-Performance Computer Architecture (HPCA). He was the recipient of the Rockwell Leonardo Da Vinci Award (Engineer of the Year) in 1992, the National Chiao Tung University Distinguished Alumnus Award in 1997, and the National Tsing Hua University Distinguished Engineering Alumnus Award in 2002.