# D-Band CMOS Transmitter and Receiver for Multi-Giga-Bit/sec Wireless Data Link

Zhiwei Xu, Qun Jane Gu, Yi-Cheng Wu, Adrian Tang, Yu-Ling Lin*, Ho-Hsian Chen*, Chewnpu Jou*, Mau-Chung Frank Chang
EE Department, University of California, Los Angeles, CA90024, USA
*Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, R.O.C.

***Abstract* -We present the design and test results for D-band CMOS transmitter (Tx) and receiver (Rx) for ultra-high speed and short distance data communications. The Tx/Rx employs modulation/de-modulation based on Amplitude-Shift Keying (ASK) to facilitate a non-coherent data link without power-hungry PLL, data converters, and complex DSP. The Tx consists of a wideband 131~140GHz VCO along with an On/Off key controlled power amplifier to achieve >90% ASK modulation; the Rx consists of a digital controlled LNA, an envelope detector (ED) and a programmable gain amplifier (PGA) to achieve >60dB dynamic range. Both Tx and Rx are implemented in 65nm CMOS and occupy an active area of 0.03mm$^2$/0.12mm$^2$. Test results validate linkage data rates up to 2.5Gbps at the carrier frequency of 140GHz with Tx/Rx power consumption of 115mW/120mW, respectively.**

## I. INTRODUCTION

D-band (110~170GHz) has been allocated for digital communication, radar, and imaging applications due to its unique ability to penetrate through fog, dust and fabrics. Traditionally, systems implemented in this spectrum range have been realized using discrete components based on less accessible technologies such as GaAs or InP HBTs and HEMTs, which inevitably lead to large form factor and high cost.

Recent circuit development based on deep-scaled CMOS continues to push the circuit/system applications into the higher frequency regime with broader bandwidth by monolithically integrating the mm-Wave front-end and the baseband digital signal processor for smaller form factor and less power consumption. It has been proven that 65nm CMOS can support >200 GHz frequency division [1], 192GHz fundamental frequency oscillation [2] and 140GHz CMOS receiver front-end for imaging applications [3].

In this paper, we report the first demonstration of an integrated Tx/Rx link that can operate up to 2.5Gbps wirelessly for short distance (<10cm) data link applications via a 140GHz carrier. Such applications encounter increasing demands under space-limited, cable-bandwidth-limited and reliability/cost-constrained conditions for board-to-backplane, board-to-board and chip-to-chip and even on-chip communications [4].

## II. D-BAND TRANSMITTER AND RECEIVER ARCHITECTURE

Fig. 1 depicts the top-level block diagram for the Tx and Rx, respectively, intended for short distance data links. In Tx, a VCO made of a regular resonance tank in stacking with a novel negative-resistance tank, which will be detailed in section III-A, is devised to generate ultra-high carrier frequencies from 131GHz to 140GHz with a 2-bit binary digital control for frequency selection. An input data buffer is utilized to control the digital input signal and modulate the amplified VCO output for achieving the desired >90% modulation index through a single stage Class-B power amplifier that is detailed in Section III-B. The buffered modulator is designed to support up to 10GHz data bandwidth.

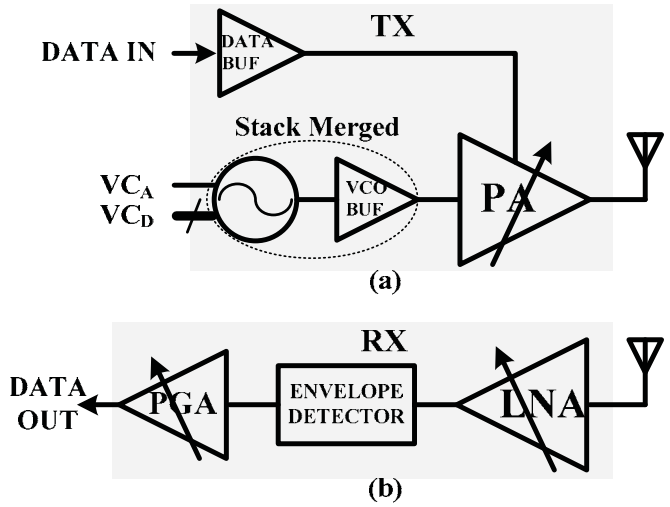


Fig. 1 Block Diagram of D-band (a) Transmitter (b) Receiver

The receiver features a three stage differential LNA with 18dB gain range, followed by a sensitive envelope detector with external adjustable offset-voltage to down-convert the receiving signal into the baseband. Subsequently, a seven-stage PGA with a DC offset cancellation is implemented to offer a total 42dB dynamic range with 6dB gain step. The DC cancellation corner is carefully designed to be under 1MHz.

Since the Tx and Rx communicate via a non-coherent modulation/demodulation scheme, there will be no need for a frequency synthesizer in the intended data link. Consequently, it minimizes the Tx/Rx power and area consumptions by eliminating the PLL and other building blocks for frequency synthesis/synchronization, ultra-high speed frequency dividers, high linear up/down conversion mixers and AD/DA converters, as well as other power hungry timing recovery circuits.

In this intended non-coherent communication scheme, even though the Tx carrier frequency may deviate substantially from the intended carrier frequency due to frequency drifts of the

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unlocked VCO and process variations, the data link may still be secured because the Rx is insensitive to the carrier frequency so long as the transmitted signal spectrum falls into the purposely designed LNA frequency range of about 5GHz. This simple communication scheme may prove itself to be robust as very few strong jammers can be present due to limited D-band transmission power from interfering sources and limited interfering range due to high atmospheric attenuation.

## III. Circuit Design

### *A. D-Band Voltage Controlled Oscillator (VCO)*

Although technology scaling has boosted both $f_T$ and $f_{max}$ of 65nm digital CMOS to about 200GHz and 240GHz, respectively, physical drawbacks in CMOS such as the substrate loss, gate resistance, and circuit parasitic still limit its maximum operation frequency. It is difficult for traditional cross-coupled VCO to achieve oscillation near its intrinsic cut-off frequencies due to the extra load introduced by device/interconnect parasitic. For instance, 5um-width active devices should supposedly resonate with less than 40pH inductance to obtain 140GHz self-resonant frequency. However, such low inductance value will render the tank impedance too low to oscillate.

As a result, a new circuit architecture is required to boost the tank resonant impedance and simultaneously allow the use of a low inductance in the resonance tank to obtain high resonant frequency. Such oscillator circuitry is devised and demonstrated in Fig. 2 (a) by stacking a negative-resistance tank in parallel to the traditional resonant tank to boost the fundamental oscillation frequency. The detailed circuit operation mechanism can be analyzed as follows:

The stacking resonant tank consists of a conventional tank with $L_{\tan k}$ shunt between two drains of the bottom cross coupled pair and a stacking negative-resistance tank with $L_g$ shunt between two cascode devices at the top of the oscillator. Consequently, the newly devised stacking architecture can tolerate larger $L_{\tan k}$ and $L_g$ inductances by combining them via the cascode devices to form a hybrid tank with effectively lower inductance to support oscillations at the higher frequencies. Moreover, due to the fact that the negative-resistance parallel tank has boosted the overall stacking resonator impedance, it eases the demand on the cross-coupled device's $g_m$, hence allowing smaller NMOS devices to further increase the oscillation frequency. Because the added negative resistance parallel tank shares the same current with the regular tank, it consumes no extra power. It not only saves the current consumption by sharing the VCO current, but also effectively decreases the VCO load by decoupling the subsequent stage from the oscillator core, thus enabling higher oscillation frequency and a faster communication data rate.

The mechanism can be further detailed in Fig.2 (b) and (c). The regular tank shown in Fig. 2(b) is a cross couple structure similar to that of traditional oscillators. It would deliver a higher oscillation frequency than $1/\sqrt{L_{\tan k}C_{\tan k}}$ and boost the tank impedance by stacking the negative-resistance tank (Fig. 2(b)). This can be elaborated by assessing the small signal input impedance at the cascode source:

$$Z_{in}=\frac{1-(C_{gs}/2)L_g\omega^2}{g_m/2}\left\|\frac{1-(C_{gs}/2)L_g\omega^2}{j\omega(C_{gs}/2)}\approx\frac{-C_{gs}L_g\omega^2}{g_m}\right\|j\omega L_g \quad (1)$$

At operation frequencies beyond $\sqrt{2/(L_gC_{gs})}$, the imaginary part of Eq. (1) shows an inductor with effective inductance of $L_g$, in parallel with bottom regular tank inductor $L_{\tan k}$ to obtain a combined equivalent inductance of $L'_{\tan k}=L_{\tan k}\,//\,L_g$, which in fact can be substantially reduced to enable a much higher resonant frequency possibly even beyond the cut-off frequency of the device. Meanwhile, its real part results in a negative impedance to boost the combined equivalent tank impedance, $R'_p=R_p\left\|\left(-C_{gs}L_g\varpi^2/g_m\right)\right.$, which in turn allows the use of smaller cross coupled devices to facilitate stable oscillation with relaxed $g_m$ requirement.

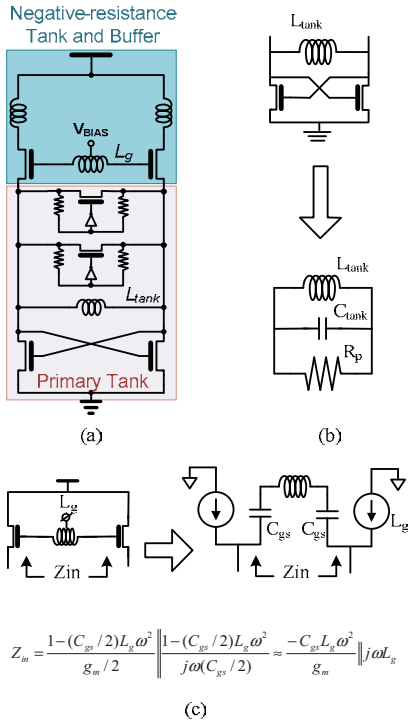



Fig. 2 (a) Oscillator schematic with stacking resonant tanks (b) regular tank equivalent circuit model (c) negative-resistance tank circuit model

### *B. D-Band Low Noise Amplifier (LNA)/Power Amplifier (PA)*

Although a 65nm NMOS device can achieve cut-off frequencies >200GHz, it still presents a considerable challenge to realize the intended D-band amplifier due to device/ substrate/line parasitic. Fig. 3 illustrates our designed LNA circuit, which is implemented differentially to ensure its immunity to supply/ground coupling noise. An on-chip balun converts the single-ended input into differential signals and

matches the LNA to 50ohm. Unlike its RF/microwave frequency counterparts which would easily lose 1~2 dB in gain/noise figure, this 140GHz balun only degrades the LNA gain/noise figure by 0.3~0.5dB in simulations. This is because the magnetic coupling through the balun becomes more effective at the mm-Wave frequencies, also exemplified by the much higher inductor Q that is easily >30 versus <15 at RF/microwave frequencies. As shown in Fig. 3 (a), a three-stage differential amplifier follows the balun to form the LNA core. Transformers are utilized between stages to attain optimal inter-stage matching for the maximum voltage gain. Also, two serial inductors connecting the amplification device and the cascode device in each amplifier stage evolve into a π-matching network along with their source/drain capacitance to achieve the desired wide band amplification. Two small source degenerative inductors are incorporated in the first stage LNA to accomplish wideband input matching. Simulations confirm the LNA achieving >16dB gain across135-147GHz with less than 10dB noise figure.

Fig. 3 (b) depicts the power amplifier schematic for Tx. It mimics the LNA in the architecture except the balun is now power matched for achieving saturation power gain of > 6dB. The ASK modulation is accomplished through the on/off switch between the power amplifier's differential inputs. The similar switches are also implemented across the VCO buffer load to ensure the fast modulation up to 10Gbps.

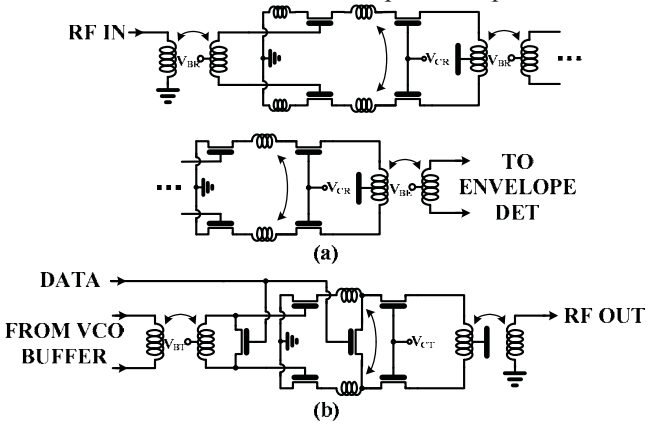



Fig. 3 Schematic of (a) 140GHz, 3 stage LNA (b) 140GHz PA

*C. Envelope Detector(ED)*

Envelope detector (ED) is often used in control and energy estimation systems to assess the signal strength at either the RF input or power amplifier output. It is designed to process low frequency envelop signal by using an op-amp based feedback loop. Prior ED design was also often based on the linear transconductor to deliver wide input dynamic range with low power consumption, it typically did not improve the operation frequency and operated below a few hundred MHz. Gyrator-C active inductor has been incorporated in the OTA to insert a zero into the transfer function and further boosts the envelope detector bandwidth up to GHz. However, it will not satisfy the proposed ultra-high speed data link needs to demodulate multi-giga-bit/sec incoming data at D-band carrier frequency.

Fig. 4 sketches the implemented high speed envelope detector circuit: two input NMOS extract the signal envelope from its D-band carrier. The two input NMOS are chosen with the feature channel length and biased as a class-B amplifier so that the incoming differential signals with carrier frequency can be rectified to reserve the modulated signal envelope. A differential amplifier is subsequently added to improve the circuit's PSRR, whose bias $V_{BO}$ comes from the signal envelope offset voltage, possibly obtained via a passive low-pass filter.

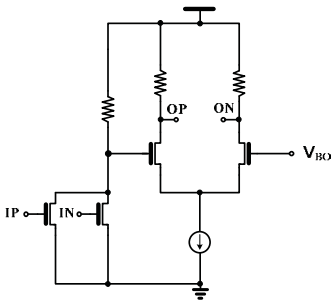



Fig. 4 Envelope Detector Schematic

*D. Wide Band Programmable Gain Amplifier (PGA)*

To further amplify the incoming signal and enhance the Rx dynamic range, a seven-stage PGA with 42dB gain range, 6dB gain step is implemented in the Rx chain, as shown in Fig. 5 (a). A DC offset cancellation loop is integrated on chip to remove the offset voltage in 1MHz cancellation corner and ensures the Rx's proper function. To achieve wideband amplification, Cherry-Hooper amplifier [5] is adopted in each stage, as shown in Fig. 5 (b). It utilizes the feedback instead of inductors at the output stage to sponsor high frequency peaking with relatively small area and power overhead.

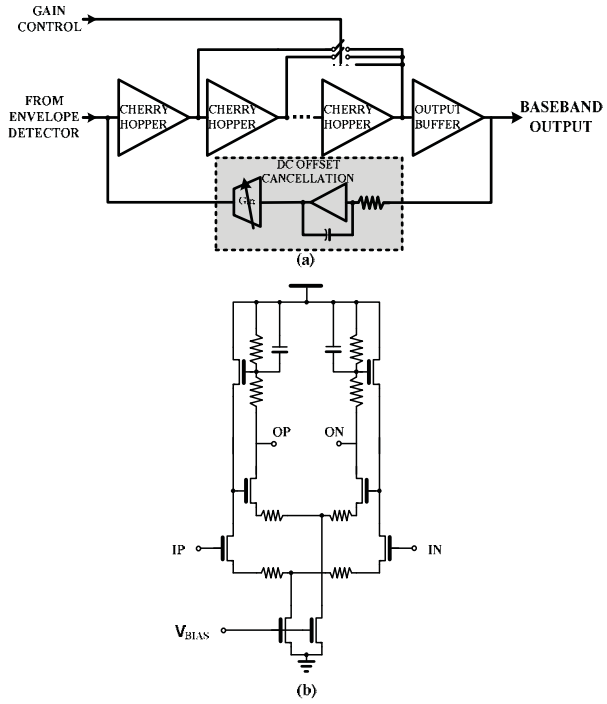
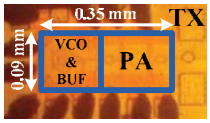



Fig. 5 Diagram of (a) PGA (b) Cherry-Hopper Amplifier Stage

## IV. Experimental Results

Fig. 6 shows the Tx/Rx die photos in 65nm CMOS, whose active areas are $0.03mm^2/0.12mm^2$, respectively. Fig. 7(a) demonstrates the transmitter CW tone at 140.326GHz as input data sets to one. The VCO can generate 131 ~ 140 GHz carrier frequencies through a 2-bit digital control. Due to our Lab test setup limitation, we currently characterize this D-band Tx based on existing V-band wave-guides and cables. Substantial loss in output power reading is therefore inevitable. Fig. 7(a) shows the un-calibrated spectrum when data=1; Fig. 7(b), on the other hand, shows the spectrum when modulated by 2Gbps $2^{\wedge 23}$-1 PRBS input data with energy spreading across the spectrum and buried under the setup noise floor. The Tx/Rx data linkage is verified by locating them in close proximity (~1cm) and coupling with bond wire. A 2-2.5Gbps $2^{23}$-1PRBS are successfully tested for data link, as shown in Fig. 8(a) and (b), respectively. The communication distance is currently limited by the low Tx output power and transmission efficiency, and the data rate is limited by $R_X$ baseband bandwidth of about 1.2GHz.



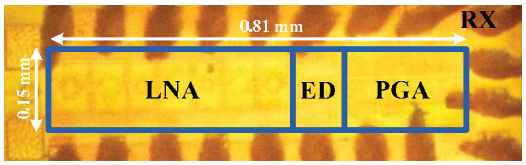
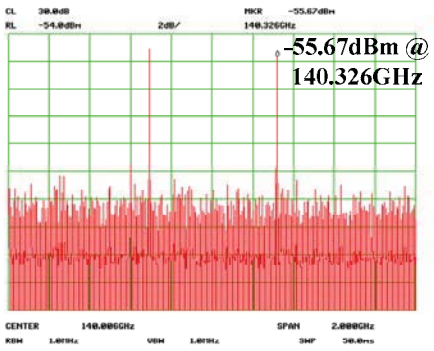
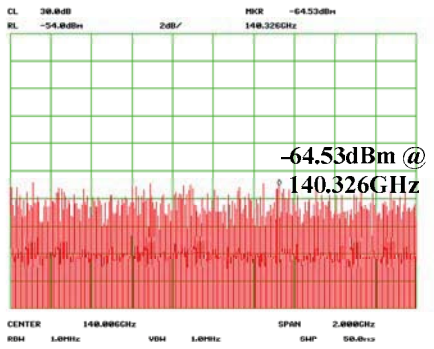




Fig. 6 Die Photo of D-band Tx and Rx

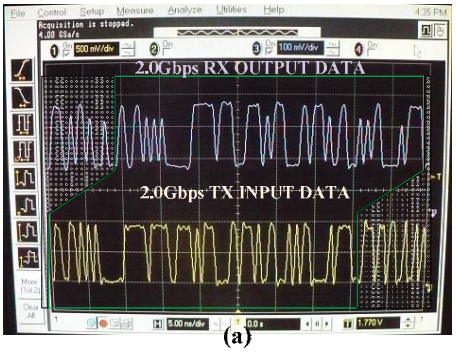



(a)

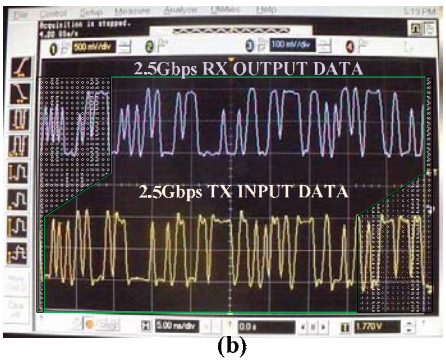



(b)

Fig. 7 Measured Tx spectrum at (a) data=1 (b) PRBS data




(a)




(b)

Fig. 8 Measured $R_X$ output versus $T_X$ input with (a) 2Gbps (b) 2.5Gbps $2^{\wedge 23}$-1PRBS

## V. Conclusion

In summary, we have demonstrated a 2.5Gbps data link at the carrier frequency of 140GHz between separately integrated Tx and Rx made of 65nm CMOS. The Tx/Rx only occupies $0.03mm^2/0.12mm^2$ die area and consumes 115mW/120mW, respectively. To the best of our knowledge, this is the first time that an integrated D-band data link has been realized in standard 65nm CMOS, which paves the way to implement future short-distance (<10cm) and ultra-high-speed data links for board-to-backplane, board-to-board and chip-to-chip communications under constraints of space, structure, or cost for computer, communication, and consumer electronics systems.

## Acknowledgment

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