An Integrated Frequency Synthesizer for 81-86GHz Satellite Communications in 65nm CMOS

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***Abstract* — We present an integrated frequency synthesizer in 65nm CMOS to enable the 81-86GHz satellite communication transceiver. The frequency synthesizer is inserted in a two-step zero-IF millimeter-wave transceiver with LO_{RF} at 70-78GHz and LO_{IF} at 1/8 of LO_{RF} to cover the desired entire frequency bands. It also features coarse phase rotation to endow beam forming capabilities for the intended communication system. The phase noise is < -83dBc/Hz at 1MHz offset as extrapolated from measured value at 1/8 of the VCO frequency (~9.4GHz). The measured reference spur is <-49dBc. Total synthesizer power consumption including LO buffers and phase rotators is 65mW at 1V power supply and the compact layout has rendered small synthesizer core area of 0.16mm^2.**

***Index Terms* — Frequency Synthesizer, injection locking divider, multi-modulus programmable divider, millimeter-wave transceiver, phase rotation, VCO .**

I. Introduction

The 81-86GHz frequency segment of W band (75–110 GHz) is allocated by the International Telecommunications Union (ITU) to satellite services to alleviate the crowded spectrum for microwave frequency satellite communications. Because of the abundant bandwidth to enable the wireless communication at a very high data rate, it is drawing increasing interest from the commercial satellite operators.

Traditional W band applications are based upon discrete components or exotic technologies, such as GaAs and InP HBTs, which are bulky and expensive. Fortunately, recent advances in deep-scaled CMOS technology make it feasible to realize ~100GHz millimeter-wave integrated circuits operating with >180GHz f_T devices [1], which has been recently exemplified by a fixed division ratio PLL in [2]. The unsurpassed CMOS integration capability allows the incorporation of various functions, such as RF modulation and demodulation, digital processing, encryption and decryption, etc., into a single chip, thus fulfilling the quest for low-cost, low-power and light weight communication systems for satellite services.

Within RF/millimeter-wave communication systems, the frequency synthesizer is one of the key building blocks, which is required to generate a low-phase noise and stable local oscillation (LO) signal for signal modulation and demodulation. Numerous research efforts [3-6] have been made in the past to design frequency synthesizers for millimeter-wave communications. Ref. [3] implemented a 15-18GHz synthesizer and a frequency tripler to avoid large division ratio and cumbersome high frequency LO routing to both receiver and transmitter in SiGe technology. Ref. [4] developed a 77-81GHz synthesizer in SiGe as well to support short-range pulsed-radar transceiver, with a fixed division ratio and relaxed quadrature LO matching requirements. Ref. [5] and [6] reported two stand-alone frequency synthesizers running at 40GHz in 130nm CMOS and 57-66GHz in 45nm CMOS, respectively, to support V-band applications.

In this paper, we present an integrated frequency synthesizer in 65nm CMOS with fully-programmable division ratios and phase rotators to accomplish 81-86GHz satellite communication that simultaneously boasts wide frequency range, low power consumption and small chip area. It employs a chain of complementary injection locking dividers to realize the demanded high-frequency prescaler, and an injection locking buffer with high drivability to facilitate a compact and high performance transceiver.

II. Transceiver Architecture and Frequency Plan

Direct conversion architecture can realize a compact RF transceiver with power efficient RF modulation/de-modulation in lower GHz RF operations. However, the higher the operation frequency, the more sensitive the circuits are to process variations in deep-scaled CMOS. For example, the vast LO quadrature mismatches, especially the phase mismatch due to component mismatches, asymmetrical capacitive/magnetic coupling effects can seriously impede direct conversion transceiver performance in millimeter-wave frequency bands. Polyphase filter may be exploited to alleviate the problem at the price of high power consumption but lead to low LO drivability that may dramatically deteriorate the transceiver linearity and noise figure performance. Additional digital baseband calibration may be applied but often with limited range and consuming extra power.

Instead of chasing challenging millimeter-wave frequency quadrature LO operation in the direct conversion, a two-step zero-IF architecture is adopted in

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this work to lower the quadrature operation to about 10GHz frequency range (i.e. LO_{IF}), which permits LO signals to be generated through a resistive load CML divider-by-2 circuit with small mismatches. This architecture not only enables more accurate quadrature LO signal generation, but also renders more compact realization without extra area-consuming inductors in deep-scaled CMOS. It is also easier to harness various LO phases more accurately to implement a more sophisticated beam-forming front end. Fig. 1 depicts the intended transceiver architecture for 81-86GHz satellite communications.

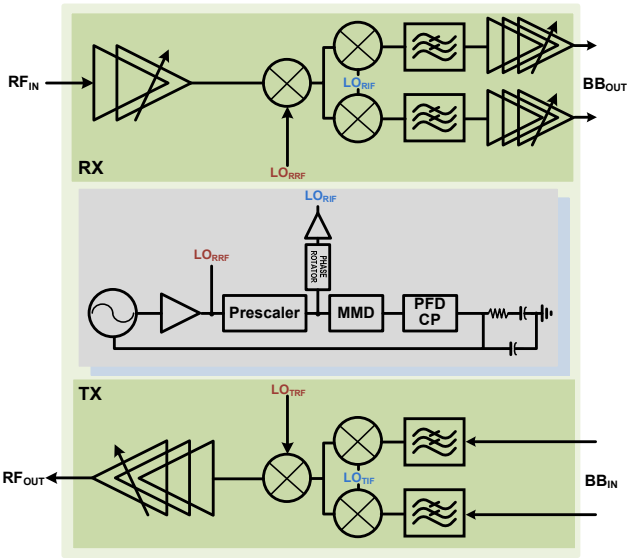

Fig. 1. Integrated synthesizer with phase rotators and T/R LO buffers to support 81-86GHz Transceiver for satellite communications.

A frequency synthesizer contains VCO at 70-78GHz as the LO_{RF} and 1/8 of its frequency as the LO_{IF} to cover the intended 81-86GHz frequency bands. The following phase rotator at LO_{IF} supports 0^0, 90^0, 180^0 and 270^0 coarse phase-tuning capability that facilitates baseband processing with various combinations of I+Q, I-Q, -I+Q and –I-Q. Integer-N frequency synthesizer architecture is chosen due to its superior phase noise performance and small form factor, which can sufficiently meet the channel requirement of required wide band applications. LO drivability to TRX up/down conversion mixers in millimeter-wave frequency is fairly challenging so we use two dedicated synthesizers for receiver and transmitter, respectively to alleviate this issue.

III. Circuit Implementation

The proposed type II, 3rd order frequency synthesizer consists of a reference buffer, a pseudo differential PFD with charge pump, a second order loop filter, a voltage controlled oscillator (VCO) with injection locked buffer, an asynchronous multi-modulus divider (MMD), an additional phase rotator and a LO_{IF} buffer, as shown in Fig. 1. We place the injection locking buffer, RF mixers and the prescaler in close proximity to minimize the routing load, which not only eliminates extra buffers but also alleviates undesirable inter-stage matching at the millimeter-wave frequency. Consequently, we can use a single buffer to drive both prescaler and RF mixers with smaller insertion area and an estimated 30% power-saving in comparison with that of using two separate buffers.

The phase rotator and LO_{IF} buffers are also located in close proximity with IF mixers to allow well-matched resistive load buffer with sufficient drive and good matching. To ensure low power operation and circuit reliability, a single 1V supply is used for the entire synthesizer. The supply is also separated from the receiver and transmitter supplies for better isolation. Fully and/or pseudo differential implementations are exploited in the entire synthesizer design to further attenuate invading spurs from both the supply and ground and the spur emission from the synthesizer itself.

A. VCO and Injection Locking Buffer Amplifier

The VCO, as shown in Fig. 2(a), adopts LC cross-coupled pair by using NMOS as the switching transistors due to its higher f_T. A resistive bias is used at the top instead of the PMOS current source to avoid the device flicker noise from coupling into the tank to degrade the phase noise through AM-to-PM conversion. Accumulation mode NMOS varactor is used to fine-tune the oscillation frequency while a three bit switch controlled MIM capacitors are used to achieve a wide tuning range to cover desired frequency bands from 70GHz to 78GHz. The same switch capacitors are used in subsequent injection locking buffers and dividers to line up VCO, injection locking buffer and divider operating frequencies. In millimeter-wave VCO design, the tank quality (Q) is often determined by that of switch capacitors and varactors rather than that of inductors, which typically have a high Q of >20. To attain a good quality factor in switch capacitor for both on/off states, a hybrid π-switch and moderate C_{max}/C_{min}(~2) are adopted for optimized phase noise performance.

According to our simulations, LO_{RF} buffer must support larger than $600mV_{p-p}$ signal output to drive both RF mixer and prescaler. An inductive loading cascode structure is used to reduce the capacitive load to the preceding VCO by mitigating the Miller effect. One positive feedback cross coupled pair is inserted in Fig. 2(b) as an injection locking buffer to further boost the signal strength. Post-

layout simulations show combined VCO and the injection locking buffer can achieve 70~81GHz tuning range with 1.4GHz/V K_{VCO} and larger than 650mV_{p-p} LO_{RF} outputs.

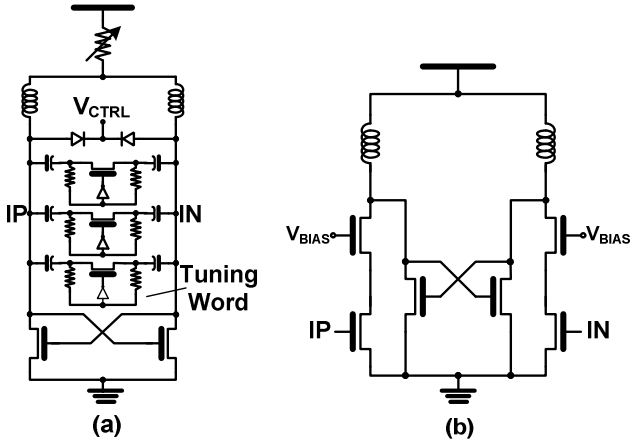

Fig. 2. Schematic of (a) VCO and (b) Injection Locking LO_{RF} Buffer Amplifier.

B. Prescaler Divider and Phase Rotator

One challenge in millimeter-wave frequency synthesizer is the high speed prescaler design, which mandates an extensive tuning effort due to lack of accurate models for passive/active components and interconnects. To obtain good performance with design success on the first try, several practices have been employed besides a robust divider design: 1) Careful floor-planning of the prescaler chain and optimization of connections between them; 2) Simulation of passive components and routing paths by using EM tools, such as ADS momentum, SONNET and HFFS; 3) Extraction of device parasitics and their inclusion in simulations and verifications. As a result, simulations have achieved a deviation of less than 5% in comparison with the actual measured results.

Fig. 3(a) sketches the complementary injection locking divider. Differential circuit realization not only achieves robust design without the imbalance problem typically in a single-ended counterpart, but also utilizes both polarities to increase the locking range by injecting signals into the tank via both NMOS and PMOS devices. The injection signal threshold and effectiveness can be adjusted through the device body voltage. Such injection locking structure is adopted in the first two stages of prescalers. Their currents are controlled by a two-bit DAC, and the locking range is further enlarged by another three-bit switch-controlled MIM capacitors.

Beam forming has proven to be an effective method of boosting the transmission output power and improving the receiver sensitivity. A coarse phase rotator is designed, as shown in Fig. 3(b), to support four different phase options followed by amplitude controlled resistive load LO_{IF} buffer. This phase rotator can further obtain finer phase step by adding phase interpolators.

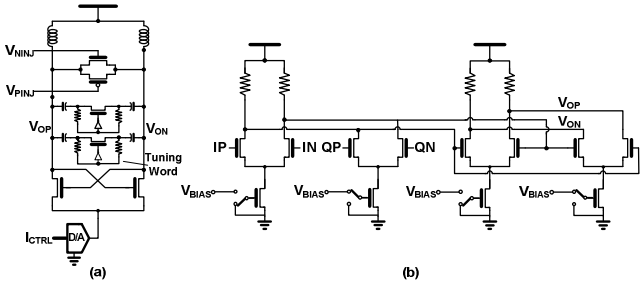

Fig. 3. Schematic of (a) prescaler divider and (b) phase rotator.

C. Programmable Divider Chain

A multi-modulus divider in fully differential structure is implemented to provide programmable division N_{div} from 128 to 248. The total division ratio of the loop equals $8\times N_{div}$. Fig. 4 manifests the asynchronous multi-modulus divider and depicts the detailed CML logic circuit. Compared with the synchronous implementation, it consumes less power and smaller real estate. However, it may introduce excessive noise due to noise accumulation through cascade stages. A re-synchronization circuit is thus used to counter the accumulated noise along the chain by realigning the signals.

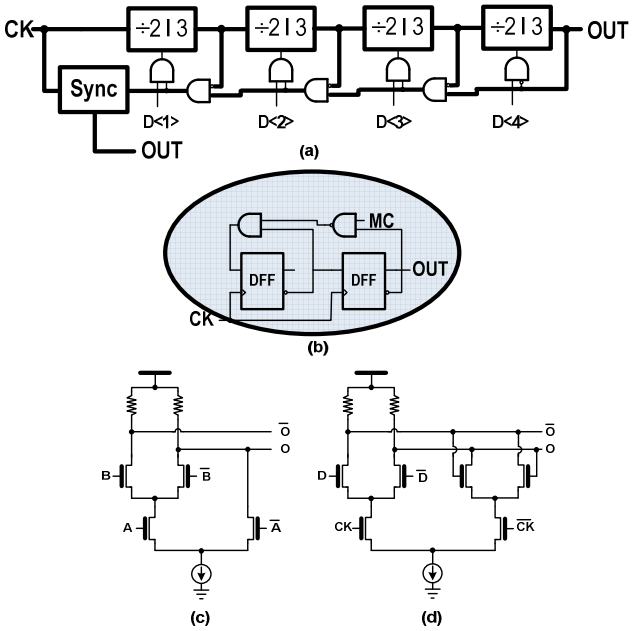

Fig. 4. (a) Multi-modulus programmable counter and its building block circuitry, including (b) ÷2/3 module, (c) "And2" logic and (d) latch

Afterwards, a pseudo-differential reference buffer, a PFD with the charge pump driven by programmable current from 50μA to 400μA, as well as a second order

on-chip loop filter, are employed to complete the frequency synthesizer with 300 KHz loop bandwidth.

IV. Experimental Results

Fig. 5 shows the die photo of an 81-86GHz transceiver. Within it, the integrated frequency synthesizer occupies a core area of 0.16mm^2 and burns 65mW power from a 1V supply. Fig. 6(a) demonstrates the 86GHz output from the transmitter and Fig. 6(b) demonstrates a baseband output tone from the receiver. Both of them confirm the proper function of the integrated frequency synthesizer. Fig. 6(c) draws the transmitter output frequency curve versus various control bits, which covers the desired communication frequency bands with safety margins (79GHz~88GHz). Additionally, Fig. 6(d) reveals the synthesizer phase noise measured at 1/8 of VCO frequency f_{VCO} (i.e. 9.4GHz, equals to 1/9 of TX output frequency f_{OUT}) from a separate test chip, which can be extrapolated into -83dBc/Hz @1MHz in 75GHz.

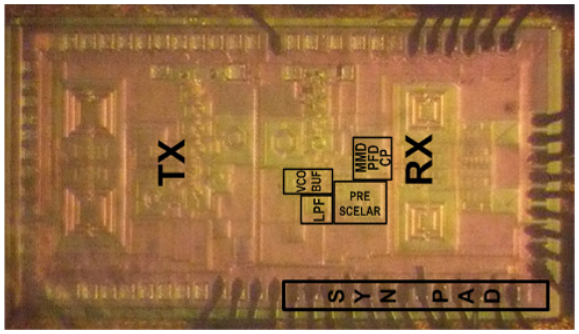

Fig. 5. Die photo of the transceiver and frequency synthesizer.

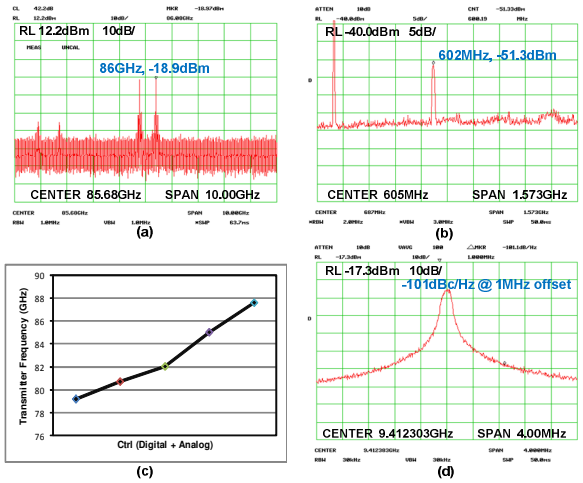

Fig. 6. Measured (a) signal spectrum at 86GHz from transmitter and (b) baseband output signal from receiver when injecting a 85GHz CW tone; (c) frequency tuning curve at TX output and (d) the phase noise performance @ $f_{VCO}/8$ (9.4GHz)

V. Conclusion

An integrated frequency synthesizer which enables the transceiver operation at 81-86GHz for satellite communication is realized in 65nm general purpose (GP) CMOS. Table I summarizes measured performance versus those of prior developments in similar frequency range [2, 5 and 6] based on deep-scaled CMOS technologies. This frequency synthesizer clearly demonstrates its performance advantages in wider frequency range, better phase noise, and more compact design to facilitate the transceiver SoC for intended satellite communication. Its slightly higher power consumption than that of Ref. [2] is primarily due to its much wider frequency coverage and extra integration of phase rotators and T/R LO buffers.

	[2]	[5]	[6]	This Work
Type	Fundamental, Independent	Fundamental, Independent	Fundamental, Independent	Offset, Integrated
Center Freq. (GHz)	95.1~96.5	40	57~66	70-78
Divisions	256	256/258/260/262	512~8184	1024~1984
Phase Noise (dBc/Hz)	-75.9dBc/Hz @1MHz	-75.3dBc/Hz @1MHz	-75dBc/Hz @1MHz	-83dBc/Hz @1MHz
Reference Spurs (dBc)	-51.8	-46	-42	-49
Supply (V)	1.2	1.5	1.1	1.0
Power (mW)	43.7	105	76	65
Area (mm^2)	0.7 (WiPad)	0.56 (core), 1.69(WiPad)	0.82 (WiPad)	0.16 (core), 0.31 (WiPad)
Technology	65nm CMOS	0.13um CMOS	45nm CMOS	65nm CMOS

Table I. Performance Summary and Comparison

Acknowledgement

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