A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c TRX

David Murphy*, Qun Jane Gu*, Yi-Cheng Wu*, Heng-Yu Jian*, Zhiwei Xu*, Adrian Tang*, Frank Wang*,
Yu-Ling Lin†, Ho-Hsiang Chen†, Chewnpu Jou†, Mau-Chung Frank Chang*
*EE Department, University of California, Los Angeles, USA; Email: dmurphy@ee.ucla.edu
†Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, R.O.C.

***Abstract*— A low phase noise, wideband, mm-wave, integer-N PLL that is capable of supporting a 802.15.3c heterodyne TRX is reported. The PLL can generate 6 equally spaced tones from 43.2GHz to 51.84GHz, which is suitable for a heterodyne architecture with LO=(4/5)RF. Phase noise is measured directly at the LO frequency and is better than -97.5dBc/Hz@1MHz across the entire band. The total power consumption is 72mW from a 1V supply. The reported frequency synthesizer is smaller, exhibits less phase noise, and consumes less power than prior art. In addition, the LO tone corresponds to the fundamental of the VCO as opposed to a higher harmonic.**

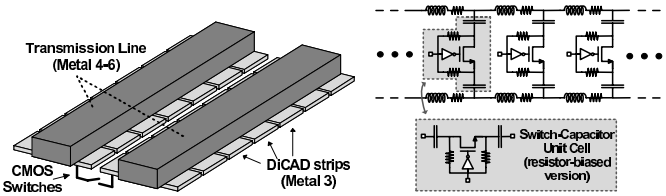
Central to the PLL performance is the design of a low-noise, mm-wave VCO with a 22.9% tuning range. It is noted that resonator nonlinearities may result in significant up-conversion of flicker noise in wideband, mm-wave VCOs. To overcome this, Digitally-Controlled-Artificial-Dielectric (DiCAD) is used to linearize the resonator.

I. Introduction

The past few years have seen a dramatic rise in the number of mm-wave publications targeting the unlicensed 57-66GHz spectrum. Both the IEEE 802.15.3c and wirelessHD standards define 4 bands centered at 58.32GHz, 60.48GHz, 62.64GHz and 64.8GHz. To achieve full compliance with these standards, an extremely wideband, mm-wave PLL is needed. Achieving good phase noise performance in such a wideband synthesizer is challenging, but will be necessary for systems employing complex modulation schemes. Within this context, we present a low noise, integer-N PLL that is capable of supporting a heterodyne 802.15.3c (or wirelessHD) TRX with LO=4×RF/5=4×IF. Unlike the current art [1], which uses a quadrature-VCO and a push-push technique to isolate the 2nd harmonic, this work achieves a wide tuning range and low phase noise using a VCO to directly generate the LO frequency.

Central to this endeavor is the design of a wideband, mm-wave VCO. While recent works have applied RF circuit techniques to mm-wave frequencies with some success, the design paradigm does in fact change. Most notably, resonator loss is typically determined by the quality of the varactor rather than the inductor. Moreover, while flicker noise can dominate in any wideband CMOS VCO, the situation is even more deleterious in mm-wave oscillators, since it is difficult to realize a high impedance node at twice the oscillation frequency across the entire tuning range [2]. The problem is further exacerbated by the large KVCO values that are typical of mm-wave VCOs [3]. Another practical concern is routing parasitics, which can result in large discrepancies between simulation and measurement in mm-wave design. To address these problems, this work embeds Digitally-Controlled-Artificial-Dielectric (DiCAD) [3] in a cross-coupled LC oscillator (Fig. 1). DiCAD originated as a method to control the permittivity of a differential transmission line using CMOS switches. When used in resonators, it is a useful technique that enables fine and linear digital frequency tuning and a corresponding reduction in KVCO and AM-to-PM conversion.

Section II introduces the PLL topology. Section III documents key mm-wave design choices, while measurement results are provided in Sec. IV. Conclusions are drawn in Sec. V.



(a) Physical Realization (b) Circuit Equivalent Model

Fig. 1. Embedded Digitally-Controlled-Artificial-Dielectric (DiCAD) in standard CMOS technology.

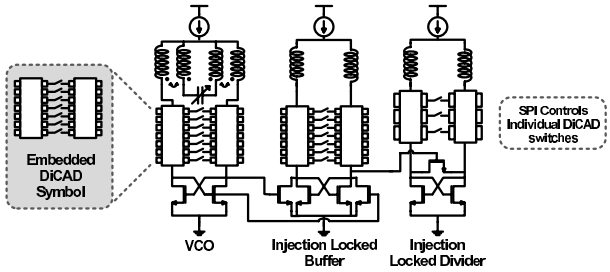


Fig. 2. DiCAD is embedded in all mm-wave blocks (VCO, injection-locked buffer, and injection-locked divider.)

II. PLL Topology

The proposed programmable integer-N, Type-II, 3rd order PLL is shown in Fig. 3. The mm-wave blocks consist of a DiCAD-based VCO, injection-locked buffer and injection-locked frequency divider (shown separately Fig. 2). The rest of the divider chain consists of CML-based logic; a prescaler divides the 24GHz divider output by 16 while also generating IQ phases at 12GHz, and a multi-modulus divider further

divides the signal by 16+N (where N is a 4-bit binary code.) Using this scheme, any divide ratio from 512 to 992 in steps of 32 can be obtained. This divide ratio together with a 54MHz reference enables synthesis of the required tones. A PFD, current-steering charge pump and 2nd order on-chip loop filter complete the block. To increase flexibility during testing, the on-chip loop filter can be disable, and an off-chip loop filter can be employed.

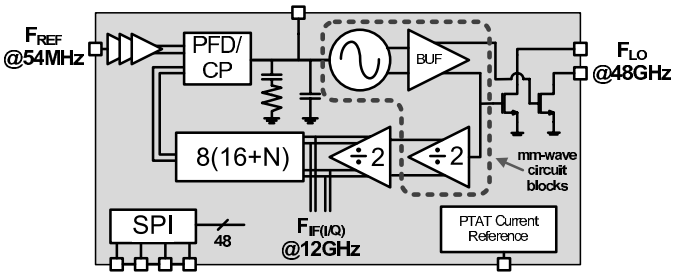


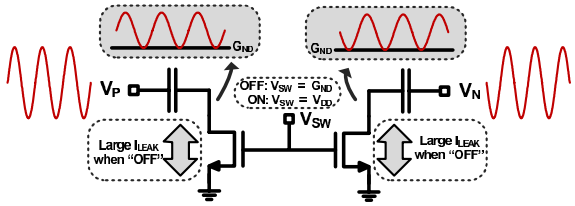
Fig. 3. Fabricated mm-wave PLL with frequency plan.

III. Key mm-Wave Design Choices

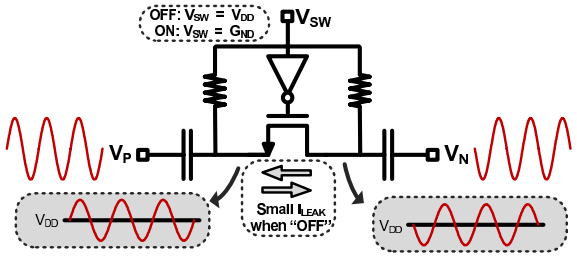
The circuit blocks operating at RF frequencies (i.e. CP, PFD and CML dividers) have been well studied and the associated trade-offs are understood. What is less clear is the performance limitations of the mm-wave blocks. Moreover, it is the performance of these blocks that translate directly into typical integer-N PLL performance metrics such as tuning range, power consumption, and out-of-band phase noise. As outlined, the design of wideband, mm-wave VCOs do differ from their RF counterparts; specifically, the Q of varactors degrade significantly and flicker noise becomes increasingly problematic. Minimizing these effects was a key focus of the design. The design highlights are as follows:

1) DiCAD Resonator: To enable fine digital tuning, DiCAD is embedded in all mm-wave blocks (Fig. 2). This linearizes the resonate tanks and limits flicker noise up-conversion in the VCO [3]. In [3], DiCAD was presented as a permittivity-programmable transmission line and was used to control a digital oscillator, but the structure can equally be viewed as a distributed switched capacitor bank (see Fig. 1(b)). From a mm-wave perspective, DiCAD's value lies in its periodic structure which is easily modeled and is suitable for fast and accurate EM simulation. Indeed, since the structure can be imported into an EM simulator along with the inductor, parasitics arising from routing are greatly reduced. This enables fine digital tuning and first-time "right" design.

2) Switch-Selection: Since, schematically at least, DiCAD resembles a distributed switched capacitor bank consisting of identical switched-capacitor unit cells (see Fig. 1(b)), we can analyze it as such. Two common switch-capacitor unit cells are shown in Fig. 4. Because of its simplicity, the self-biased switch is most widely used. The resistor-biased version, however, exhibits an enhanced Q and, thus, exhibits a better trade-off between tuning range and phase noise [4]. In addition, we have also observed a reduction in phase noise degradation due to drain-to-source leakage currents. Consider the self-biased switch in Fig. 4(a). When the switch is in the "OFF" state, the oscillation waveform at the drain node is such that at the trough of an oscillation, the drain voltage briefly drops below the source. This causes the device to pull current from the ground. Under steady-state conditions, the amount of charge pulled from ground must equal the charge lost due to device leakage current. Noise associated with these currents can degrade the overall phase noise performance of the VCO. By contrast, the resistor-biased switch (Fig. 4(b)) does not suffer from this effect; when "OFF", both V_{GS} and V_{GD} of the transistor are biased around a large negative potential ($-V_{DD}$) and, so, the amount of leakage current is greatly reduced. Fig. 5 shows simulation results for our finalized VCO, with both the self-biased and resistor-biased switches. As expected, when the switches are on, the performance is the same. However, when all 32 switches are off, the resistor-biased switch achieves an 7.5dB improvement in phase noise. Using SpectreRF, it was deduced that this degradation was due to noise current flowing in the off switches. This mechanism is likely to be apparent only in deep-scaled GP CMOS technologies.



(a) Self-biased switched capacitor: when "OFF", V_{GS}=0 and large leakage current flows



(b) Resistor-biased switched capacitor: when "OFF", V_{GS}=-1 and V_{GD}=-1 and, so, leakage current is reduced

Fig. 4. Two common switch capacitor unit cells that can be employed in DiCAD. The capacitor is realized by the DiCAD metal strip in Fig. 1(a).

3) Frequency Control: Because DiCAD is a distributed structure, the unit capacitor-cells, although identical, do not have have the same effect on the oscillation frequency. To ensure monotonicity, a thermometer code is used to digitally control the DiCAD. This allows minimization of varactor size (and KVCO). In order to save area, the varactor is magnetically coupled to the inductor.

4) Current Control: The current source contributes a large portion of the flicker noise in any oscillator and, in mm-wave designs, it does not prevent flicker and thermal noise from the differential pair from up-converting to the output. Therefore,

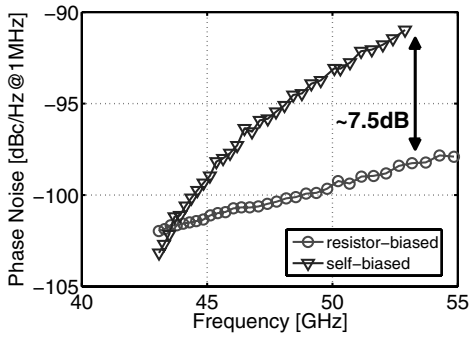


Fig. 5. Simulated phase noise performance of DiCAD-VCO with self-biased switch and resistor-biased switch. When "OFF", leakage current in the self-biased switch results in an 7.5dB degradation in performance.

it is replaced with a bank of switchable resistors that can limit the amount of current flowing in the oscillator core.

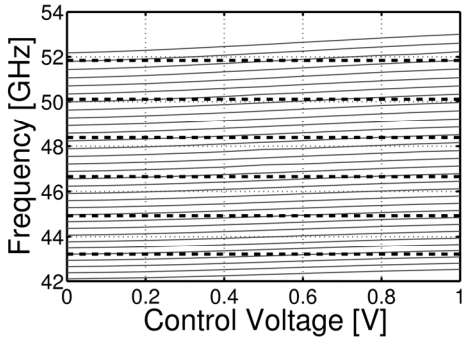
5) DiCAD-Based Injection-Locked Buffer and Divider: Since the PLL is intended for use in a TRX, it is required to drive a large capacitive load with maximum possible swing (mixer conversion gain is proportional LO swing.) To this end, an injection-locked oscillator is employed as the buffer (Fig. 2). This low power option provides the large output swing required and prevents corruption of the LO signal by the mixer stages. The injection-locked buffer has a very similar design/layout to that of the oscillator itself; this ensures frequency alignment and limits phase noise degradation due to kickback. The first divide-by-2 stage is also an injection-locked topology (Fig. 2). Although the divider could be realized by an aggressive CML design, the injection-logic topology is low power. Like the buffer, precise frequency alignment is required; in this case, the free-running frequency of the divider needs to be half that of the VCO/buffer.

IV. Measurement Results

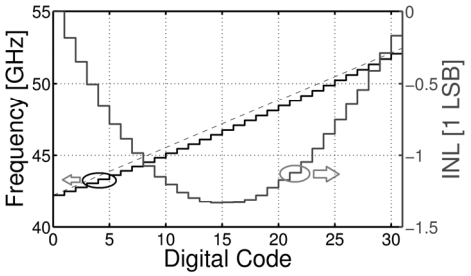
The PLL was fabricated in a 65nm GP process. The 48GHz injection-locked buffer drives two open drain buffers, which in turn drive the test equipment (Fig. 3). An on-chip SPI controls 48 bit-lines that are used for digital control current and digital frequency tuning. A PTAT current reference is used to provide accurate bias currents. The control voltage is connected directly to a pad so that VCO tuning curves can be measured and the loop bandwidth can be modified during testing. The reference is provided by an ultra-low noise Crystek XO.

The measured VCO tuning curves are shown in Fig. 6(a). Continuous tuning from 42.1GHz-to-53GHz is achieved with a KVCO of less than 1GHz/V. The distributed nature of DiCAD results in very fine, monotonic digital tuning that is extremely linear, as shown in the digital INL plot in Fig. 6(b).

Under closed-loop operation, the PLL is capable of generating 6 equally spaced tones: 43.2GHz, 44.928GHz, 46.656GHz, 48.384GHz, 50.112GHz and 51.84GHz. The latter 4 tones are precisely 4/5 of the channel frequencies defined in the 802.15.3c standard and, so, are suitable for a heterodyne 802.15.3c TRX with LO=(4/5)RF. The out-of-band noise is



(a) Measured VCO tuning curves; heavy dotted lines correspond to frequencies that can be synthesized with 54MHz reference.



(b) Digital tuning and digital INL: the distributed nature of DiCAD results in extremely linear digital tuning.

Fig. 6. Frequency range of VCO.

measured using a large off-chip loop filter that reduces the PLL loop bandwidth to less than 100kHz. Phase noise measurements are listed in Table I, and typical outputs from the spectrum analyzer are shown in Fig. 7. Note that the noise performance is maintained across the entire band. This is important, as a wideband PLL may experience a flicker-noise null at a single point [5]. Since the out-of-band noise is basically the noise contribution of the VCO itself, Table II compares the DiCAD-VCO with recently reported deep-scaled, wideband, mm-wave VCOs. When performance across the entire band is considered, the DiCAD-VCO achieves the best performance in terms of tuning range and FOM_T.

TABLE I
Phase Noise and Figure of Merit Measurements @1MHz Offset

Freq [GHz]	$\mathcal{L}\{\Delta\omega\}$ [dBc/Hz]	FOM† [dBc/Hz]	FOM_T‡ [dBc/Hz]
43.2	-99.17	-179.84	-187.04
44.928	-99	-180.01	-187.21
46.656	-98.33	-179.67	-186.87
48.384	-99.17	-180.82	-188.02
50.112	-97.5	-179.46	-186.66
50.84	-97.67	-179.92	-187.12

†$\text{FOM} = \mathcal{L}\{\Delta\omega\} + 20\log_{10}(\omega_0/\omega_m) - 10\log_{10}(\text{P}_{\text{DC[mW]}})$
‡$\text{FOM}_\text{T} = \text{FOM} + 20\log_{10}(TR/10)$

When the on-chip loop filter is enabled, the loop bandwidth sits around 1MHz and the inband noise is measured at -81dBc/Hz (see Fig. 8). This number is better than other standard integer-N topologies that employ similar divide ratios [8] [9], and can be reduced further by increasing the charge pump current (only 400μA is currently dissipated).

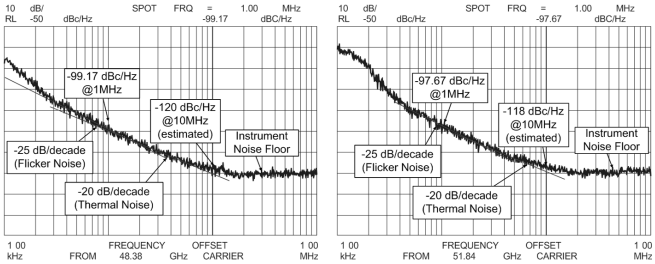


Fig. 7. Phase noise measurements with large off-chip loop filter.

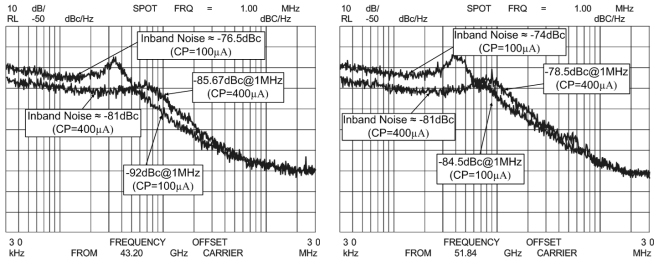


Fig. 8. Phase noise measurements with on-chip loop filter enabled.

TABLE II

COMPARISON WITH OTHER 65NM/90NM WIDEBAND MM-WAVE VCOS

Ref.	This Work	[6]	[7]
Tech.	65nm CMOS	90nm CMOS	65nm CMOS
Freq	47.55GHz	58.4GHz	56GHz
Supply	1V	0.7V	1.2V
$\mathcal{L}\{\Delta\omega\}$ @1MHz	$\leq$-97.5dBc/Hz‡	-91dBc/Hz	$\leq$-89.84dBc/Hz‡
Power	16mW	8.1mW	15mW
Core Area	220μm×125μm	96μm×80μm	350μm×152μm
VCO TR	22.9%	9.32%	17%
FOM_T	-186.66dBc/Hz‡	-176.6dBc/Hz	-178dBc/Hz‡

‡ Worst-case measurement across entire band.

Finally, Table III compares our PLL design with the current state-of-art [1]. Our work improves normalized phase noise, covers an additional 60GHz band, consumes less power and 64% less area, and operates at a higher frequency. More importantly, the VCO also directly generates the LO frequency. This is in contrast to [1], which isolates the 2nd harmonic of a push-push QVCO operating at LO/2. Therefore, we avoid the problem of limited 2nd harmonic drive strength and all issues associated with QVCOs (unpredictable mode behavior, increased I/Q mismatch, increased area). The die micrograph of the testchip is shown in Fig. 9(a). The PLL is intended for use in a dual-synthesizer TRX and, so, a micrograph of that chip is shown in Fig. 9(b).

V. CONCLUSION

A low-noise, wideband PLL that can support a complete IEEE 802.15.3c TRX is reported. The circuit is simple and robust, and the LO tone is generated by the fundamental of the VCO rather than by some harmonic. Further, by embedding DiCAD in all mm-wave blocks, the synthesizer achieves state-of-art performance (i.e. phase noise, area, frequency coverage, power) that is maintained across the entire band.

ACKNOWLEDGEMENTS

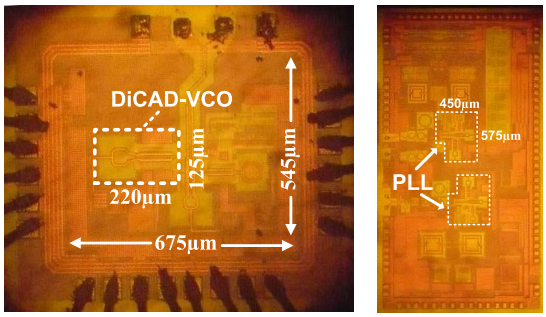
This work is supported in part by the DARPA/SPAWAR HEALICS program and by Intel Corporation.

TABLE III

COMPARISON OF PLL WITH RECENT STATE OF THE ART

Ref.	This Work	ISSCC 2010 [1]
Tech.	65nm CMOS	65nm CMOS
Architecture	Integer-N (VCO@50.112GHz)	Integer-N (VCO@20.88GHz)
Supply	1V	1.2V§
$\mathcal{L}\{\Delta\omega\}$@1MHz (Band 3)	-95.56dBc/Hz†	-90.46dBc/Hz‡ -93.98dBc/Hz♯
F_{ref}	54MHz	36MHz
Power	72mW	80mW
IEEE 802.15.3c Band Coverage	All 4 Bands	3 Bands
Core Area	0.68mm×0.55mm	1.1mm×1mm
VCO TR	22.9%	17.9%
$\mathcal{L}_{inband}\{\Delta\omega\}$	-81dBc/Hz	N/A

§ 1.8V used for CP/PFD
† Normalized to 62.64GHz from 50.112Hz measurement
‡ Normalized to 62.64GHz from 20.88Hz measurement
♯ Normalized to 62.64GHz from 41.96Hz measurement



(a) PLL test chip (b) 60GHz TRX

Fig. 9. Die micrographs

REFERENCES

[1] O. Richard *et al.*, "A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for wireless HD applications," *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, pp. 252–253, Feb. 2010.

[2] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[3] T. LaRocca, J. Liu, F. Wang, D. Murphy, and F. Chang, "CMOS digital controlled oscillator with embedded DiCAD resonator for 58-64GHz linear frequency tuning and low phase noise," *Proc. IEEE Microwave Symps. (MTT-S)*, pp. 685–688, Jun. 2009.

[4] H. Sjoland, "Improved switched tuning of differential CMOS VCOs," *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Processing*, vol. 49, no. 5, pp. 352–355, May 2002.

[5] E. Hegazi and A. A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, Jun. 2003.

[6] L. Li, P. Reynaert, and M. Steyaert, "Design and analysis of a 90 nm mm-wave oscillator using inductive-division LC tank," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1950–1958, Jul. 2009.

[7] J. Jimenez, F. Badets, B. Martineau, and D. Belot, "A 56GHz LC-tank VCO with 17% tuning range in 65nm bulk CMOS for wireless HDMI applications," *Proc. IEEE Radio Frequency Integrated Circuits Symps. (RFIC)*, pp. 481–484, Jun. 2009.

[8] C. Marcu *et al.*, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3434–3447, Dec. 2009.

[9] H. Hoshino, R. Tachibana, T. Mitomo, N. Ono, Y. Yoshihara, and R. Fujimoto, "A 60-GHz phase-locked loop with inductor-less prescaler in 90-nm CMOS," in *Proc. European Solid State Circuits Conf. (ESSCIRC)*, Sep. 2007, pp. 472–475.