A Compact, Fully Differential D-band CMOS Amplifier in 65nm CMOS

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***Abstract*—A fully differential 144GHz CMOS amplifier has been demonstrated in 65nm CMOS. It validates a maximum 20dB power gain and has positive gain over 38GHz frequency range from 126GHz to 164GHz. With stacking circuit architecture, the amplifier can tolerate up to 2V supply without reliability concern. It also delivers over 5.7dBm saturated output power with P1dB of 5dBm under a 2V supply. The amplifier features a 3-stage common-source cascode architecture with on-chip inter-stage matching. The chip occupies 0.05 mm^2 area and draws 39mA and 51mA from 1.4V and 2V supplies respectively. To our best knowledge, this amplifier achieves the highest power gain for CMOS amplifier beyond 100GHz and paves the way for D-band radar and passive imaging system applications.**

I. Introduction

CMOS technology has been widely used for various RF applications, such as cellular phone, WLAN, and Bluetooth, due to its super integration scale and powerful on-chip digital signal processing capability. It has become a dominant driver in monolithic integration circuits and systems today in addition to its already overwhelming presence in computing and microcontroller applications. CMOS technology continues to push the frontier to integrate more and more sophisticated functions into a single die for miniature systems under space, weight and power (SWaP) constrained environments.

Recent CMOS technology advancements are enabling the integration of high frequency applications like HDMI, WLAN and WPAN communications in 60GHz band or beyond. Several V band CMOS transceivers have been successfully demonstrated [1][2] and proved the CMOS millimeter wave (mm-Wave) feasibility. With digital assisted design methodology and on-chip self-healing algorithm, CMOS technology could deliver high performance mm-Wave system as good as the more expensive III-V counterpart.

Mm-Wave amplifier is one of the most critical and challenging blocks inside the transceiver, which serves as low noise amplifier of receiver to pick up the small input signal and power amplifier of transmitter to produce large enough output power. Disregarding constrains of slow transistors and losses of the integrated passive components in CMOS, a 150GHz amplifier with 8dB gain and 27GHz bandwidth has been demonstrated in 65nm CMOS by using dummy prefilled micro-strip lines [3]. It uses simple matching topologies together with optimized transistor to push the operation frequency limit. Reference [4] reports a six stage 140GHz amplifiers in 65nm CMOS, which achieves maximum 9dB gain with 1.2V supply. All reported amplifiers beyond 100GHz [3],[4],[5] nonetheless had low gain (<10dB) and utilizes single ended architecture, which would hinder their application in communication and imaging systems that request a sufficiently high gain to boost the receiver sensitivity, and prevent themselves from integration into a single chip system owing to its susceptibility to supply/ground spurious and substrate coupling.

To meet the system gain requirement and be immune from common mode noise, we developed a fully differential CMOS amplifier around 144GHz. Besides amplifier design, we will also discuss device size/layout optimization and inter-stage matching with measurement results.

II. Amplifier Design

A. Mm-Wave CMOS Device

Although 65nm CMOS could offer higher than 200GHz/230GHz f_T and f_{MAX}, the Silicon Foundry does not support the corresponding device model. It is because the actual device performance is highly layout dependent. In particular, the extrinsic parasitics, such as gate/source/drain resistance, substrate resistance and coupling capacitors among them, ultimately determine the maximum achievable gain. The MOS f_T and f_{MAX} can be simply summarized as:

$$f_T = \frac{g_m}{2\pi C_{gt}}, f_{\max} = \sqrt{\frac{f_T}{8\pi R_g C_{gd}}} \quad (1)$$

where C_{gt} is the total capacitance of gate, R_g is gate resistance and C_{gd} is the gate-drain capacitance. To reduce the gate resistance, a multi-finger structure has been adopted for wide gate width, thus providing a high trans-conductance (g_m). It not only boosts the f_{max}, but also significantly improves noise figure. However, the gate to substrate capacitance increases as the finger number increases given a fixed device width, which in turn degrades f_T. Double gate connection is used to further reduce the series gate resistance. However, it inevitably increases the gate capacitance due to induced coupling, which becomes more severe when the operation frequency is higher than 100GHz. To trade off the performance, 0.6μm finger width has been chosen in this amplifier with single end gate connection; it not only provides relatively small gate serial resistance and capacitance, but also allows area efficient connection that offers low resistance source/drain tie.

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The device metal connections also significantly affect the device performance. The wiring style of RF device supported by the Foundry might not be best optimized due to its large gate connection resistance and excessive coupling capacitance between gate and drain that contributes to parasitic Miller capacitors, as shown in Fig. 1(a). Given wide signal wiring inside mm-wave amplifier, a new device access using single gate connection illustrated by Fig. 1(b) might render better performance by offering smaller gate resistance through paralleling and minimized gate drain capacitance.

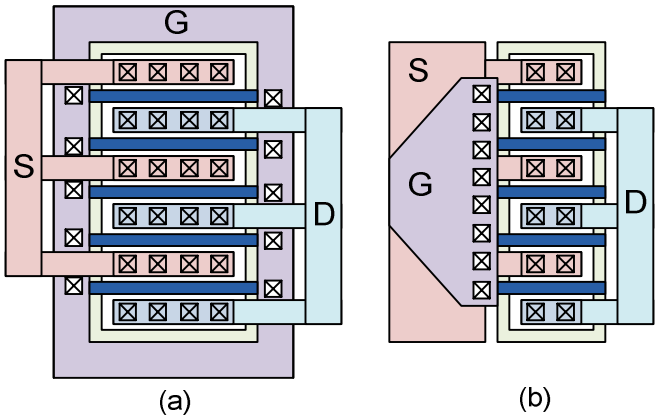

Figure 1. MOS device connection (a) RF device provided by Foundry, (b) device layout design in this amplifier

The existing BSIM3V4 model dedicated to lower frequency (<30GHz) operation supported by foundry cannot be directly applied to mm-Wave amplifier design. An improved model equipped with extrinsic parasitics like serial resistors, coupling capacitors, substrate capacitors and access line effects is used to facilitate the design as shown in Fig. 2(a). R_G, R_D, and R_S stand for the serial resistors to gate, source and drain introduced by the connection; C_{GS}, C_{GD}, C_{DS} are coupling capacitors and the transmission lines embody the access line effects which incorporate both resistive/capacitive and magnetic effects. Practically, it is hard to model these parasitics into lump fashion, so the powerful EDA tools are necessary to assist the procedure. A core device is extracted through Caliber RCX to form a model core consisting of transistor, poly connection resistors and coupling capacitors; then the metal wirings are simulated with EM tools to cover the access line effects. The ultimate mm-wave device model is formed by these two parts, as depicted in Fig. 2(b).

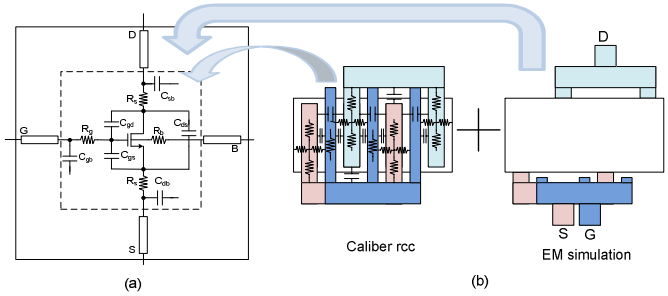

Figure 2. (a) Mm-wave MOS device model, (b) Caliber RCX extracts rcc model of the device core and access lines are simulated by EM tools

B. *Transformer and Maganetic Couppling*

Inter-stage matching is critical to amplifier performance. Microstrip line and coplanar line matching networks are widely used due to their less sensitive parameters. Although they are frequently used at mm-Wave frequency range, they tend to occupy larger chip area with a ~250µm quarter wavelength at this frequency compared with the lumped element approaches. Lumped element impedance matching using inductors delivers most compact implementation, which has been validated in 60GHz and 77GHz transceiver design. But with the increased frequency, the long inter-connections between stages, mandated by the inductor size, becomes significant. It has to be incorporated into design and requests careful modeling. Moreover this connection forms a serial stub that might transfer the load into unwanted impedance which could not be matched by practical on-chip inductors.

DC blocking is another serious issue related to inter-stage matching networks to allow individual gate and drain biasing. Non-cascode structure amplifier may live with same gate and drain bias situation. However, it limits the amplifier supply voltage, sacrifices linearity performance and requires a complicated supply network that would deteriorate amplifier power efficiency. Cascode amplifier architecture is used to decrease inter-stage Miller capacitance and boost stability, which is hostile to the identical bias voltage for both drain and gate, then necessitates DC blocking. However, DC blocking capacitor between stages inevitably decreases the amplifier maximum achievable gain and complicates the physical design.

Transformer has been used in radio frequency circuits in early days of telegraphy to couple the power from one winding to the other without significant loss. Because the transformer blocks the direct current flow, it provides the flexibility to the windings biased at different potentials. Fig. 3 depicts on-chip transformer design and its associated model. It has several prominent characteristics: first, innate DC blocking function; second, flexible voltage/current gain by adjusting the winding turn ratio; third, natural inter-stage T matching network; fourth physically spanned input and output signals that forms necessary space for isolation, which eliminates extra undesired wiring and support symmetrical/compact physical design.

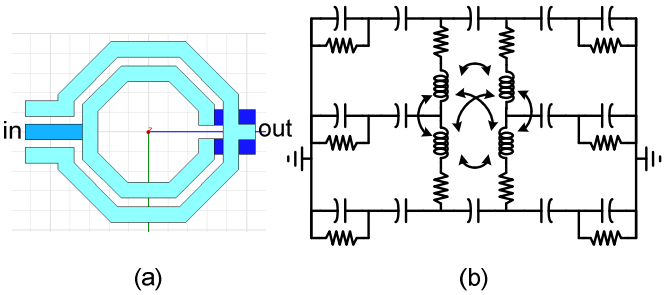

Figure 3. Monolithic Transformer (a) layout and (b) model

With higher operation frequency, the magnetic component quality improves as does the coupling strength between the transformer windings. For example, a well designed inductor only has quality factor Q up to15 at lower GHz frequencies, but the Q could be over 30 at above 120GHz frequency range.

It indicates the effectiveness of magnetic coupling in mm-Wave frequencies. In this amplifier design, monolithic transformers have been used as inter-stage matching network extensively to achieve a compact and efficient realization. However, an accurate model is mandatory to ensure the design accuracy for high performance.

C. *144GHz Amplifier*

The receiver low noise amplifier serves as the first amplification stage that is susceptible to noises. System-on-a-chip (SoC) requires high supply rejection ratio and common mode rejection to mitigate the coupling from supply and substrate for high signal Signal-to-Noise Ratio (SNR). In transmitter side, the pre-amplifier also needs to obtain low spurious generation that could contaminate other circuit blocks in one common integrated substrate. To ensure these, a fully differential architecture is preferred. Fig. 4 sketches the schematic of the proposed differential amplifier.

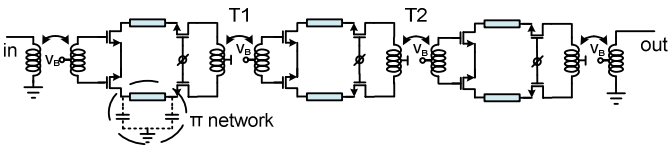

Figure 4. 144GHz fully differential CMOS amplifier schematic

It features three-stage amplification and adopts fully differential, common source cascode structure. Two transformers, T1 and T2, serve as inter-stage matching networks. The amplifier has single ended input and output to facilitate testing. An on-chip balun not only transfers the input single ended signal to differential signals to feed the amplifier, but also serves as matching network for 50ohm. The output is processed similarly. The amplifier can also be used as fully differential arrangement by simply converting the input/output baluns into normal transformers. Each stage's gate and drain biases are set through the transformer/balun center taps separately for independent optimization.

Cascode structure isolates the amplifier output from the input, which alleviates the Miller effect and stabilizes the design. However, the associated parasitic capacitors at the middle cascode node establish a low impedance node and greatly reduce the maximum achievable gain of each stage. These capacitors are mainly composed of C_{GD} of amplification device and C_{GS} of cascode device. To mitigate the effect, a serial transmission line stub is inserted between them to form a wide band inter-stage PI matching network, as shown in Fig. 4. It not only improves the amplifier gain profile, but also broadens the bandwidth that is a key spec for passive imaging application. The amplifier also uses an independent substrate bias for the cascode devices so as to tolerate as high as 2V supply voltage without degrading reliability.

III. PHYSICAL DESIGN AND FABRICATION

To mm-Wave amplifier, physical design is critical and determines the ultimate performance. We place the amplifier stages based upon signal stream and cascade them in identical sequence, as the schematic shown in Fig. 4. With this approach, it ensures minimum parasitics and realizes well matched symmetrical design; uniformed and structured design style simplifies the physical design and improves passive component modeling accuracy, which greatly reduces design iterations. Fig. 5 shows the die photo of this 144GHz fully differential CMOS amplifier. It is fabricated in 65nm CMOS technology and the amplifier core occupies 0.1X0.5mm^2. The die area is about 0.21mm^2 including PADs. To eliminate excessive parasitics, the input/output PADs only utilize top metal and they are incorporated into input and output matching network during design phase. There is no extra ESD protection in the input/output and still achieves very good ESD performance because the baluns isolate the active devices.

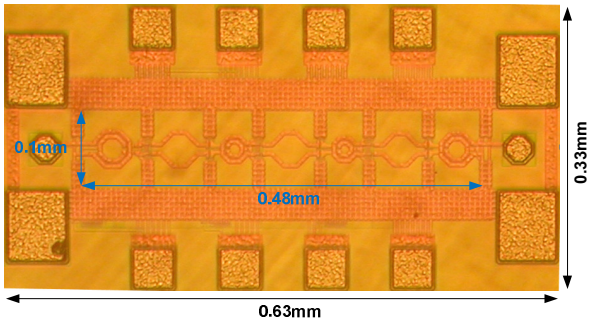

Figure 5. 144GHz CMOS amplifier die photo

IV. MEASUREMENT RESULTS

The amplifier performance characterization in such high frequency is a major challenge due to delicacy of the setup and lack of instruments. Fig. 6 shows our measurement setup. It uses a frequency multiplier chain to generate 140GHz signals and a power sensor to detect signal strength. A linearly adjustable attenuator is used to sweep the input power.

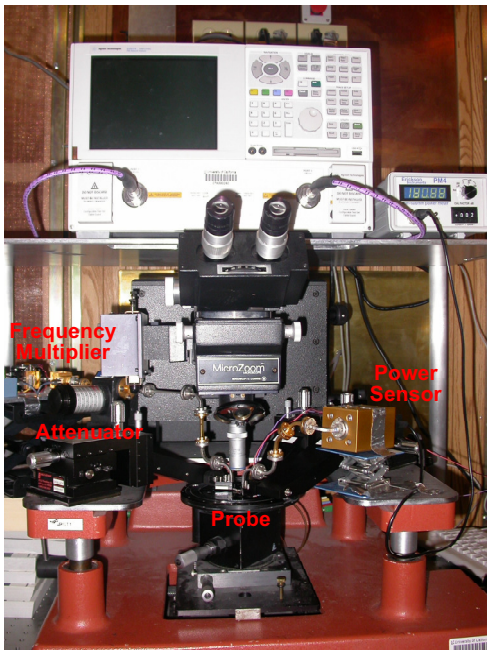

Figure 6. Measurement setup

Fig. 7 shows the measured output power versus input signal taking into account the setup loss. It confirms 18.05dB

amplifier gain and over 5.7dBm Psat and OP1dB at 154.4 GHz under 2V supply. The S-parameters are measured through a D band VNA, the results are shown in Fig. 8 and Fig. 9. The amplifier demonstrates 3dB lower gain when biased under 1.4V supply compared with 2V supply and shows consistent measurement results. It draws 39mA and 51mA from 1.4V and 2V supply, respectively. The measurement matches with simulation with 4dB gain difference, which validates the device modeling and design methodology. Table I summarizes the amplifier performance and supports the comparison with most recent CMOS amplifiers. This amplifier demonstrates highest gain with fully differential implementation.

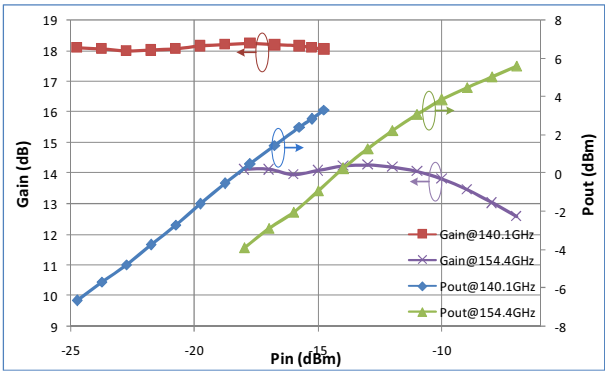

Figure 7. Measured amplifier large signal characteristics

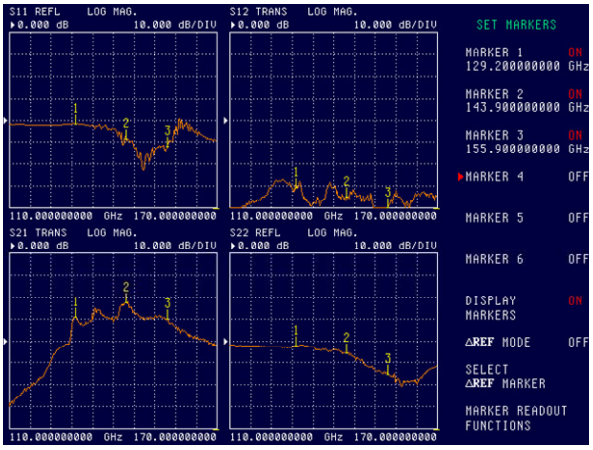

Figure 8. Measured S parameters under 1.4V supply

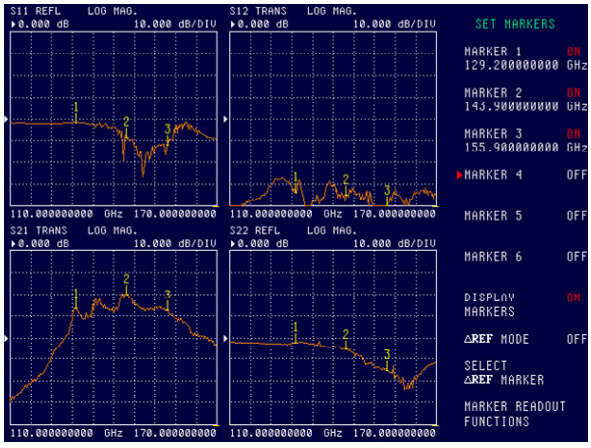

Figure 9. Measured S parameters under 2V supply

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

	This work	[3]	[4]	[5]
Architecture	**Differential**	Single End	Single End	Single End
No. of Stages	**3**	3	6	3
Technology	**65nm CMOS**	65nm CMOS	65nm CMOS	90nm CMOS
Center Frequency (GHz)	**144**	150	140	103.8
3dB BW (GHz)	**33GHz > 10dB Gain**	27	10	5
Gain (dB)	**20.6**	8.2	8	9.34
Psat (dBm)	**>5.7**	6.3	>-1.8	N/A
P1dB (dBm)	**5**	1.5	-5	N/A
S11 (dB)	**-24**	-7.4	N/A	-9.8
S22 (dB)	**-15**	-13.6	N/A	-5.5
Power Consumption (mW)	**54.6@1.4V 102@2V**	25.5	63	22
Core Area (mm2)	**0.05**	0.16	0.06	0.24

V. CONCLUSTIONS

A fully differential 144GHz amplifier with 20dB gain and 33GHz amplification bandwidth (with >10dB gain) has been successfully demonstrated in 65nm CMOS. It draws 51mA from a 2V supply and occupies compact 0.05mm^2 die area. To the author's best knowledge, it is the highest gain amplifier ever achieved at higher than 100GHz by using CMOS technology and sets the foundation for future CMOS implementations of communication, radar and passive imaging systems in D-band frequency spectra.

ACKNOWLEDGMENT

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