A 60 GHz High Gain Transformer-Coupled Differential Power Amplifier in 65nm CMOS

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***Abstract*— A fully differential 60 GHz three-stage transformer-coupled amplifier is designed and implemented in 65 nm digital CMOS process. On-chip transformers which offer DC biasing for individual stages, extra stabilization mechanisms, and simultaneous input/inter-stage/output matching networks are used to facilitate a compact circuit design. With a cascoded circuit configuration, the amplifier is tested with a linear gain of 30.5 dB centered at 63.5 GHz and a -40 dB reverse isolation under a 1 V supply. The amplifier delivers 9 dBm and 13 dBm output power under 1 V and 1.5 V supplies, respectively and occupies a core chip area of 0.05 mm^2. The measurement results validate a high gain and area efficient power amplifier design methodology in deep-scaled CMOS for millimeter-wave communication system applications.**

***Index Terms*— CMOS, differential amplifiers, millimeter-wave, transformers**

I. Introduction

The explosive growth of portable wireless communication has spurred the need for technologies that enable high data rate, short distance communications with low power consumption. The free 60 GHz ISM band, with its broad bandwidth (57 - 64 GHz), attracts more and more interest for short distance (<10 m) and ultra high throughput applications due to its high attenuation rate in the air. The amplifier is one of the essential building blocks in an integrated radio. Traditionally, millimeter-wave amplifiers are designed with exotic III-V technologies, such as GaAs, InP HEMT, which are expensive, less area effective and power hungry. CMOS technology is a well recognized choice in order to be successful in a high-volume market due to its low cost and high-level integration. However, the drawbacks in CMOS, such as the conductive and lossy substrate and constrained power supply due to low breakdown voltage, impose design difficulties, especially in amplifier design. In recent years, the feasibility of CMOS amplifier design in millimeter-wave has been demonstrated in [1]–[6], due to its ever-increasing device speed in super-scaled technologies.

In millimeter-wave design, the operating frequency is close to the device cut-off frequency, f_t, which challenges design efficiency. For example, the simulated f_t in 65 nm CMOS technology is about 180 GHz, shown in Fig. 1, for a transistor of 80 μm width with 1 μm per finger width and biased at 0.7 V. The maximum available gain of the same device is only 10 dB under the same bias condition as shown in Fig. 2. This limits the maximum achievable gain for each stage. By including the layout parasitics and losses of matching networks, the amplifier performance will be further degraded in millimeter-wave frequency range, such as 60 GHz. Therefore, millimeter-wave CMOS amplifier not only needs innovative design methodology and device optimization, but also demands careful physical layout for minimum parasitics to achieve optimum performance.

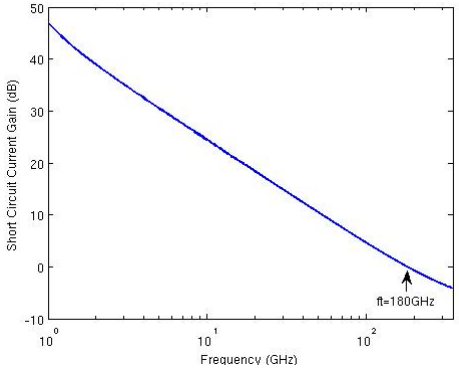


Fig. 1. Simulated short-circuit current gain.

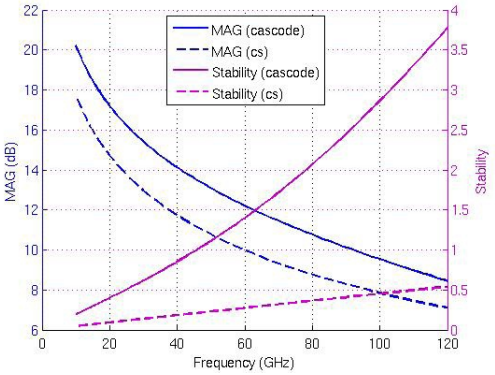


Fig. 2. Simulated maximum available gain and stability factor.

This paper presents a three-stage fully differential 60 GHz amplifier in 65 nm CMOS process with transformer-coupled inter-stage technique. Input, inter-stage, and output matching are realized with the on-chip transformers. Cascode configuration is chosen to achieve high gain performance and better reverse isolation. Device layout is optimized to minimize the gate resistance and parasitic capacitance of the cascode devices to minimize gain degradation.

The rest of this paper is organized as follows: Section II describes the design of the amplifier. The layout considerations are discussed in section III. The on-chip measurement setup and results are presented in section IV. Section V concludes the paper.

II. Amplifier Architecture And Design

The proposed millimeter amplifier is a three-stage, cascode design using the tsmc 65 nm 1P6M (six metal layers) standard digital process with 3.4 μm thickness top metal layer for low loss interconnect, inductor and transformer design. The schematic is shown in Fig. 3. The amplifier is biased at a class AB quiescent point. This bias point balances efficiency, gain, and power. Design details are explained as follows.

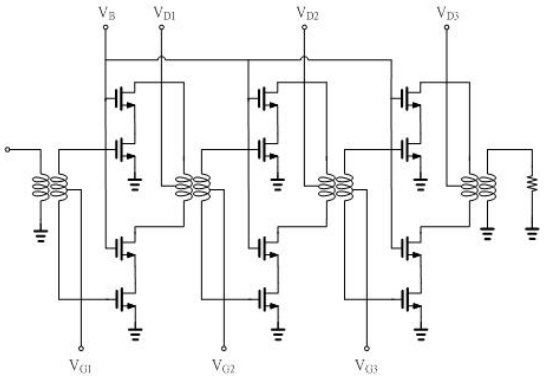


Fig. 3. 60 GHz CMOS amplifier schematic.

The differential configuration takes full advantage of virtual ground to reject common mode noise, lowers the even order harmonics, minimizes the interferences with other blocks, and doubles the power comparing to the single-ended structure with small area increment. Transformer combines the utilities of DC biasing and matching networks. DC biasing is applied at the center tap of the transformer that eliminates the need for a separate choke or bias line. This approach not only simplifies the physical design, but also optimizes the performance by providing well-matched differential signal paths. Furthermore, it helps to boost common-mode stability due to its inherent high pass characteristic and by adding stabilization network on the common mode nodes [6]. Transformer-coupled structure enables a compact millimeter-wave amplifier design.

Cascode topology is applied to each stage to achieve high gain, improve stability with good isolation and minimize Miller effect. The maximum available gains for both cascode device and common-source device are shown in Fig. 2. The cascode configuration has 3 dB more gain than its common-source counterpart at frequencies lower than 10 GHz. The gain superiority decreases when frequency increases because the layout parasitics are more pronounced. The maximum available gain for a single-ended cascode stage is 12 dB at 60 GHz. Simulated stability factor, shown in Fig. 2, shows that cascode configuration is more stable over the entire band than the common-source due to better reverse isolation provided by the cascode. An output-oriented design process [6] is adopted. The amplifier is designed such that the last stage moves into large-signal saturation first, with each preceding stage getting into saturation approximately 3 dB later for maximum power delivery. Individual finger width is chosen to be 1 μm for the first two stages and 1.2 μm for the last stage for optimal trade-off between gate resistance and capacitance that balances stability and gain. All transistors are of the minimum gate length (60 nm) for shortest channel transition time. The size of the last stage is 144 μm and the size ratio of the three stages is 1:2:4. The first stage is matched for maximum linear gain. A 1:2 vertically coupled transformer is selected at the input to boost up the voltage swing at the first stage, hence increasing the voltage gain. Vertically coupled transformer is preferred for its higher coupling factor. Gate terminal of the cascode device and power supply terminals are decoupled by high quality factor capacitors to provide a low impedance path to AC ground to facilitate stability. The bypass capacitors are placed as close as possible to the terminals. All the NMOS transistors are implemented in separate deep N-well to lower the harmonic distortion because the intrinsic gate-source capacitance variation is reduced by the junction capacitance formed between p-substrate and deep N-well, and to suppress the noise coupling through the conductive substrate [7].

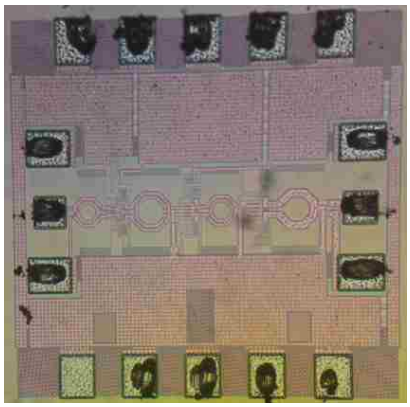
III. Layout

The layout of the amplifier is shown in Fig. 4(a). To improve the millimeter-wave amplifier performance, the gate resistance is minimized to improve fmax by breaking a large device into four identical unit cells. A simplified device layout in Fig. 4(b) shows the double gate connections. Layout parasitics between two cascode devices is minimized to avoid the loss at the internal node. Each terminal is parasitic extracted independently by the extraction tool to analyze its effect to the overall performance. A large VDD/GND plane is inserted to lower the serial inductance and resistance.

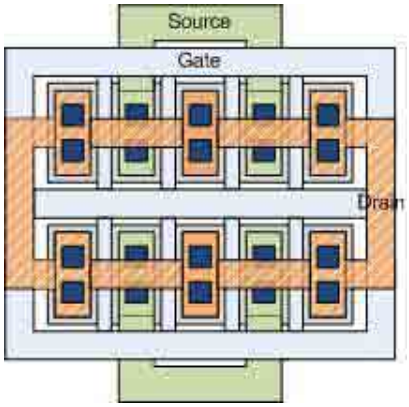
The amplifier occupies an area of 0.05 mm^2 excluding the pads and 0.3 mm^2 including the pads. In order to minimize the pad losses, the signal pad only consists of the top metal and its dimension is 50 μm $\times$ 50 μm. All the active devices, matching networks, interconnections and pads were simulated with full-wave EM simulators, HFSS and momentum.

IV. Measurement Setup And Results

A 60 GHz high gain amplifier is achieved in a compact design enabled by on-chip transformers. The measurement is performed through on-chip probing. The current consumption of the first stage is approximately 19 mA, the second stage



(a)



(b)

Fig. 4. (a) 60 GHz amplifier layout (core area 0.4 mm × 0.15 mm). (b) Simplified device layout.

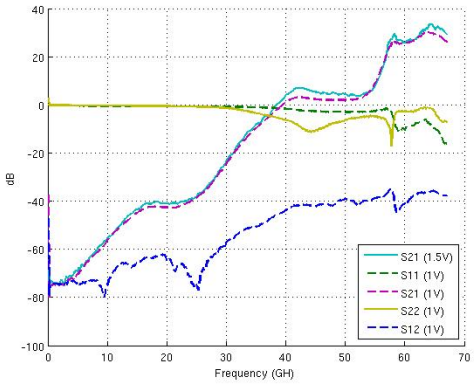


Fig. 5. Wideband linear response of the CMOS amplifier.

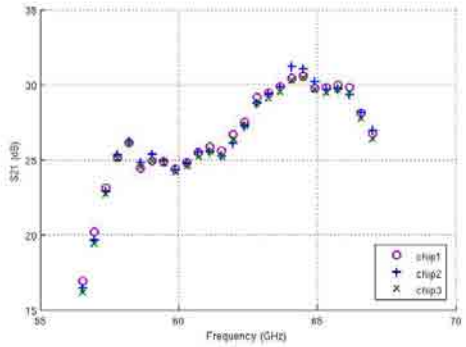


Fig. 6. In-band S21 of CMOS amplifier for three chips.

is 39 mA, and the last stage is 85 mA under 1 V supply voltage. When the supply voltage is 1.5 V, the current is 25 mA, 48 mA, and 140 mA for each stage, respectively. The gate oxide breakdown is 3 V for this 65 nm technology. Under both DC supplies, the transistors are well below the breakdown voltage to ensure reliability. The small-signal and large-signal measurement results are discussed in the following sections.

A. Small-Signal Performance

The amplifier S-parameter is tested from DC to 67 GHz using the Agilent 8731E network analyzer and calibrated using the Cascade SOLT GSG 101 calibration substrate. The amplifier peak linear gain under 1 V supply is greater than 30 dB centered at 63.5 GHz shown in Fig. 5. The 3 dB bandwidth is 4.2 GHz from 62.14 GHz to 66.3 GHz. The bandwidth can be further extended to cover the full band by using wideband matching networks. Under 1.5 V supply, the peak linear gain is 33.4 dB centered at 63.9 GHz.

Three different chips were tested to confirm the design robustness. The in-band linear gain is plotted in Fig. 6.

B. Large-Signal Performance

The large-signal performance is tested in a standard power measurement setup shown in Fig. 7. The signal source is provided by Agilent 83640A synthesized sweeper that drives an HP 83557A V-band millimeter-wave source module to generate 57 - 65 GHz signal. The output signal of the amplifier connects to the Agilent V8486A V-band power sensor. The power sensor is first calibrated with the power meter HP E4419B after warming-up for an hour.

We then carefully measure the swept input power before and after the probe tips that are connected by a short on-chip thru line using the Cascade Infinity I67 GSG probes. The measured loss of the probe tips, V-band coaxial, WR15 V-band waveguide transition is divided equally between the input and output, and the loss is de-embedded from the raw measurements. The final step is to test the large-signal performance. The error should be within 0.5 dB.

The swept power performance of the power amplifier is shown in Fig. 8. Under 1 V supply voltage, the gain is 31 dB with saturation power of 9 dBm, output-referred 1 dB compression point of 4 dBm and peak PAE of 7.2%. Under 1.5 V, the gain is 34 dB with saturation power of 13.17 dBm, output-referred 1 dB compression point of 7.8 dBm and peak PAE of 8.3%. The linear gain agrees with the small-signal measurement. The output power of the cascode is limited by the inevitable large headroom required by cascode devices. However, the cascode topology allows higher supply voltage without driving the transistors into breakdown region.

TABLE I
COMPARISON TO PRIOR ARTS

Reference	Technology	Gain (dB)	Psat (dBm)	Max. PAE (%)	Supply (V)	Area (mm^2)	Architecture
This work	65 nm	31	9	7.2	1	0.5×0.6	3-stage cascode
This work	65 nm	34	13.17	8.3	1.5	0.5×0.6	3-stage cascode
[1]	65 nm	13.4	13.8	7.6	1.2	1.5×0.6	4-stage CS
[2]	90 nm	14	6	6	1.5	0.3×0.5	3-stage (1^{st}&2^{nd} cascode, 3^{rd} CS)
[3]	90 nm	17	8.4	5.8	1.8	N/A	3-stage (1^{st} cascode, 2^{nd}&3^{rd} CS)
[4]	90 nm	10	12.6	6.9	1	0.8×0.8	3-stage CS
[5]	90 nm	19.5	8.2	4.2	2	1.18×0.96	3-stage cascode

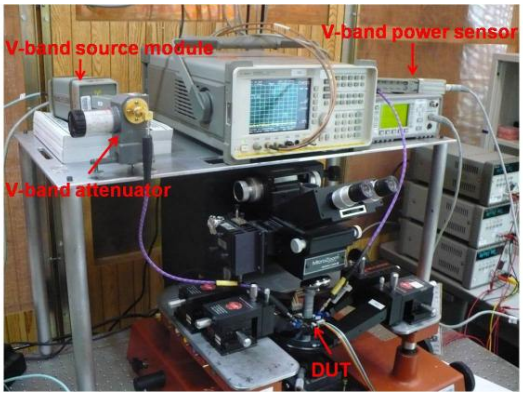
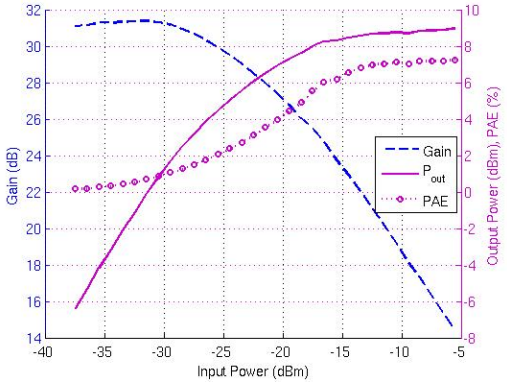
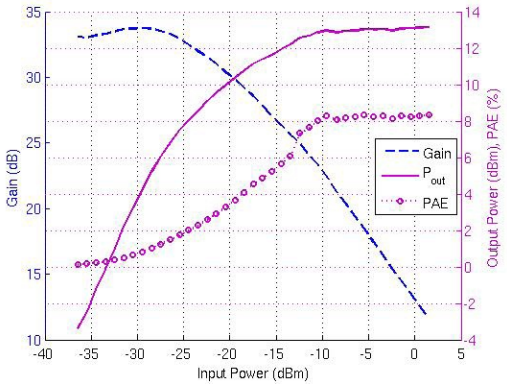


Fig. 7. Measurement Setup.



(a)



(b)

Fig. 8. (a) Swept power large signal performance of the amplifier under 1 V at 64 GHz. (b) Swept power large signal performance of the amplifier under 1.5 V at 64 GHz.

V. CONCLUSION

The design of a 60 GHz CMOS transformer-coupled three-stage differential power amplifier is reported. The presented amplifier is fabricated in a standard 65 nm CMOS technology. The on-chip measurement shows the gain exceeding 30 dB at 63.5 GHz. The amplifier consumes a quiescent current of 143 mA under a supply voltage of 1 V. The saturation output power is 9 dBm. This compact amplifier design only occupies 0.05 mm^2 excluding the pad area and 0.3 mm^2 including the pad area. The design is shown to be stable and repeatable. Compared to the prior arts in Table I, this amplifier shows an improvement in gain-area efficiency from the prototype based on the proposed design methodology.

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