200GHz CMOS Prescalers with Extended Dividing Range via Time-Interleaved Dual Injection Locking

Qun Jane Gu*, Heng-Yu Jian*, Zhiwei Xu*, Yi-Cheng Wu*, Mau-Chung Frank Chang*, Yves Baeyens** and Young-Kai Chen**

*University of California, Los Angeles, CA, USA
**Alcatel-Lucent/Bell-Labs, Murray Hills, NJ, USA

***Abstract* — An unique time-interleaved dual injection locking scheme has been devised to enable ultra high-speed and low-power frequency division with extended frequency locking range. To prove the concept, two frequency dividers (or prescalers) have been realized in 65nm digital CMOS: one divides continuously from 158GHz to 195GHz (or 21% locking range) with input signal < 0dBm and the other divides from 181GHz to 208GHz (or 14% locking range) with input signal < -1dBm. Both prescalers consume < 2.5mW at 1V supply and contribute negligible phase noise. These test results set the highest F.O.M. (2721 and 2188 GHz^2/mW, respectively) for prescalers implemented in any semiconductor technology up to this date, which in both cases is almost 10 times higher than that of prior arts.**

***Index Terms* — high speed prescaler/frequency divider, time-interleaved dual injection locking, figure-of-merit.**

I. Introduction

Electromagnetic radiation windows located at W- and G-band (i.e. 94GHz, 148GHz and 220GHz) has attracted increasing interest for the implementation of multi-gigabit/sec wireless communication and through-fabric/fog imaging systems. Continuous scaling has increased cut-off frequencies (f_t and f_{max}) of CMOS beyond 200GHz in 65nm CMOS and opened possibilities for various applications in these emerging areas. The prescaler after VCO is one of the most challenging building blocks in wireless communication and imaging systems due to very stringent requirements for high dividing frequency, wide locking range, high input sensitivity, and low power consumption.

In traditional prescaler designs, high dividing frequency and wide locking range often impose mutually conflicting requirements on resonant tank characteristics. Recently reported CMOS high-frequency dividers have clearly revealed such tradeoffs: Ref. [1] achieved a 14% locking range with lower than 100GHz dividing frequency; while Ref. [2, 3] achieved higher dividing frequencies (120GHz and 130GHz, respectively) but with limited locking range of about 7%.

To pave the way for realizing portable mm-Wave or Terahertz radio, radar and/or imaging systems, we have devised a time-interleaved dual injection scheme to ease prescaler design tradeoffs and successfully demonstrated G-band prescalers (up to 208GHz) with extended dividing ranges (up to 21%).

II. Conventional Schemes

From the frequency divider or prescaler's architecture point of view, high frequency injection locking schemes can be divided into two categories: Ring Oscillation based Injection locking frequency divider (RO-ILFD) and LC based Injection locking frequency divider (LC-ILFD). Ref [4] has carefully analyzed both types of injection locking schemes in terms of their operating mechanisms and design concerns to conclude that LC-ILFD is more suitable for high frequency division.

However, it is very challenging for conventional LC-ILFD to simultaneously achieve both high dividing frequency and wide locking range. This is because an injection locking divider's free-running oscillation frequency is determined by the tank self-resonant frequency of $\omega_o = 1/\left(\sqrt{L_{\tan k} C_{\tan k}}\right)$. To achieve higher dividing frequency, smaller $L_{\tan k}$ and $C_{\tan k}$ are required. However, Barkhausen gain criteria for oscillation demands a high resonant tank parallel impedance of $H_N = \omega_o L_{\tan k} Q$. With the constraint of choosing smaller $L_{\tan k}$ for higher frequency, the tank impedance can only be boosted by maximizing the quality factor Q, which narrows the locking range of the divider [4].

In order to develop a more effective and efficient approach in ultra-high frequency prescaler design, a novel time-interleaved dual injection scheme is presented in this paper to pave the road for future mm-Wave and Terahertz communication and imaging systems to achieve concurrently high dividing frequency, wide injection range, low power consumption and small silicon real estate.

III. Proposed Prescaler Architecture

A. Important Observations

Before discussing the newly devised time-interleaved

978-1-4244-6241-4/978-1-4244-6242-1/
978-1-4244-6243-8/10/$26.00 © 2010 IEEE

dual injection scheme and its insertion to a prescaler circuit, let us first review two traditional types of injection schemes which have never been clearly differentiated by past research: the voltage injection scheme and the current injection scheme. These two injection schemes operate based on completely distinct mechanisms that in reality have prevented them from working with each other in prior prescaler designs.

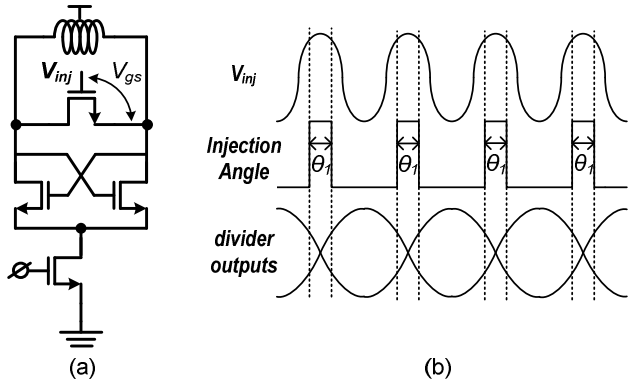

Fig. 1. (a) Voltage injection prescaler circuit insertion and (b) its effective injection angle θ_1 indicated around prescaler output's crossing period.

One circuit insertion example according to the voltage injection scheme is shown in Fig. 1(a). A voltage signal V_{inj} is injected through a NMOS mixer that shunts outputs of the crossing couple. As the injection voltage increases and the V_{gs} starts to exceed the device threshold, the mixer turns on and introduces a low impedance path to pull its source and drain (or the cross-coupled outputs) voltages closer. As a result, when voltage injection occurs at an instance outside of the output crossing time period of the prescaler, the voltage injection tends to pull outputs toward it. In case the prescaler's natural oscillation frequency is close to half of the injection frequency, such an effect will ultimately align the prescaler's output frequency and its phase with the voltage injection signal, as shown in Fig. 1(b). Consequently, the prescaler's output zero-crossings will naturally be synchronized (or locked) with voltage injection time zones, represented by the voltage injection angle θ_1.

On the other hand, the circuit insertion example for the current injection scheme is shown in Fig. 2(a). A current signal I_{inj} is injected via the current source of the crossing couple pair. During the positive (or negative) current injection cycle, the increased (or decreased) source current would split unequally to the resonant tank and increase (or decrease) the voltage difference between prescaler outputs. Provided the prescaler's natural oscillation frequency is close to half of the current injection frequency, the prescaler's output maximum (or minimum) points will be synchronized with effective current injection time zones, represented by the current injection angle θ_2, as shown in Fig. 2(b). Nonetheless, during the prescaler's output zero-crossing periods, I_{inj} flows as a common mode current which is distributed evenly to the prescaler's outputs without any push-or-pull locking effect.

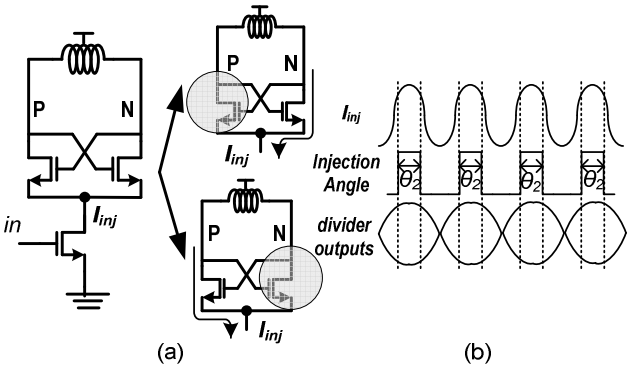

Fig. 2. (a) Current injection prescaler circuit insertion and (b) its effective injection angle θ_2 indicated around prescaler output's positive (or negative) peaking period.

B. Proposed Circuits

The aforementioned analyses have indicated that neither voltage nor current injection can synchronize or lock the prescaler's outputs at all time periods with its limited injection angle. It is therefore beneficial to interleave voltage and current injections at the prescaler's different output periods to extend its effective injection angle and consequently widen its locking range.

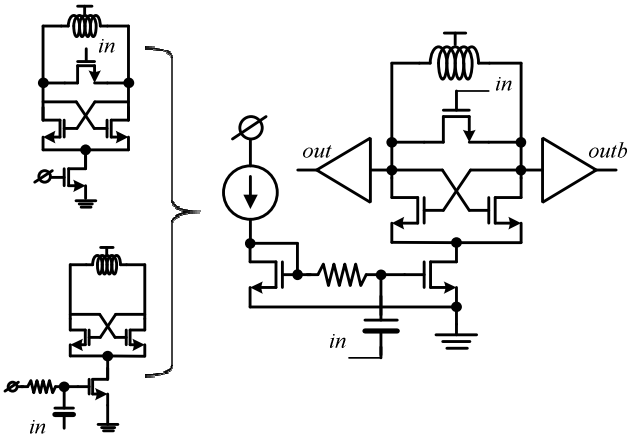

Fig. 3. A time-interleaved injection locking prescaler with enhanced injection angle.

The proposed dual-injection prescaler circuit topology is shown in Fig.3. The first injection is accomplished by injecting the signal voltage at the gate of the mixer that

shunts the cross-coupling pair's outputs. The second is accomplished by injecting signal current through the cross-coupling pair's common source node. The voltage and current injections will interleave in time to cover two different injection locking periods: one for the zero-crossing period and the other for the positive/negative peaks. By combining both of them, which are time-interleaved to each other, the prescaler's overall injection angle is substantially greater than either one individually.

Physical circuit simulations also confirm the effectiveness of such a combination: separate voltage and current injections achieve a locking range of 11.5% and 4%, respectively. By interleaving both types of injections, the prescaler obtains up to 16% locking range at 180GHz input frequency and -4dBm input power. To validate this time-interleaved dual injection locking scheme, two prescalers have been implemented in 65nm CMOS technology by varying the value of the loading inductors.

IV. Measurement Results

It is quite challenging to generate prescaler input signals at the G-band with sufficient power. Fig.4 shows our measurement setup. The signal from an external frequency synthesizer drives a multiply-by-3 and a subsequent power amplifier to generate signal at the W-band, which is then fed into a multiply-by-2 to produce the needed G-band input signal for prescaler wafer-probing. After dividing by 2, the prescaler output is down-converted by a mixer to feed into the spectrum analyzer to complete the test.

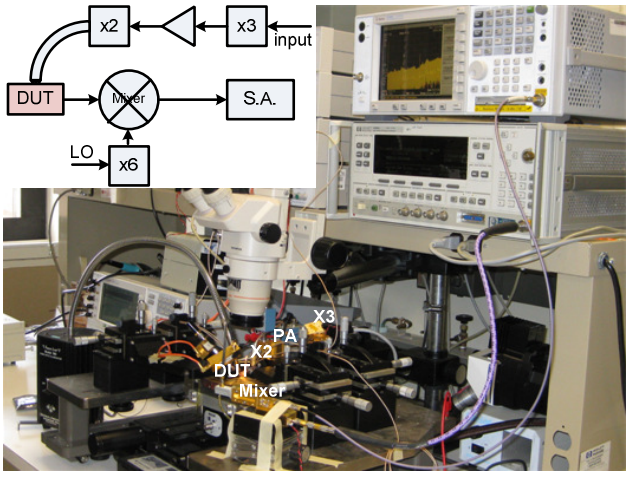

Fig. 4. Measurement setup.

Both prescalers' measurement results are shown in Figs. 5 and 6, respectively. The input sensitivity of the first prescaler is plotted by its minimum input power versus the input frequency. The measured locking range in Fig. 5(a) is over 37GHz (158GHz~195GHz, or 21%) with < 0dBm input power. Its lowest and highest frequency output spectra are also shown in Fig. 5(b). Correspondingly, the second prescaler's input sensitivity is plotted in Fig. 6(a) with 27GHz (181GHz~208GHz, or 14%) locking range with < -1dBm input power. Its lowest and highest frequency output spectra are shown in Fig. 6(b).

Fig. 5. FD-V1 measured results (a) input sensitivity (b) output spectrums at lowest/highest input frequencies of 156/195GHz.

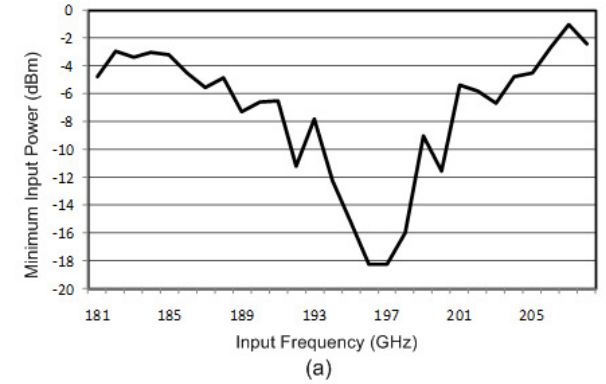

Fig. 6. FD-V2 measured results (a) input sensitivity (b) output spectrums at lowest/highest input frequencies of 181/208GHz

Phase noise measurement results are shown in Fig.7, which indicate -91.7dBc/Hz and -91.6dBc/Hz@100KHz offset for both prescalers, respectively. They are limited by the input source phase noise of -107dBc/Hz @100KHz at 1/6 of the prescaler output frequency. The added 15.4dB phase noise is mainly due to the frequency up-conversion effect. Both prescalers draw about 2.4mA from a 1V power supply.

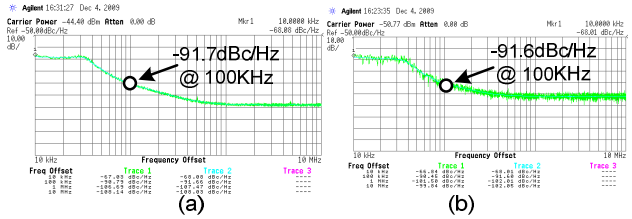

Fig. 7. Measured output phase noises of (a) first divide, (b) second divider.

A chip photo is shown in Fig. 8 with the core chip area 0.12mm x 0.09mm. Both prescalers possess the same area with the only difference being the inductor size.

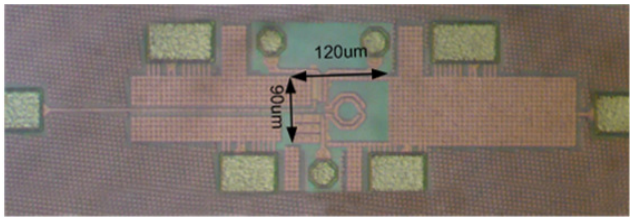

Fig. 8. Die photo of CMOS prescaler with time-interleaved dual injection locking.

Table 1 summarizes key performance measured from both prescalers and indicates that their performance figure-of-merits have exceeded prior arts substantially in terms of dividing frequency, locking range, and power consumption. We compare their performance according to a defined F.O.M. of

$$FOM = Center\ Frequency \times Locking\ Range / Power$$

where the center frequency and locking range are in Giga-Hertz (i.e. GHz) and power consumption in milli-Watt (i.e. mW). The measured F.O.M.s of our two prescalers are 2721 and 2188 GHz^2/mW, respectively, which are in either case almost 10 times higher than that of prior arts.

V. Conclusion

In summary, this paper successfully demonstrates an unique time-interleaved injection locking scheme for CMOS prescalers to achieve the highest dividing frequency (195GHz/208GHz) ever reported for any semiconductor technology (versus the highest dividing frequencies reported by SiGe [5] and InP HBT [6]), simultaneously having wide locking range (37GHz/27GHz), high input sensitivity (< -1dBm/0dBm across the bands), low phase noise (< -91dBc/Hz @100KHz offset), as well as low power consumption (2.4mW). The combined F.O.M. (2721/2188 GHz^2/mW) in either case has exceeded that of prior arts by almost 10 times [1-6]. The demonstrated time-interleaved dual injection scheme has paved the road to implement prescalers in commercial CMOS technology for future integrated mm-Wave and Terahertz communication/imaging systems.

Table 1 Performance comparison with CMOS state-of-the-arts.

	[1]	[2]	[3]	This Work	
Technology	65nm	90nm	65nm	65nm	65nm
Center Frequency	89GHz	121GHz	133GHz	176.5GHz	194.5GHz
Locking Range	82~94GHz (12GHz)	117~125GHz (8GHz)	128~137GHz (8.76GHz)	158~195GHz (37GHz)	181~208GHz (27GHz)
Input Power	0 dBm	N/A	N/A	0dBm	-1dBm
Phase Noise	N/A	N/A	-78.8dBc/Hz @400KHz	-91.7dBc/Hz @100KHz	-91.6dBc/Hz @100KHz
Power Consumption	3.92 mW	10.5 mW	5.5 mW	2.4mW	2.4mW
Chip Area	N/A	0.3mm* 0.14mm	0.32mm* 0.16mm	0.12mm* 0.09mm	0.12mm* 0.09mm
FOM (GHz^2/mW)	272	92	212	2721	2188

References

[1] P. Mayr, C. Weyers, and U. Langmann, "A 90GHz 65nm CMOS Injection-Locked Frequency Divider," *ISSCC Dig. Tech. Papers*, pp. 198-199, Feb., 2007.

[2] B. Razavi, "A Millimeter-Wave Circuit Technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2090-2098, Sep., 2008.

[3] B.-Y. Lin, K.-H. Tsai and S.-I. Liu, "A 128.24-to-137.00GHz Injection Locked Frequency Divider in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 282-283, Feb., 2009

[4] Q. Gu, Z. Xu, D. Huang, T. La Rocca, N. Y. Wang, W. Hant, and M. C. F. Chang, "A low power V-band frequency divider with wide locking range and accurate quadrature output phases," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 991–998, Apr. 2008.

[5] S. Trotta, H. Li, V.P. Trivedi and J. John, "A Tunable Flipflop-Based Frequency Divider up to 113GHz and a Fully Differential 77GHz push-push VCO in SiGe BiCMOS Technology," *IEEE Radio Frequency Integrated Circuits Symposium*, June 2009.

[6] Z. Griffith, M. Dahlstrom, M. Rodwell, "Ultra High Frequency Static Dividers >150 CHz in a Narrow Mesa InGaAs/InP DHBT Technology," 2004 Proceedings of the Bipolar/BiCMOS Circuits and Technology, 2004

[7] T.-N. Luo, Y. -J. E. Chen, "0.8mW 55GHz Dual-Injection-Locked CMOS Frequency Divider," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 3, pp. 620-625, Mar. 2008.