A Wide Locking Range and Low Power V-band Frequency Divider in 90nm CMOS

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Abstract

A new topology for injection locked frequency divider (*ILFD*) is proposed to achieve high speed, wide locking range and quadrature phase operation. The dividing mechanism is analyzed and agrees well with the simulation. A prototype is implemented in TSMC 90nm CMOS and realizes 4GHz locking range (55.8GHz-59.8GHz) with -3dBm input power and 5mW DC power consumption. The divider attains the widest locking range with the lowest power consumption to date for V-band frequency dividing applications.

Introduction

Wide range unlicensed band at 60GHz for wireless Ethernet and Wireless HDMI (or WirelessHD) demands broadband and low-power frequency dividers for efficient frequency syntheses. The CMOS solution is preferable for its higher integration and lower cost.

For high frequency operations, injection-locked frequency dividers (*ILFDs*) are superior to their digital counterparts in terms of maximum operation speed and low power consumption. However, conventional *ILFDs*, including the *LC type ILFD (LC-ILFD)* and *Ring Oscillator type ILFD (RO-ILFD)*, do not offer both wide locking range and high dividing speed simultaneously. The former is excellent in dividing speed but limited in locking range; the later is the opposite with wide locking range but with limited speed. In order to implement low power CMOS *ILFD* concurrently with sufficient locking range and dividing speed for *V-band* frequency synthesis applications, a new *WLR-ILDF* (*Wide Locking Range ILFD*) topology with combined strength of *LC-ILFD* and *RO-ILFD* is proposed.

Circuit Design and Analysis

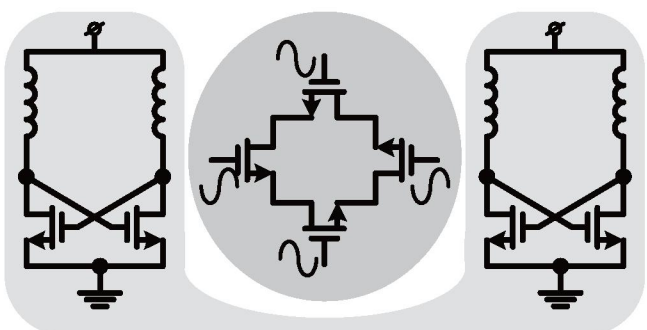

Fig.1 *WLR-ILFD* with mixer-loop sandwiched by cross-coupled pairs with resonance tanks

As depicted in Fig.1, this new *WLR-ILDF* comprises a loop of four NMOS-mixers sandwiched by two cross-coupled NMOS differential pairs with on-chip LC resonance tanks. The differential pairs are designed to resonate at the sub-harmonic of the input frequency like that of *LC-ILFD*. The loop of mixers is intended to produce proper locking range and quadrature phase outputs similar to that of *RO-ILFD*.

A. Locking Range

Since *ILFDs* work by synchronizing built-in oscillators to incident signals, both of their gain and phase should satisfy the Barkhausen criteria. As to the phase, the central loop of the *WLR-ILDF* is designated to provide $2k\pi$ phase shifts. The gain is analyzed according to Fig.2, which represents one of the NMOS loop mixers driven by an incident signal at the gate to synchronize subharmonic outputs between its drain and source. Equation (1) presents the effective drain loading by paralleling the tank impedance of $\left(H_0 \Big/ \left(1 + j\frac{2Q}{\omega_N}(\omega_o - \omega_N)\right)\right.$, where $H_0 = \omega_o LQ$) with the input resistance of $1/g_m$ seen to the following NMOS mixer source.

$$Z(j\omega_o) = 1/g_m \left\| \frac{H_0}{1 + j\frac{2Q}{\omega_N}(\omega_o - \omega_N)} \cong \frac{H_0}{H_0 g_m + j\frac{2Q}{\omega_N}(\omega_o - \omega_N)} \right. \quad (1)$$

where ω_N is the tank resonant frequency.

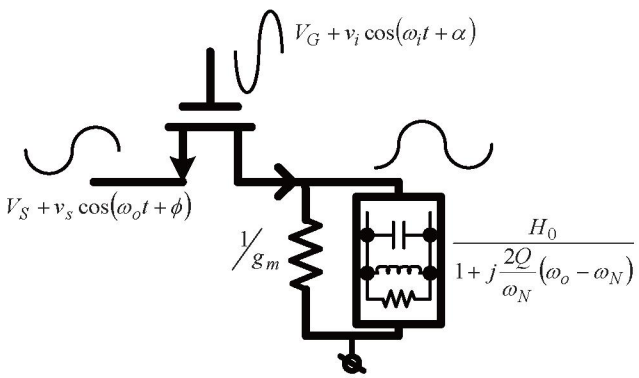

Fig.2 Divider locking range analysis

On the other hand, the drain current of the NMOS mixer is

$$I_d = K\left(V_G + v_i \cos(\omega_i t + a) - V_S - v_s \cos(\omega_o t + \phi) - V_{th}\right)^2 \quad (2)$$

where $K = 1/2\,\mu_n C_{ox}\, W/L$ and $\omega_i = 2\omega_o$ for the case of divide-by-two. Assuming frequency components distant from the tank resonance frequency will be filtered out, only those near the desirable output frequency are retained as

$$\begin{aligned} I_d(j\omega_o) &= K\left(-2v_s(V_{GS} - V_{th})\cos(\omega_o t + \phi) - v_i v_s \cos(\omega_o t + a - \phi)\right) \\ &= \mathrm{Re}\{Kv_s(V_{GS} - V_{th})e^{j\omega_o t} e^{j\phi}\left(-2 - \eta\cos(a - 2\phi) - j\eta\sin(a - 2\phi)\right)\} \end{aligned} \quad (3)$$

where the injection ratio is defined as $\eta = v_i/(V_{GS} - V_{th})$

To fulfill the Barkhausen criteria for oscillation, the gain of the mixer must exceed unity. Therefore, right at the dividing frequency, the amplitude of the output or drain voltage (v_d) must exceed that of the input or source voltage (v_s). Accordingly,

$$|v_d/v_s| \geq 1 \quad \Rightarrow \quad |v_d| = |I_d(j\omega_o) \times Z(j\omega_o)| \geq |v_s| \tag{4}$$

From (4), the locking range of the *WLR-ILDF* is derived as

$$\frac{\Delta\omega}{\omega_N} \leq \frac{H_0}{2Q} g_m \sqrt{\eta + \frac{\eta^2}{4}} \tag{5}$$

Analytic inequality of (5) reveals critical insights for *WLR-ILFD* design: Increasing H_0/Q, or device g_m, or incident ratio η can effectively improve the locking range. This analysis is further validated by circuit simulations as shown in Fig.3. For example, the locking range increases initially proportional to $\sqrt{\eta}$ and later to η as injection ratio increases. Compared with the locking range of $\Delta\omega = (\omega_N/2Q)(V_i/V_o)$ deduced for traditional injection locked oscillators [4], the *WLR-ILFD* offers enhanced locking range by implementing sufficiently high $H_0 g_m$.

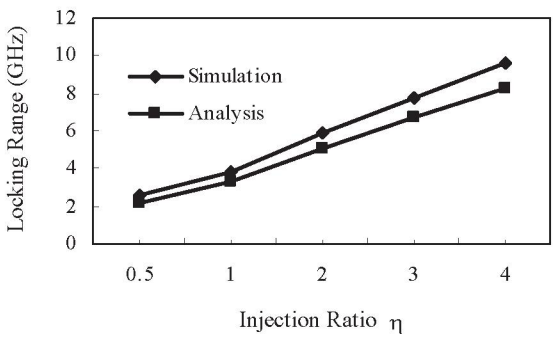

Fig.3 Locking range versus injection ratio η

B. Phase Accuracy

Firstly, the phase shift of the whole mixer loop is $2k\pi$. The phase shift between the drain and source of an individual mixer in the mixer loop is confined to quadrature when differential incident signals are presented to adjacent mixer gates. For this reason, the *WLR-ILFD* can maintain better phase accuracy than traditional *LC-ILFD*s. It is also superior in resisting phase deviation caused by mismatches of cross-coupled pairs due to device/process variations as simulated in Fig.4.

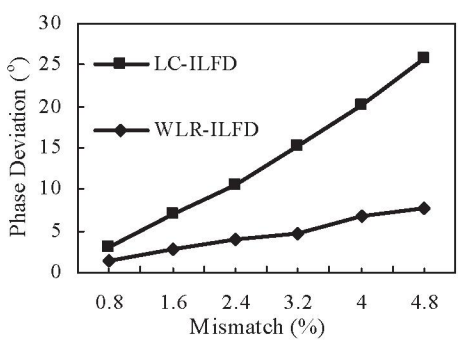

Fig. 4 Phase deviation versus mismatch in cross-coupled pairs

Measurement Results

Figure 5(a) records the minimum input power required by the prototype *WLR-ILFD* at dividing frequencies of V-band. The 4GHz (55.8-59.8GHz) locking range attained by -3dBm input power is lower than simulated results (about 6GHz with equivalent input voltage of 0.22V at 50 Ω load), probably due to hidden device parasitics that are not included in the simulation. The die photo is shown in Fig. 5(b) with a core area of 100μm x 150μm. As compared in Table 1, the *WLR-ILFD* achieves the widest locking range (4GHz) and the best dividing efficiency (F.O.M.=23.2GHz/mW when normalized to differential outputs) beyond the state-of-the-art for V-band applications.

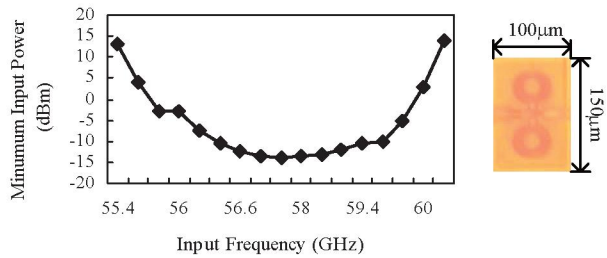

Fig. 5 (a) Measured minimum required input power versus dividing frequency (b) Die photo

Table 1 Comparisons with the state-of-the-art

	[1]	[2]	[3]	**This work**
Technology	0.15μm GaAs	0.2μm CMOS	0.18μm SiGe	**0.09μm CMOS**
Operation Frequency	64GHz	55GHz	60GHz	**58GHz**
Locking Range	2.81GHz	3.2GHz	350MHz	**4GHz**
Power Consumption (normalized to diff. outputs)*	7.5mW	10.1mW	25.2mW	**2.5mW**
FOM (GHz/mW)	8.5	5.45	2.38	**23.2**

* This work and ref [3] offer quadrature outputs.

Conclusions

A new *WLR-ILFD* topology for injection locked frequency divider has been devised to achieve high dividing frequency, wide locking range and quadrature phase outputs. A *WLR-ILFD* prototype is fabricated in TSMC 90nm CMOS and has realized the highest locking range (4GHz) simultaneously with the highest dividing efficiency (23.2GHz/mW) to date for V-band applications.

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