17.4 A 60GHz CMOS VCO Using On-Chip Resonator with Embedded Artificial Dielectric for Size, Loss and Noise Reduction

Daquan Huang, William Hant, Ning-Yi Wang, Tai W. Ku, Qun Gu, Raymond Wong, Mau-Chung F. Chang

University of California, Los Angeles, CA

In the past decade, the best frequency synthesizers of millimeter-wave communication systems were made from III-V (GaAs or InP) compound based HBTs because of high f_T and f_{max}, low $1/f$ noise, low substrate loss, and high-Q on-chip transmission lines and passive components [1, 2]. More recently, SiGe HBTs were also used for VCOs due to their low $1/f$ noise and high speed properties [3, 4]. However, these HBT technologies are more costly and less available than mainstream CMOS. It is thus beneficial to build high integration, low-cost communication systems using super-scaled modern CMOS technologies.

Although the speed of super-scaled CMOS is approaching that of III-V and SiGe HBTs, the lossy silicon substrate and metal interconnects of CMOS inevitably lead to low-Q transmission lines and lossy on-chip passive components. These issues hinder the development of key transceiver building blocks such as the VCO. Prior art has proposed use of a floating metal strip slow-wave structure underneath the transmission line to reduce the length of on-chip interconnects [5] and oscillators [6]. This approach has been extended to the use of embedded 2-dimensional artificial dielectrics [7] in order to shrink the resonator size, reduce metal/substrate losses and enhance resonator Q. In addition, CMOS varactors can be used to alter the artificial dielectric constant and thus tune the resonator frequency.

Figure 17.4.1 shows a coplanar strip line $\lambda/4$ standing wave resonator with underlying artificial dielectric consisting of a 2-dimensional array of conducting strips. These strips are embedded into a dielectric medium with permittivity ε. When an external electric field $\boldsymbol{E}$ is applied, the charges induced on the obstacles result in a dipole field with polarization density $\boldsymbol{P}$. The displacement $\boldsymbol{D}$ is given by $\boldsymbol{D} = \varepsilon\boldsymbol{E} + \boldsymbol{P} = \varepsilon'\boldsymbol{E}$, where ε' is the effective permittivity of the artificial dielectric. The artificial dielectric constant boost-factor is given by [7]

$$\kappa = \frac{\varepsilon'}{\varepsilon} = \frac{C'}{C}$$

where C' and C are the respective unit volume capacitance with and without the artificial dielectric.

Several advantages exist for this artificial dielectric medium. First, a large dielectric constant boost-factor leads to small size and high Q resonators. The plot in Fig. 17.4.2 of κ versus conducting strip horizontal spacing d, shows the size reduction of a resonator designed with and without an artificial dielectric. For our design with d = 0.6μm and $\kappa = 22$, the $\lambda/4$ resonator was reduced from 700μm, without artificial dielectric, to 150μm. Second, since current flow of the resonator is perpendicular to the conducting strips, conductive loss for the artificial dielectric is low. Third, the conducting strips shield the electromagnetic field from penetrating into the conductive substrate, and hence dramatically reduces the substrate losses.

A 60GHz VCO was designed and implemented in UMC 90nm CMOS to verify the effects of the embedded artificial dielectric on resonator size, loss, and noise reduction. As shown in the circuit diagram of Fig. 17.4.3, our design uses W/L=2μm/80nm NMOS for both the cross-coupled pair and the open drain output buffers. The coplanar line $\lambda/4$ resonator was designed for differential mode operation. The coplanar line, implemented in the top metal with w = 25μm and s = 50μm, occupies an area of 0.1×0.15mm^2. The artificial dielectric embedded underneath the coplanar line uses a total of 250 evenly distributed 0.6μm×100μm metal strips in the two lower metal layers. The artificial dielectric resonator, with simulated Q of 80, has reduced the resonator area by 79% as compared to a resonator without the artificial dielectric. 120 metal strips are individually connected to varactors, each made up of back-to-back NMOS pairs, with device size of W/L = 2μm/80nm. In order to block signal leakage from the frequency tuning path, the control voltage V_{ctrl} is externally applied through a bias-T and all of the varactor common ends are connected together at the symmetrical plane of the differential resonator where the differential signal "sees" a virtual ground (Fig. 17.4.3).

Frequency tuning is obtained by altering the electric length of the resonator through capacitance variation of the varactors. The tuning range for the VCO, Δf/f can be estimated from

$$\frac{\Delta f}{f} = -\frac{1}{2}\frac{\Delta C'}{C'} = -\frac{1}{2}\frac{\Delta C_v}{\kappa C + C_v}$$

where κC is the equivalent capacitance for the artificial dielectric, C_v is the total capacitance of the varactors, and ΔC_v is the available varactor tuning range. Using simulated C=0.2pF and assuming $\Delta C_v/C_v$=10%, Fig. 17.4.4 plots Δf/f as a function of κ. Tuning range decreases with higher κ and increases with larger C_v. The estimated frequency tuning range for this design is limited to under 0.6%, since this VCO is designed for large reductions of size, loss and noise. Limited tuning range is also due to the small varactor area (120×2×2μm×80nm) that covers only 0.3% of the effective area underneath the resonator and to the low varactor capacitance (about 400fF). The measured frequency tuning range was limited to 100MHz (0.2%) and can be improved in future designs by using more and larger varactors.

Figure 17.4.5 gives the measured VCO phase noise, the output spectrum and the performance summary. With the total current of 1.9mA from the 1V supply, the phase noise at 1MHz offset is measured as -100dBc/Hz. Fig. 17.4.6 shows that the corresponding figure of merit ($FOM=L(f_0)—20\log(f_0/f_{offset})+10\log(P_{DC}/1mw)$) is -193dBc/Hz. Note that even with CMOS $1/f$ noise typically one to two orders larger than that of the III-V and SiGe HBTs [1-3], this VCO, with embedded artificial dielectric resonator, achieves lower phase noise and FOM. These results confirm the effectiveness of the artificial dielectric in size, loss and noise reduction. Fig. 17.4.7 shows a die micrograph of the 60GHz CMOS VCO with the artificial dielectric resonator.

In summary, we have realized a 60GHz CMOS VCO with a measured phase noise of -100dBc/Hz and a -193dBc/Hz FOM at 1MHz offset. This VCO dissipates 1.9mW from a 1V power supply and occupies a chip area of 0.015mm^2 which is less than 10% of prior art (Fig. 17.4.6).

Acknowledgements:
The authors would like to thank DARPA for contract support and UMC for the foundry service.

References:

[1] P. Ma, et al., "1/f noise of AlGaAs-GaAs HBTs controlled by biasing an on-ledge Schottky diode," Proc. Bipolar/BiCMOS Circuits and Technology Meeting, pp. 211-213, Sept. 2000.
[2] J. Kim, et al, "A 60GHz InGaP/GaAs HBT push-push MMIC VCO," IEEE MTT-S International Microwave Symposium Digest, vol. 2, pp. 885-888, June 2003.
[3] J. S. Dunn, et al., "Foundation of RF CMOS and SiGe BiCMOS technologies," IBM J. Res. & Dev. vol. 47, no. 2/3, pp. 101-138, March/May 2003.
[4] B. A. Floyd," V-Band and W-Band SiGe Bipolar Low-Noise Amplifiers and Voltage-Controlled Oscillators," IEEE RFIC Symposium Dig., pp. 295-298, June 2004.
[5] T. S. D. Cheung, J. R. Long, et al., "On-Chip Interconnect for mm-wave applications using an all-copper technology and wavelength reduction," ISSCC Dig. Tech. Papers, pp. 396-501, Feb. 2003.
[6] W. F. Andress and D. Ham, "Standing Wave Oscillator Utilizing Wave-Adaptive Tapered Transmission Lines," IEEE J. of Solid-State Circuits, vol. 40, no. 3, pp. 638-651, March 2005.
[7] R.E. Collin, "Field Theory of Guided Waves" 2nd Edition, pp. 749-786, IEEE Press, New Jersey, 1990.

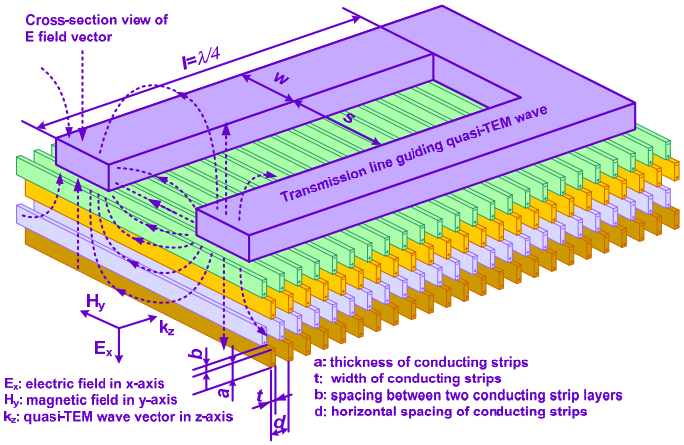


Figure 17.4.1: Quarter wavelength standing wave resonator with underlying artificial dielectric made of CMOS interconnects.

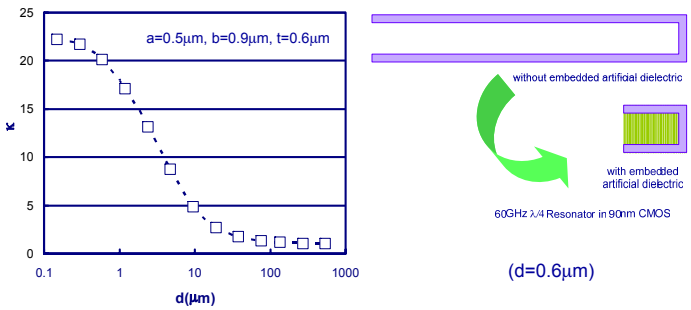


Figure 17.4.2: Dielectric constant boost-factor versus horizontal spacing of conducting strip and resonator length shrink effect.

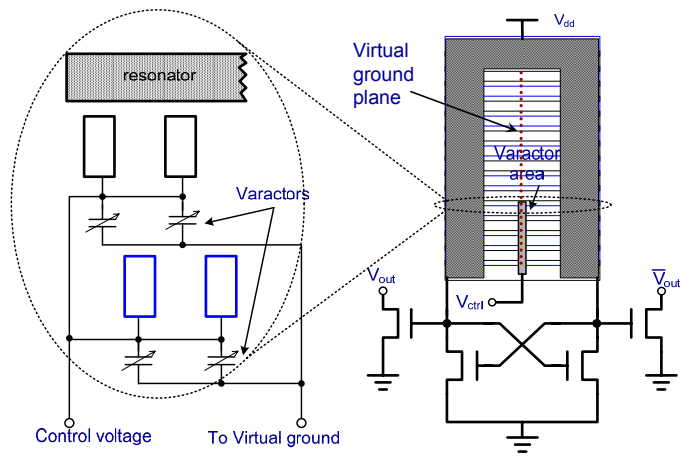


Figure 17.4.3: VCO schematic with varactor connection enlargement.

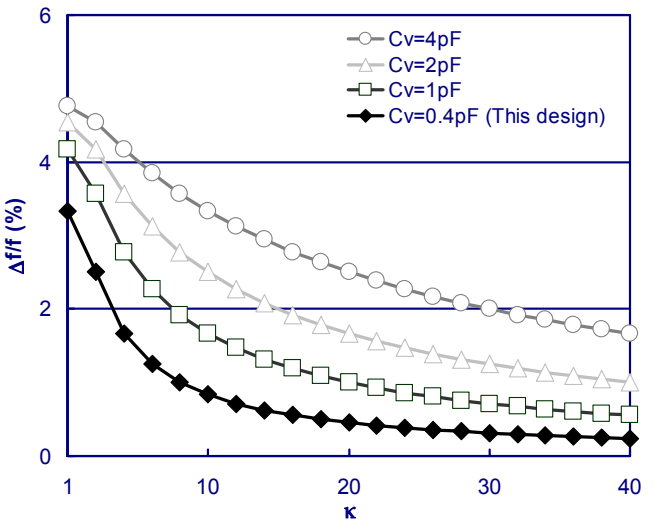
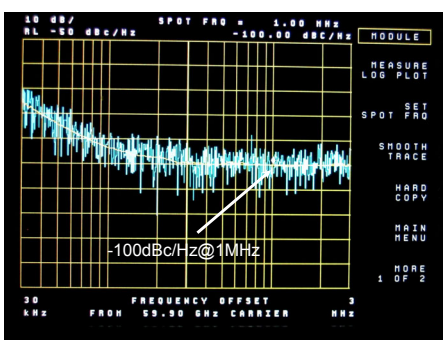
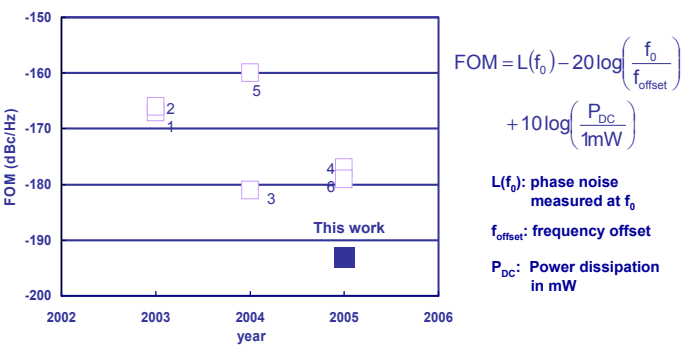


Figure 17.4.4: Frequency tuning versus dielectric constant boost-factor.



Phase noise	-100dBc/Hz at 1MHz
Figure-of-Merit	-193dBc/Hz at 1MHz
Operating frequency	60GHz
Frequency tuning range	100MHz
Supply voltage	1V
Power consumption	1.9mW
Chip area	0.015 mm²

Figure 17.4.5: Measured Phase noise, spectrum and VCO performance.



Reference.	Process	f_0 (GHz)	Power supply(V)	P_{DC} (mW)	Phase noise (dBc/Hz)	FOM (dBc/Hz)	Die area (mm²)
1 J.Kim, MTT-S, 2003	InGaP/GaAs HBT	60	3.5	158	-93@1MHz	-167	0.78
2 Y.Baeyens, MTT-S, 2003	SiGe HBT	150	6.5	163	-85@1MHz	-166	0.46
3 B.A. Floyd, RFIC, 2004	SiGe	67	3	25	-98@1MHz	-181	-
4 Y.Cho, RFIC, 2005	0.18um CMOS	53	2.1	27	-97@1MHz	-177	0.20
5 R.Liu, ISSCC, 2004	0.25um CMOS	63	1.8	119	-85@1MHz	-160	0.32
6 P.Huang, ISSCC, 2005	0.13um CMOS	114	1.2	8.4	-107.6@10MHz	-179	0.20
This work	90nm CMOS	60	1	1.9	-100@1MHz	-193	0.015

Figure 17.4.6: FOM comparison.

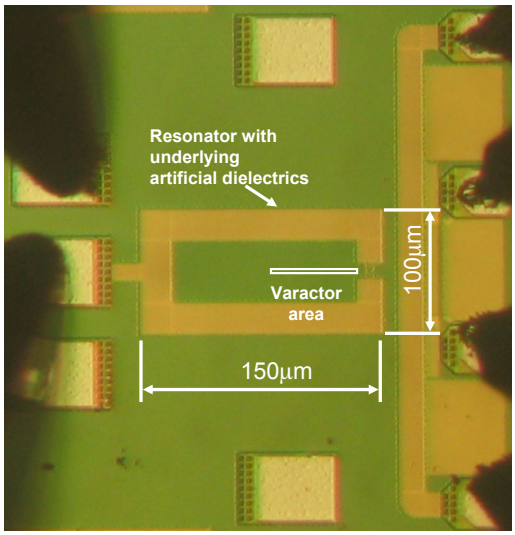


Figure 17.4.7: Die micrograph.

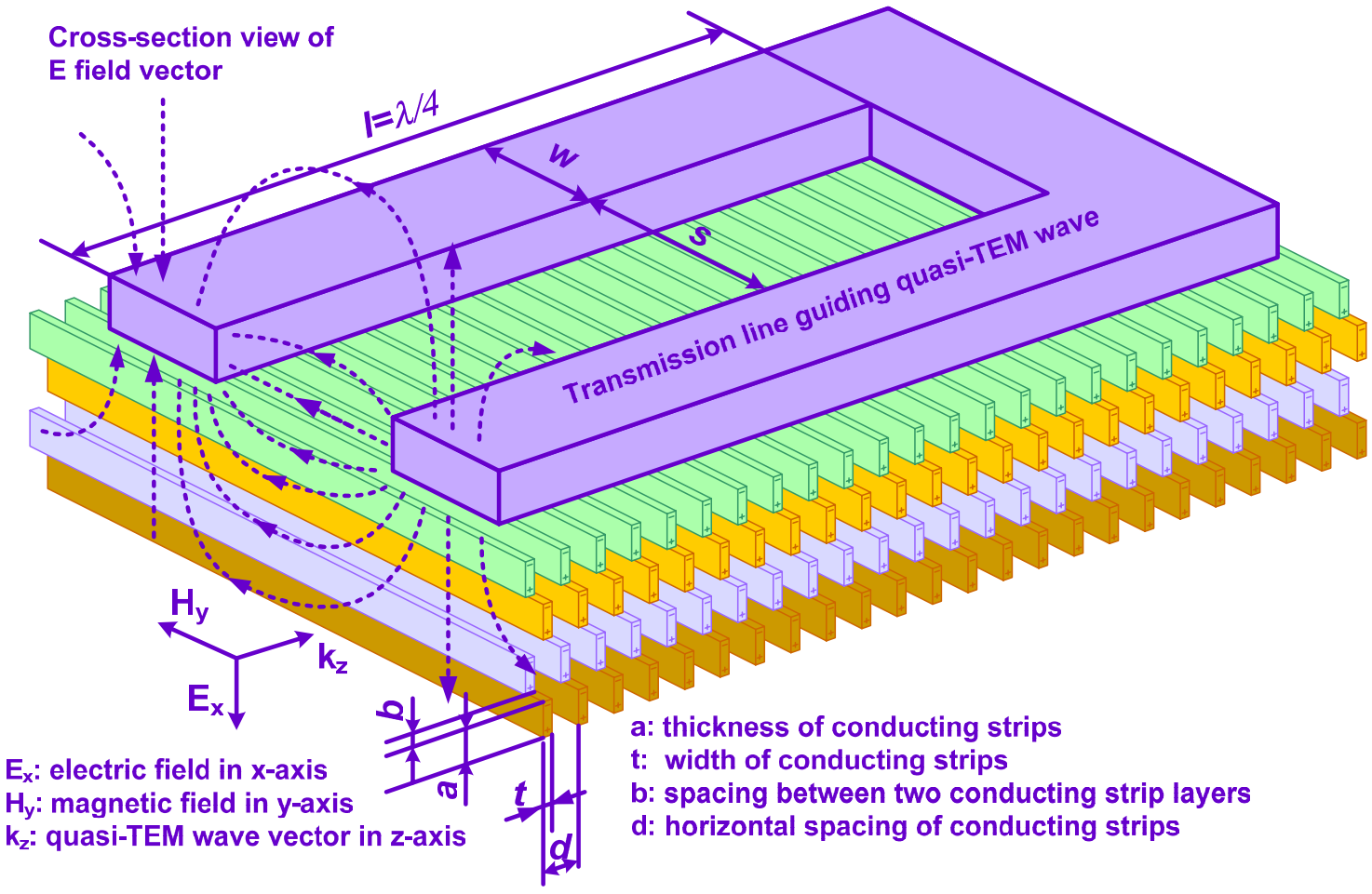


Figure 17.4.1: Quarter wavelength standing wave resonator with underlying artificial dielectric made of CMOS interconnects.

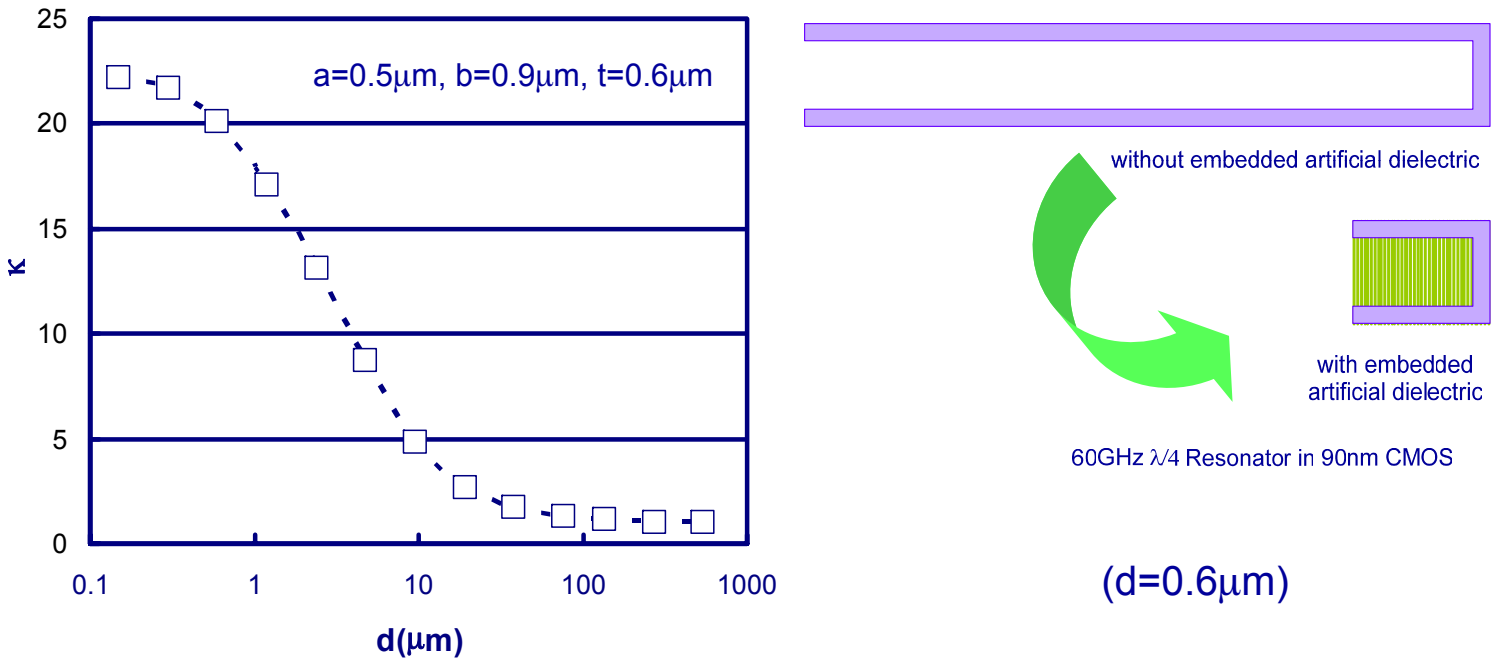


Figure 17.4.2: Dielectric constant boost-factor versus horizontal spacing of conducting strip and resonator length shrink effect.

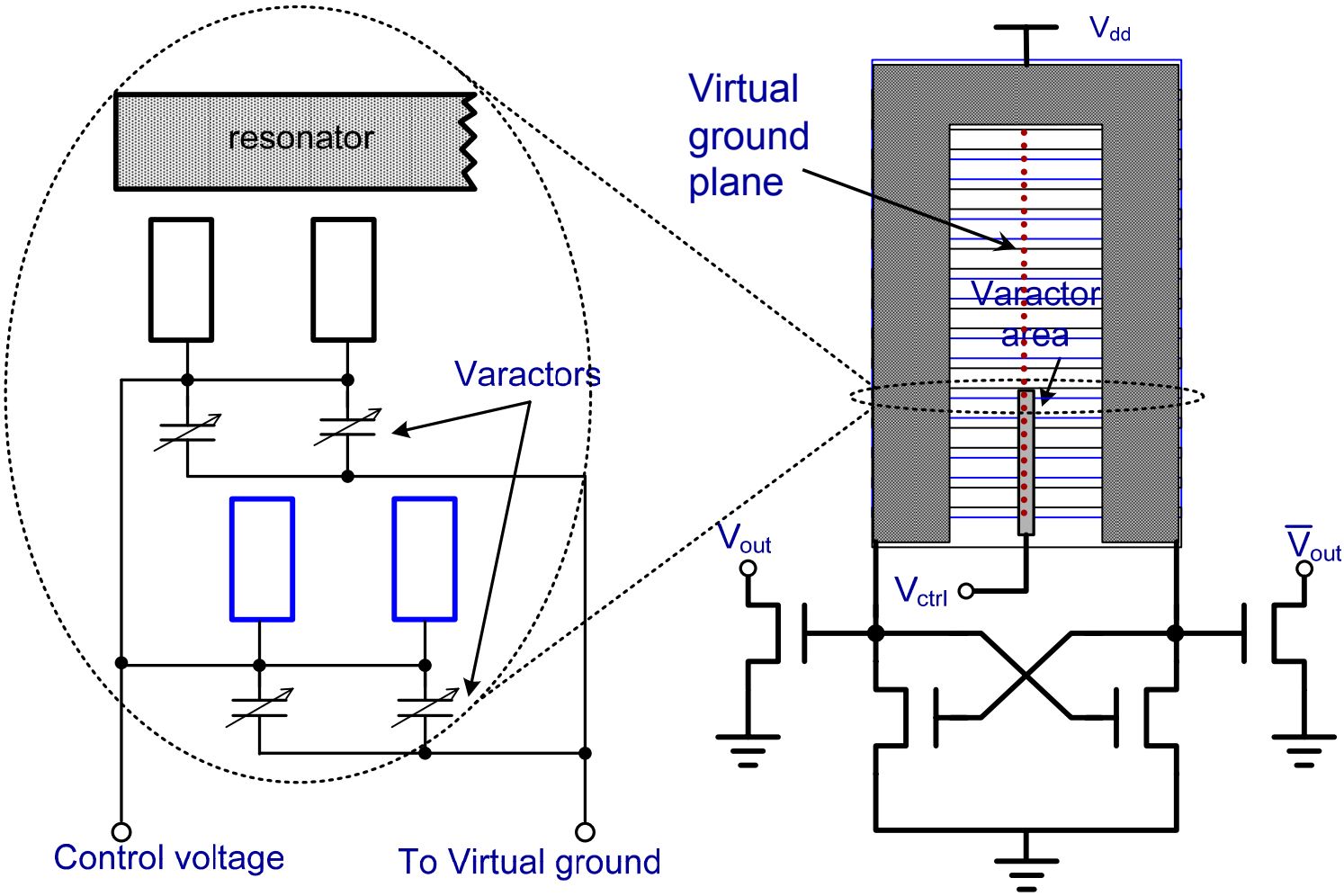


Figure 17.4.3: VCO schematic with varactor connection enlargement.

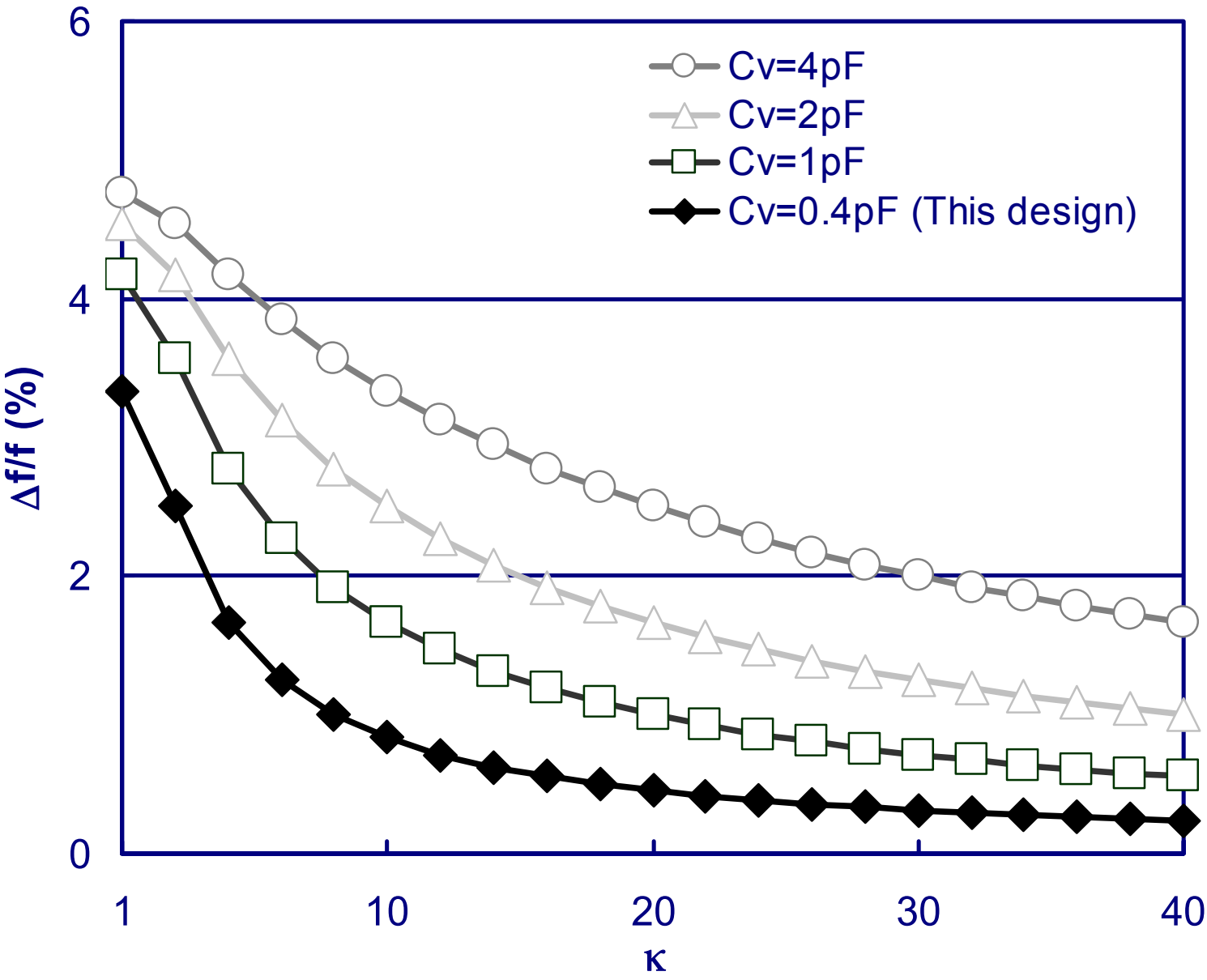
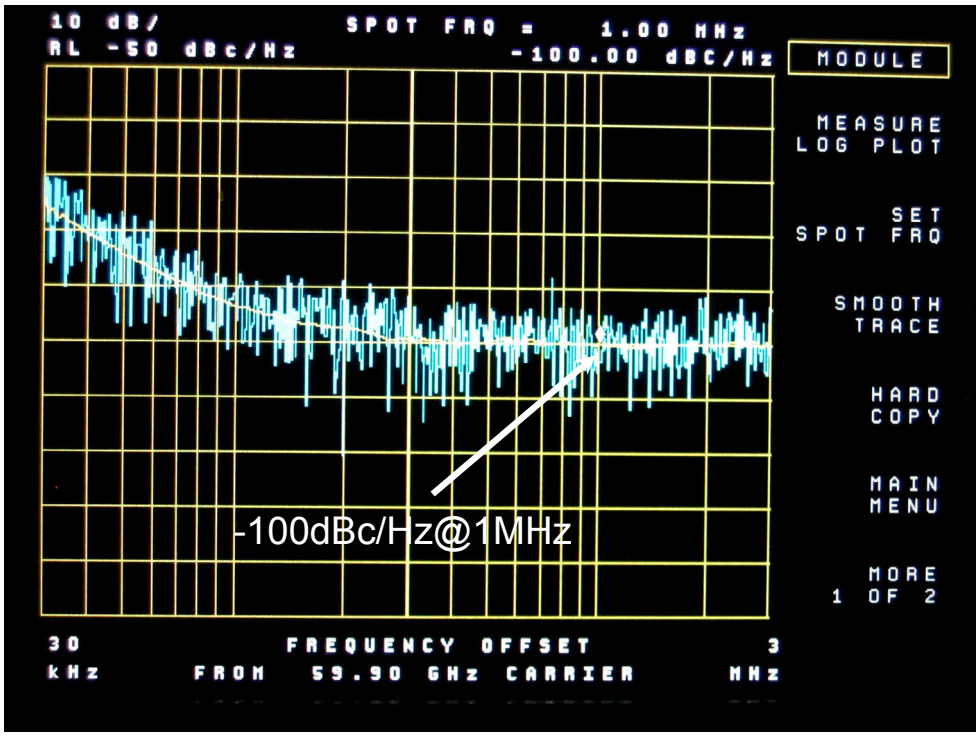
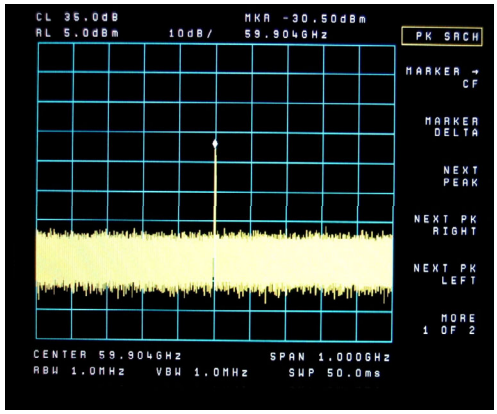


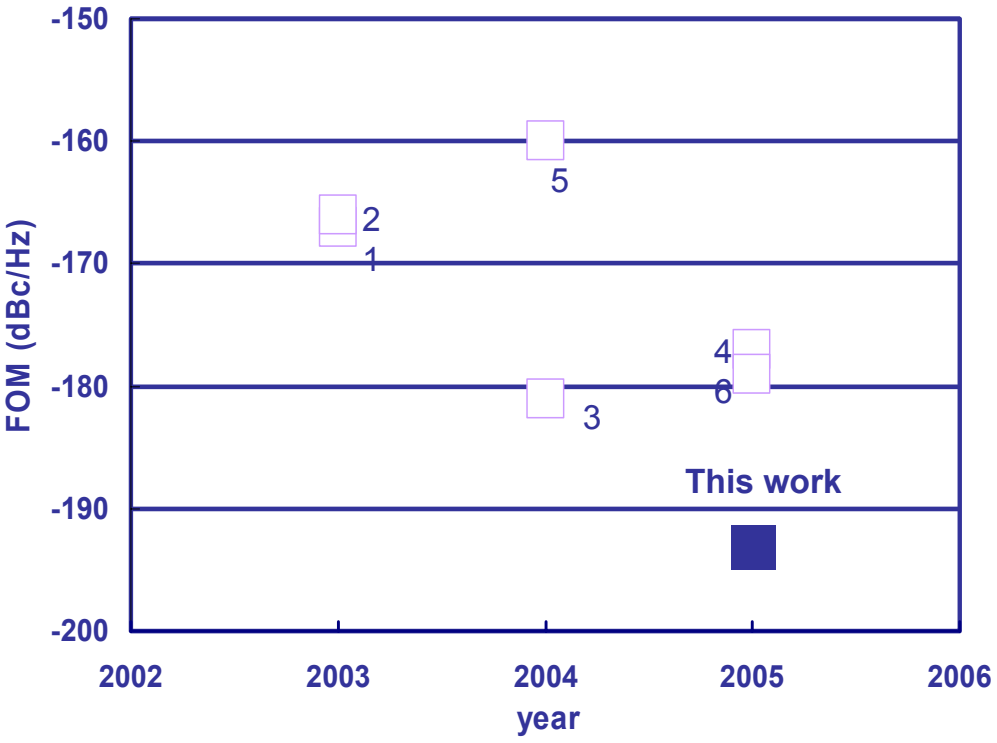
Figure 17.4.4: Frequency tuning versus dielectric constant boost-factor.





Phase noise	-100dBc/Hz at 1MHz
Figure-of-Merit	-193dBc/Hz at 1MHz
Operating frequency	60GHz
Frequency tuning range	100MHz
Supply voltage	1V
Power consumption	1.9mW
Chip area	0.015 mm^2

Figure 17.4.5: Measured Phase noise, spectrum and VCO performance.



$$FOM = L(f_0) - 20\log\left(\frac{f_0}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right)$$

$L(f_0)$: phase noise measured at f_0

f_{offset}: frequency offset

P_{DC}: Power dissipation in mW

Reference.	Process	f_0 (GHz)	Power supply(V)	P_{DC} (mW)	Phose noise (dBc/Hz)	FOM (dBc/Hz)	Die area (mm^2)
1 J.Kim, MTT-S, 2003	InGaP/GaAs HBT	60	3.5	158	-93@1MHz	-167	0.78
2 Y.Baeyens, MTT-S, 2003	SiGe HBT	150	6.5	163	-85@1MHz	-166	0.46
3 B.A. Floyd, RFIC, 2004	SiGe	67	3	25	-98@1MHz	-181	-
4 Y.Cho, RFIC, 2005	0.18um CMOS	53	2.1	27	-97@1MHz	-177	0.20
5 R.Liu, ISSCC, 2004	0.25um CMOS	63	1.8	119	-85@1MHz	-160	0.32
6 P.Huang, ISSCC, 2005	0.13um CMOS	114	1.2	8.4	-107.6@10MHz	-179	0.20
This work	90nm CMOS	60	1	1.9	-100@1MHz	-193	0.015

Figure 17.4.6: FOM comparison.

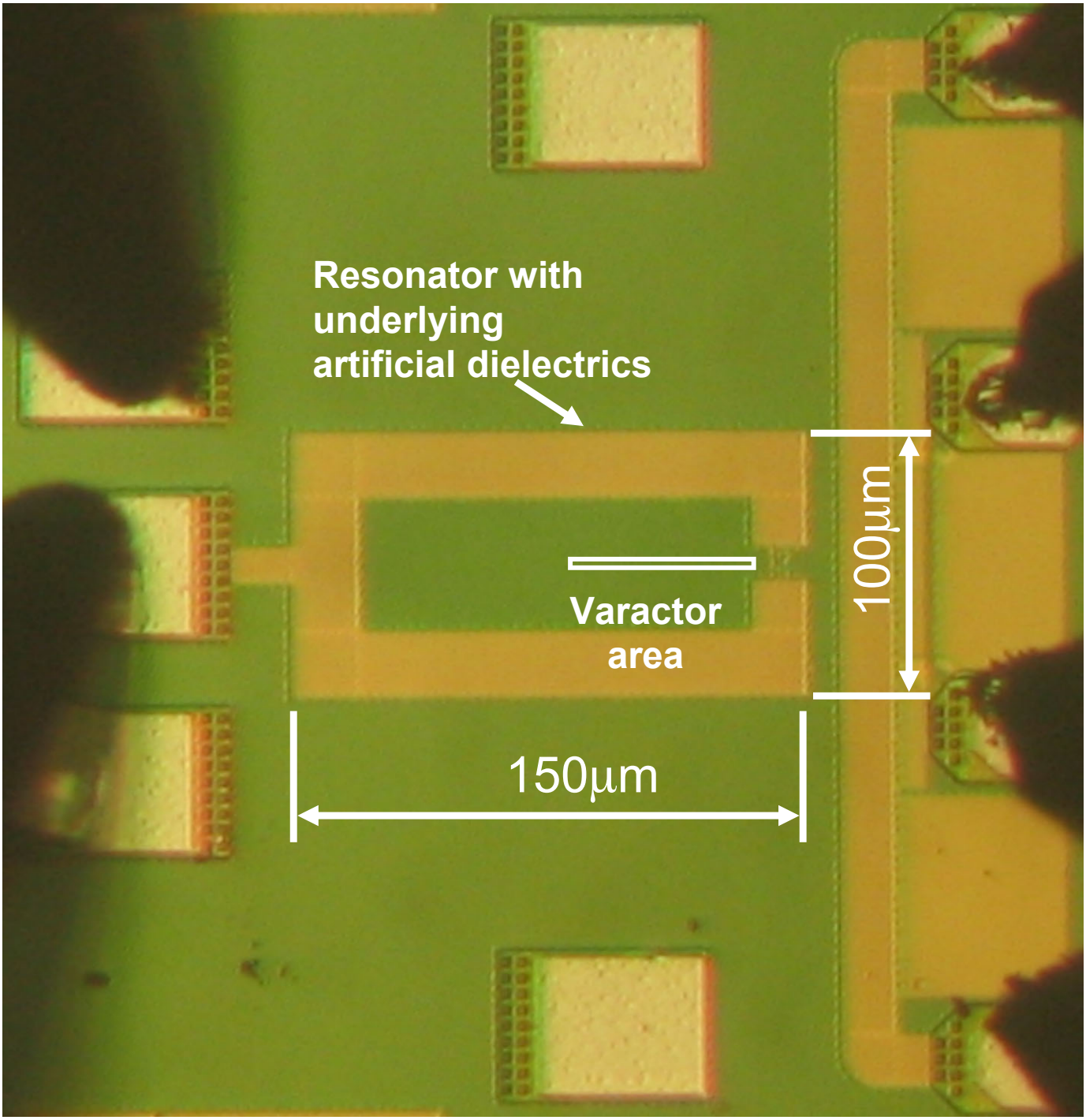


Figure 17.4.7: Die micrograph.