A 60GHz CMOS Differential Receiver Front-End Using On-Chip Transformer for 1.2 Volt Operation with Enhanced Gain and Linearity

Daquan Huang[1], Raymond Wong[1], Qun Gu[1], Ning-Yi Wang[1], Tai W. Ku[1],
Charles Chien[2] and Mau-Chung Frank Chang[1]
[1]University of California at Los Angeles, CA90095, USA, [2]SST Communications Co., Los Angeles, CA90045, USA

Abstract

A compact 60GHz CMOS differential direct conversion receiver front-end based on eight-metal-layer interleaved on-chip transformers is realized for low voltage (1.2V) and high gain (24dB) operation with input 1dB compression point of -11dBm, Noise Figure of 10.5dB and power consumption of 4.3mW/arm. Compared with prior arts in CMOS, this receiver achieves the highest gain without an output buffer, highest linearity, lowest noise, and lowest power consumption with smallest die area of 0.022mm^2.

Introduction

The 7GHz unlicensed band around 60GHz has sparked growing interest for high-data-rate wireless communications in CMOS[1-3] due to its low cost and high level of integration with digital circuits. Challenges of 60GHz RF front-end designs in super-scaled CMOS are attributable to two major reasons: 1) the continual lowering supply voltage required by low power digital circuit shrinks voltage headroom and thus degrades the gain and linearity in RF/mixed-signal circuits; 2) the inherent capacitive nature of CMOS diminishes device gain at high frequency. For example, assuming 0.5V for both the overdrive voltage $V_{ov}=V_{GS}-V_{th}$ and the signal peak-to-peak voltage V_{pp}, the traditional telescopic cascode structure requires a minimum supply voltage of 1.5V for a 2 stage stacking amplifier and 2V for a 3 stage stacking Gilbert mixer, while the supply voltage is only 1-1.2V in typical 90nm CMOS. Using horizontal cascade topology may solve this headroom problem. However, coupling between consecutive stages raises other design issues. For instance, DC coupling requires bias leveling circuitry between the stages, which often induces additional parasitic and degrades circuit's high frequency performance; the capacitive coupling not only constrains the bandwidth but also consumes large area (especially in differential circuits). This paper introduces an on-chip transformer enabled horizontal structure which relaxes the headroom problem and helps accomplish high gain and high linearity for low voltage operation. A 60GHz differential direct-conversion receiver front-end in 0.13μm CMOS has been implemented to verify the feasibility.

Circuit Architecture Description

Figure 1 shows the concept of applying a transformer to cascade a two-stage common-source (CS) amplifier. The first CS stage is designed for achieving high current gain with the aide of a serial resonant loop made of an inductor L_1 and a parasitic C_{gs1} of the M_1 CMOS gate. At the frequency of interest, L_1 resonates out C_{gs1} such that the effective transconductance of M_1 becomes $Q_1 \times g_{m1}$, where Q_1 is the quality factor of the series tank and g_{m1} is the transconductance of M_1. This current gain is enhanced by the transformer between M_1/M_2 stages with primary-to-secondary turn ratio of N_1/N_2 and further enhanced by the M_2 amplifier with an input serial resonant loop made of L_2 and C_{gs2}. Neglecting the output resistance of M_1 and M_2 transistors, the overall current gain can be expressed as

$$A_I = \frac{I_{out}}{I_{in}} = \frac{I_{d1}}{I_{in}}\frac{I_{g2}}{I_{d1}}\frac{I_{out}}{I_{g2}} = (Q_1 g_{m1} r_1)\left(\frac{N_1}{N_2}\right)(Q_2 g_{m2} r_2) = \left(\frac{N_1}{N_2}\right)\omega^2 L_1 L_2 g_{m1} g_{m2} \quad (1)$$

with the corresponding voltage gain of

$$A_V = A_I \frac{Z_L}{Z_{in}} \quad (2)$$

In our design, we choose N_1/N_2=3, Q_1 and Q_2 to be >2 and <3 to compromise the receiver front-end gain, bandwidth and stability performance.

Several advantages exist with this front-end topology. First, by separating the transistor DC biasing from its signal path, the inter-stage transformer allows each CMOS to reach its full swing up to the supply voltage, thus achieving higher linearity. Second, it facilitates the inter-stage impedance matching with simultaneous gain enhancement. Third, transformers with center taps are inherently compatible with the intended differential circuit architecture. Fourth, small CMOS (W<7μm) with higher f_{max} and lower gate paracitics can be used to resonate with higher serial inductance for 60GHz operation, which leads to low power dissipation. Finally, the series resonators act as built-in filters prior to active CMOS devices, which are instrumental in lowering the noise figure of the overall receiver system.

Eight-metal-layer Interleaved On-Chip Transformer

In this paper, we use transformers for signal coupling and impedance matching between stages. However, the silicon substrate/metal losses are significant with traditional large-area transformers. To solve this problem, we invented an multilayer-interleaved structure, in which all 8 metal layers are interleaved both horizontally and vertically[4], as shown in Fig.2. The interleaved structure greatly shrinks the transformer size (typically by a factor of 50 to 100) and thus reduces the loss and parasitic capacitances with enhanced coupling coefficient. With a size of only 20×20μm^2 and an effective turn ratio of 3:1, this interleaved transformer provides an inductance of 0.8nH at 60GHz for the primary end with a coupling coefficient of 0.78. The self-resonant frequency is simulated greater than 100GHz (Fig.3). Moreover, implemented with high symmetry, the compact interleaved structure increases the mutual inductance and enforces differential phase matching across the transformer ports. The small size also reduces the capacitance between the transformer and the silicon substrate, which helps reduce the substrate coupling.

Complete receiver with merged LNA and Mixer

As shown in Fig. 4, a fully differential 60GHz direct conversion receiver front-end based on the transformer is fabricated in 0.13μm CMOS. Transformer T_1 couples between the two CS stages of the LNA and T_2 seamlessly

merges the outputs of the LNA with the input of the switching pairs of the Gilbert mixer. T_2 also serves as the transconductor of the Gilbert mixer, providing an extra current gain. This eliminates the headroom problem resulting from stacking two transistors followed by resistive loading. The LNA can now be designed independent of the mixer switches, allowing the flexibility to optimize for both linearity and gain.

Measurements and Results

Fig 5 shows the measured conversion gain with a peak of 23.5dB at 60GHz and a 3dB bandwidth of 3GHz. The input referred compression point measured at this peak frequency is -11dBm. The noise figure is measured by the gain method[5]. Terminating the LNA input with 50Ω terminations, the output noise density is -140dBm/Hz with the ratio of the resolution bandwidth to the video bandwidth of the spectrum analyzer set to 0.11. NF is thus measured to be -140+174-23.5=10.5dB. The fully differential receiver front-end dissipates 8.6mW from 1.2V power supply and consumes a core chip area of 0.32x0.07mm^2. Table 1 summarizes the performance and compares this front-end with recently published CMOS receivers. Fig. 6 shows the die photo.

Conclusion

In conclusion, a fully differential 60GHz direct conversion receiver front-end has been realized in 0.13µm CMOS. Using an on-chip eight-metal-layer interleaved transformer, the receiver achieves a high input 1dB compression point of -11dBm, a high gain of 24dB without a buffer amplifier, a low NF of 10.5dB, a low power consumption of 4.3mW/arm and a small chip area of 0.022mm^2. The compact transformer structure enables high gain and high linearity and low NF through increased signal headroom and optimized impedance matching. Compared with prior arts in CMOS, this receiver achieves the highest linearity, highest gain without an output buffer amplifier, smallest area, and lowest power consumption with low NF.

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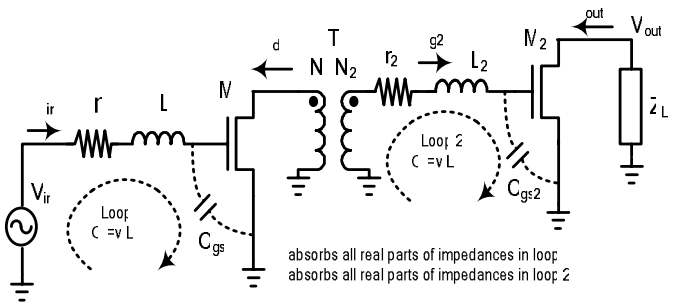


Fig. 1 Transformer coupled two-stage LNA and each stage is based on the common-source (CS) configuration

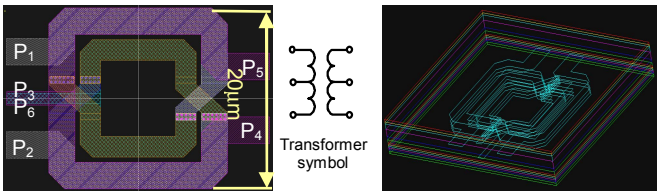


Fig. 2 Layout of interleaved multilayer on-chip transformer and 3D view

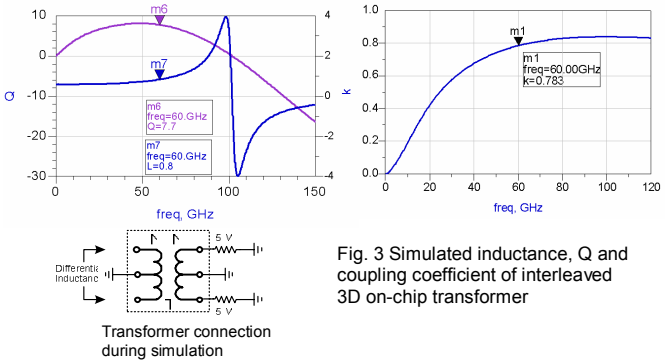
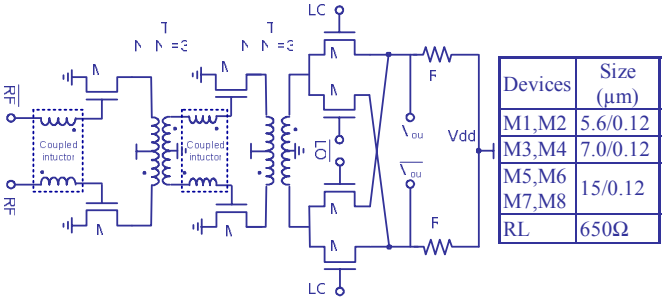


Fig. 3 Simulated inductance, Q and coupling coefficient of interleaved 3D on-chip transformer



Devices	Size (µm)
M1,M2	5.6/0.12
M3,M4	7.0/0.12
M5,M6 M7,M8	15/0.12
RL	650Ω

Fig. 4 Fully differential 60GHz CMOS Direct Conversion Receiver Front-End

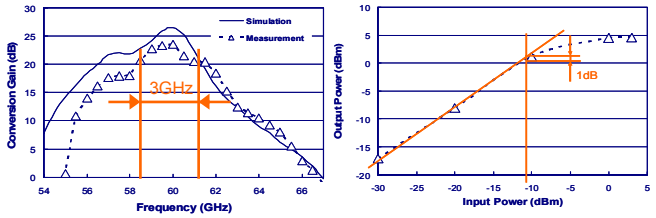


Fig. 5 Measured conversion gain and input referred compression point

Table 1 Performance summary and comparison with prior arts

	[2]	[3]	This work
Topology	Single-ended	Single-ended	Differential
Process	0.13µm CMOS	0.13µm CMOS	0.13µm CMOS
Direct conversion	Yes	No	Yes
Conv. Gain(dB)	28	8	23.5
Buffer amplifier	Yes	Yes	No
NF (dB)	12.5	-	10.5
P_{1dB} (dBm)	-22.5	-	-11
RF BW (GHz)	-	-	3
Per arm Power cons(mW)	9	-	4.3
Chip area (mm^2)	0.12	3.64	0.0224

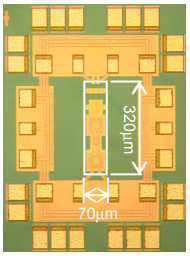


Fig. 6 Die photo