18.6 An RF/Baseband FDMA-Interconnect Transceiver for Reconfigurable Multiple Access Chip-to-Chip Communication

Jenwei Ko[1], Jongsun Kim[1], Zhiwei Xu[1], Qun Gu[1], Charles Chien[2], M. Frank Chang[1]

[1]University of California, Los Angeles, CA
[2]SST Communications, Los Angeles, CA

A scalable frequency-division multiple access interconnect (*FDMA-I*) system is proposed to enable reconfigurable and bi-directional multiple I/O chip-to-chip communications. By transmitting signals using N-orthogonal frequency channels, this *FDMA-I* achieves simultaneous multi-chip access capability between NxN I/Os on a shared bus by selectively switching various frequency bands, resulting in channel concurrency and reconfigurability.

In the past, CDMA techniques have been applied in serial links [1,2] and bus architectures [3,4] to achieve a flexible communication network. However, ISI makes it difficult to increase the data rate for these schemes. *FDMA-I*, on the other hand, can achieve the same flexible and reconfigurable I/O network with high aggregate data rate by slowing down the data rate on each of the RF carriers while increasing the number of RF carriers, resulting in smaller ISI.

To demonstrate this concept, an *FDMA-I* transceiver chip is implemented based on two-carriers, one at 7.36GHz and one at DC or baseband. This special case of *FDMA-I* is referred to as RF/baseband *FDMA-I*. Four of these chips are used to construct a 2×2 *FDMA-I* system, as shown in Fig. 18.6.1, with four RF and four baseband transceivers sharing a terminated transmission line. This RF/baseband interface enables simultaneous uni- or bi-directional signaling over a shared bus or a point-to-point link. For example, when the baseband transmitter (Tx1 of chip4) and receiver (Rx1 of chip1) are communicating with each other, the two RF-band transceivers (Tx0 of chip2 and Rx0 of chip3) occupy the same channel simultaneously by using frequency (de)modulation techniques, resulting in increased channel concurrency and reduced latency. The link between chip 1 and 4, and chip 2 and 3 may be reconfigured via software control in real-time to form a link between chip 1 and 3, and chip 2 and 4 by deactivating Rx0 in chip3 and Tx1 in chip4 and activating Rx0 in chip4 and Tx1 in chip3.

Conventional wireless RF transceiver is a narrow-band system with a data bandwidth of less than tens of MHz. In contrast, the *FDMA-I* transceiver is an ultra wide bandwidth system with a signal bandwidth of over several GHz. The challenge in designing the *FDMA-I* transceiver is to reduce the area and power overhead of the RF transceivers for each of the frequency channels, while achieving a wide signal bandwidth spanning over several GHz. To meet this challenge, the transceiver architecture is designed with a minimum number of on-chip inductors and a simple (de)modulation architecture.

Figure 18.6.2 shows the RF transmitter circuit and modulation operation. By using BPSK modulation, differential digital signals (Din/Dinb) are up-converted with an RF carrier (LO) by the mixer (M3, M4) and then transmitted into the transmission line. When Din is high/low, the mixer output is inverse/in-phase with the LO. The mixer consumes no DC power. The current-mode output driver (M5, M6) is used to drive the channel with a signal swing of a few tens of mV. Although the baseband signaling is slightly affected by the RF signal interference, it has sufficient noise margin with an output swing of a few hundreds of mV. Ultra-wide bandwidth and small area are achieved by completely eliminating inductors in the RF transmitter.

Figure 18.6.3 shows the RF-band receiver architecture. The band-pass filter amplifies the incoming RF signals and rejects the baseband signals. To compensate the RF signal distortion due to the low-pass characteristics of the channel (10-cm transmission line on FR4 PCB), the peaking frequency of the LC tank is designed to be 20% higher than the LO frequency. The I/Q mixers down-convert the bandpass signal (V_{BPF}), while the baseband interference signals are up-converted to the LO frequency and rejected by the LPFs. A frequency-locked loop (FLL) compares the envelopes of V_{I_LPF} and V_{Q_LPF} to detect and compensate for the frequency difference between the transmitter and receiver LOs. Therefore, even with a frequency discrepancy between the LOs, the original data can be demodulated correctly. To save power and area for an NxN *FDMA-I*, only the receiver with the highest carrier frequency requires the FLL while the other N-1 carriers may be generated by dividing down from the LO with the highest frequency.

Figure 18.6.4 shows the building blocks for the frequency detector (FD), charge pump (CP), and quadrature voltage controlled oscillator (QVCO) with frequency locking operation. Whenever Vcomp makes transitions, the CP will pump up or down for a short period time as controlled by the fast/slow signal, generated by sampling V_{XOR_IQ} at the Vcomp transition. Vcomp is generated by comparing the envelopes of the I/Q channel signals. The negative feedback of the FLL drives the QVCO so that its output locks onto the transmitter LO frequency at 7.36GHz.

A prototype RF/baseband *FDMA-I* transceiver chip is fabricated in a 0.18μm 1.8V CMOS technology to demonstrate simultaneous multi-chip access capability with programmable uni- or bi-directional signaling. For the baseband transceiver, conventional current-mode driver and receiver are implemented together with the RF transceiver. The test board with the two chips achieves a total data rate of 3.6Gb/s/pin over a 10-cm FR4 PCB line. The RF transceiver achieves 1.8Gb/s while dissipating 74mW (19mW for TX, 36mW for RX, and 19mW for the QVCO) and the baseband transceiver achieves 1.8Gb/s while dissipating 18mW (12mW for TX, 6mW for RX).

Figure 18.6.5 shows the measured 3.6Gb/s/pin uni-directional signaling with both the RF and baseband data rate of 1.8Gb/s. Figure 18.6.5(a) shows the input signals with 2^7-1 PRBS and the recovered data. Figure 18.6.5(b) shows the measured data eye diagram with a BER of 10^{-7} and 10^{-10} for the RF and baseband, respectively. To demonstrate the flexible bandwidth allocation, Fig.18.6.6 shows the measured simultaneous bi-directional signaling with a 2.4Gb/s/pin in baseband and a 0.6Gb/s/pin in RF-band with BERs of 10^{-9} for both. Figure 18.6.7 shows the microphotograph of the *FDMA-I* dual-transceiver chip; it occupies 0.65mm^2.

Acknowledgments:
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References:
[1] Z. Xu et al.,"A 2.7 Gb/s CDMA-Interconnect Transceiver Chip Set with Multi-Level Signal Data Recovery for Re-configurable VLSI Systems," *ISSCC Dig. Tech. Papers*, pp.82-83, Feb. 2003.
[2] M. Shiozaki et al.,"A 2Gbps and 7-Multiplexing CDMA Serial Receiver Chip for Highly Flexible Robot Control System," *Symp. VLSI Circuits*, pp.194-197, June, 2004.
[3] J. Kim et al.,"A 2-Gb/s/pin Source Synchronous CDMA Bus Interface with Simultaneous Multi-Chip Access and Reconfigurable I/O Capability," *IEEE CICC*, pp.317-320, Sept., 2003.
[4] R. Yoshimura et al.,"DS-CDMA Wired Bus with Simple Interconnection Topology for Parallel Processing System LSIs," *ISSCC Dig. Tech. Papers*, pp.370-371, Feb., 2000.

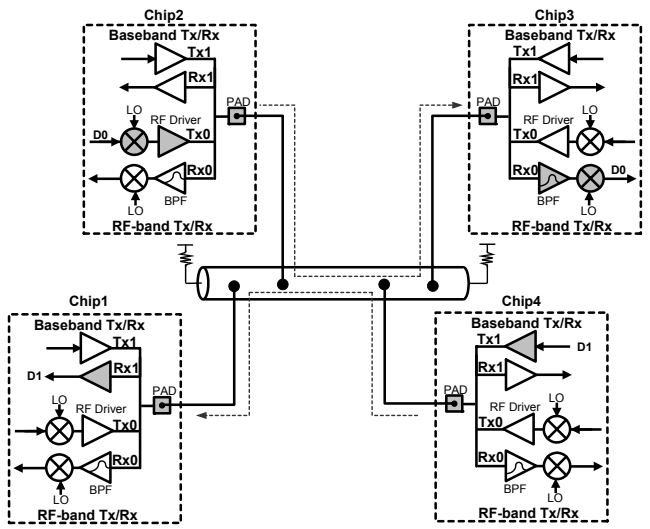

Figure 18.6.1: An RF/baseband FDMA-Interconnect system for simultaneous multiple access.

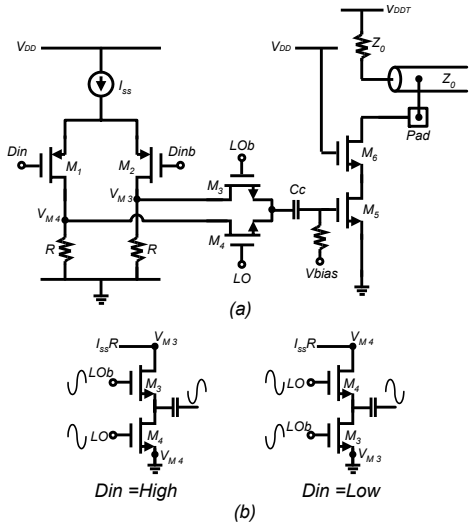

Figure 18.6.2: (a) RF-band transmitter circuit (b) Operation of BPSK modulation.

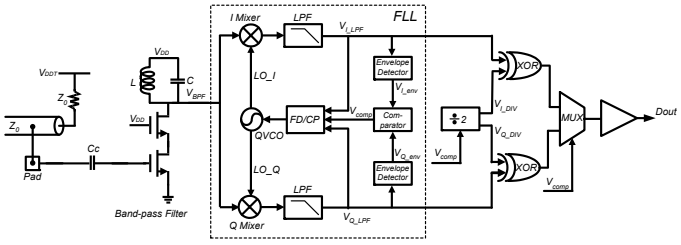

Figure 18.6.3: RF-band receiver architecture.

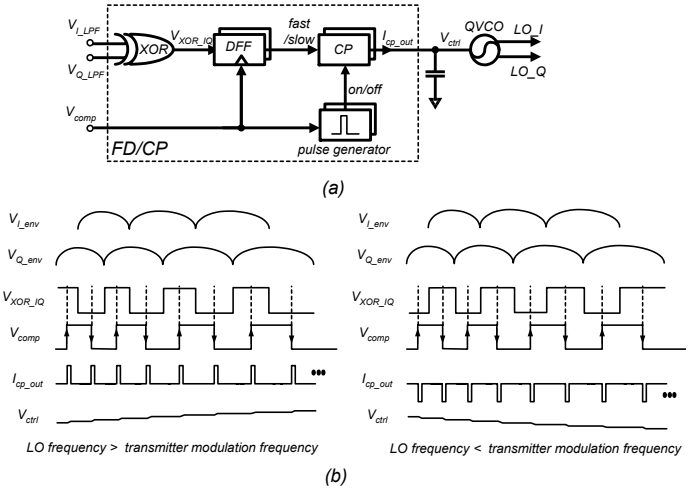

Figure 18.6.4: (a) FD and CP building blocks (b) Frequency locking operation.

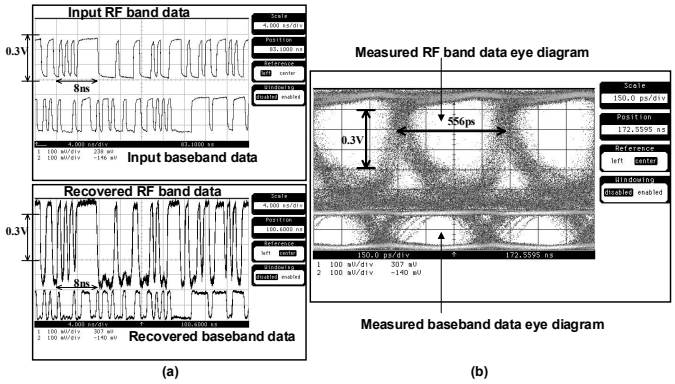

Figure 18.6.5: 3.6Gb/s/pin simultaneously uni-directional 1.8Gb/s RF and 1.8Gb/s baseband signaling (a) Input and recovered RF/baseband data (b) Measured data eye diagrams.

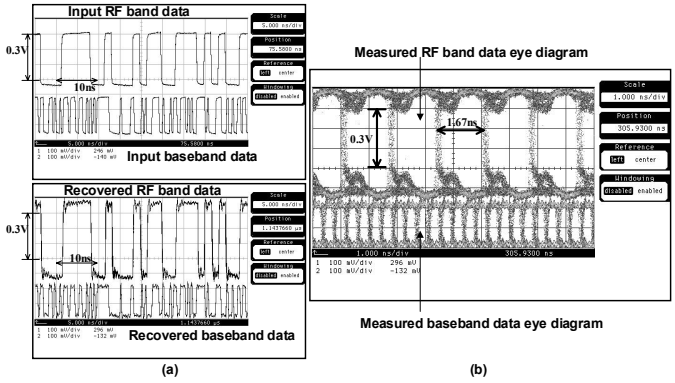

Figure 18.6.6: 3.0Gb/s/pin simultaneously bi-directional 0.6Gb/s RF and 2.4Gb/s baseband signaling (a) Input and recovered RF/baseband data (b) Measured data eye diagrams.

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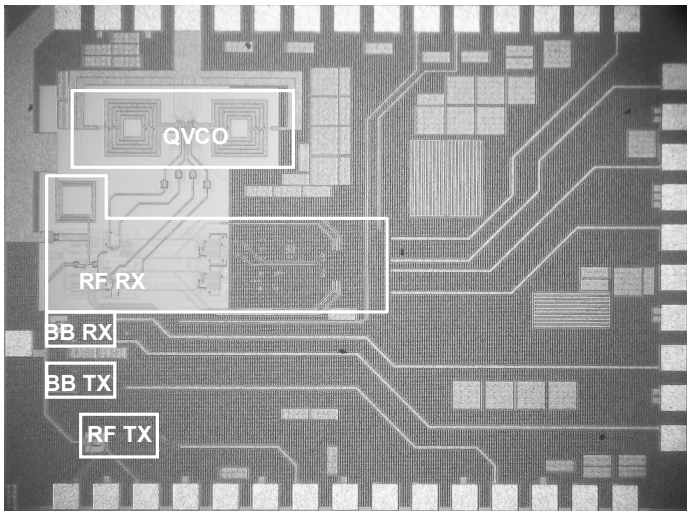

Figure 18.6.7: Chip microphotograph of FDMA-I RF/baseband dual transceiver.

