5.4 A Compact Dual-Band Direct-Conversion CMOS Transceiver for 802.11a/b/g WLAN

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Over the past several years, the WLAN market has shown more than double digit growth, dominated mostly by network interface cards and mini-PCI solutions. More recently, WLAN is beginning to penetrate into the embedded market, including applications in home entertainment, cellular phones, PDAs, and gaming. These embedded applications place stringent constraints on cost and power consumption. In this paper, a compact fully integrated 0.18μm RF CMOS transceiver is presented that meets the IEEE 802.11a/b/g WLAN requirements and covers both the 2.4-2.4835GHz and the 4.9-5.875GHz bands. The transceiver occupies 6mm^2 die area while consuming at most 182mW. Compared to previously published dual-band RF transceivers [1-3], this transceiver covers all bands specified for WLAN while achieving 50-70% smaller die area with 24-60% less power consumption.

In the past, several radio architectures have been used to realize the RF transceiver [1-4]. Although two-step zero-IF architecture [1,2] decreases the LO frequency by separating the up/down conversions into two successive steps, this scheme doubles the number of mixers, LO drivers, and frequency synthesizers. Therefore, it is difficult to use this architecture for low-power, small-die-area implementations. In contrast, direct-conversion radio architecture requires only one LO to achieve up/down conversion in one step and therefore, leads to a more compact and low-power design. Thus, the dual-band transceiver is implemented based on the direct-conversion architecture as shown in Fig. 5.4.1. To overcome the well-known impairments due to LO leakage and DC offset, an LO calibration loop and a successively switched DC offset cancellation loop have been implemented in the transceiver. The LO calibration loop reduces the amount of LO leakage to less than –29dBc while the successively switched DC offset cancellation loop improves the cancellation and has a shorter convergence time, which is critical for the 802.11a/g modes.

The transmitter shown in Fig. 5.4.1 includes separate up-conversion mixers and class AB pre-amplifiers for the 5GHz and the 2.4GHz bands, but shares a 5th-order LPF that has a variable gain with 14dB tuning range. Because of device mismatches, LO leakage exists in the transmitter output, which in the worst case could be only 15dB lower than the desired signal. To reduce the LO leakage, an on-chip LO leakage calibration circuit as shown in Fig. 5.4.2 is implemented in the transmitter to guarantee at least –29dBc LO leakage with at most ±3dBc change on the image tone.

The transmitter delivers 2.5dBm/1dBm output power with 20dBm/23dBm OIP3 for 2.4GHz/5GHz band while meeting the ACPR requirements for 802.11a/g with EVM of –31dB/–32dB. The output power flatness across 4.9GHz~5.8GHz is 4.5dB and with a variation of 3.5dB when temperature changes from 0 to 85°C. The TX output power can be further increased to 8.5dBm/6dBm for the 2.4GHz/5GHz band with the same power consumption but with a higher EVM of –28dB/–29dB.

The receiver shown in Fig. 5.4.1 consists of a shared baseband circuit and separate RF front-ends for the 5GHz band and the 2.4GHz band. The differential LNA in both bands has four different gain settings. As shown in Fig. 5.4.3, the LNA is followed by a PMOS down-conversion mixer circuit, which converts the RF signal directly into baseband signal. PMOS switching transistor is used in the mixer for low flicker noise performance. A differential inductor with a Q of 11 is used as the load for the LNA that also resonates with the parasitic capacitances at the mixer input to reduce the noise contribution from the switch transistors. Since the LNA load impedance is largely determined by the average on-resistance of the switching transistors in the mixer, the front-end can obtain wide flat gain range across the 4.9GHz~5.9GHz band. This implementation avoids high-frequency buffer between the LNA and mixer, which realizes a low-power front-end. Differential inductors also aid in producing a compact design. Both RF front-ends in 5GHz band and 2.4GHz band have greater than 30dB gain with 1.4dB gain flatness. The total receive-chain NF is 4.9dB/5dB and the IIP3 of the receive RF front-end is –7.3dBm/–8dBm (10dBm/14.5dBm) the 2.4GHz/5GHz band in high (low) gain setting. In addition, with local DC offset cancellation circuit, this front-end achieves greater than 40dBm IIP2.

The shared receiver baseband circuit consists of VGAs interleaved with filter stages. The VGAs provide 64dB gain range with 1dB gain step. The filter stages implement a 5th-order LPFs with a local bandwidth calibration loop to provide a stable bandwidth over process and temperature variations. The bandwidth can be set in 0.15MHz steps. A DC offset cancellation circuit shown in Fig. 5.4.1 is used to reduce the dc offset due to device mismatches. The DC offset cancellation circuit behaves as a HPF with a low corner frequency during normal operation. In this case, it can not track fast changes in the offset voltage, especially when the VGA gain is being adjusted during the preamble portion of the packet. To provide fast tracking, the DC offset loop bandwidth is widened while the VGA gain is being adjusted and narrowed when the gain is stabilized. However, abrupt bandwidth switch of the DC offset cancellation circuit will introduce a large DC offset transient. To reduce this transient, as shown in Fig, 5.4.4, a successive switching technique is implemented to gradually decrease the bandwidth from 1MHz to 10kHz in three discrete steps. Simulation shows a 15dB improvement in offset transient as compared to abrupt switching of the bandwidth.

The frequency synthesizer typically consumes nearly half of the power in the transceiver and therefore must be optimized. Rather than choosing to double the VCO frequency as in [3] and dissipate excessive power, an offset VCO architecture as in [4] is implemented to reduce the VCO frequency to 1.5× that of the LO frequency. The synthesizer shown in Fig. 5.4.1 employs a charge-pump PLL using 20MHz/40MHz as a reference. The VCO achieves a 25% tuning range running between 3.1GHz and 4.0GHz with a digitally controlled capacitor tank to decrease the K_{vco} below 100MHz/V. The VCO outputs are divided by a divide-by-2 circuit and mixed up to form the 4.9-5.88GHz LO signal. To form the 2.4GHz LO signals, the 5GHz LO is divided down by two as shown in Fig. 5.4.1.

The VCO core uses a cross-coupled NMOS differential pair loaded with a differential LC tank, which is biased through a PMOS current source. To avoid the unnecessary noise contribution from the NMOS differential pair when the VCO output swing is too large, a digital amplitude control loop is used to detect and maintain the optimum output swing of the VCO. The amplitude control loop is also used in LO buffers that drive the RX down-conversion mixer and TX up-conversion mixer to save unnecessary power consumption due to overdrive. The amplitude control loop can save up to 15% power consumption in VCO and LO buffers and also improve phase noise by avoiding overdrive. The frequency synthesizer and VCO draw 26mA and 4.5mA from a 1.8V supply, respectively. Figure 5.4.5 shows the measured carrier phase noise of –100dBc/Hz at 100kHz offset for 5.6GHz and 2.44GHz LO frequencies. Figure 5.4.6 summarizes the measured transceiver performance and Fig. 5.4.7 shows the die photo.

References:

[1] M. Zargari et al. "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN," *ISSCC Dig. Tech. Papers*, pp. 96-97, Feb., 2004.
[2] Rami Ahola et. al. "A Single Chip CMOS Transceiver for 802.11 a/b/g WLANs," *ISSCC Dig. Tech. Papers,* pp. 92-93, Feb., 2004.
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[4] A. Behzad et. al. "A 4.92-5.845GHz Direct-Conversion CMOS Transceiver for IEEE 802.11a Wireless LAN," *RFIC Symposium Dig. of Papers*, pp. 335-338, June, 2004.

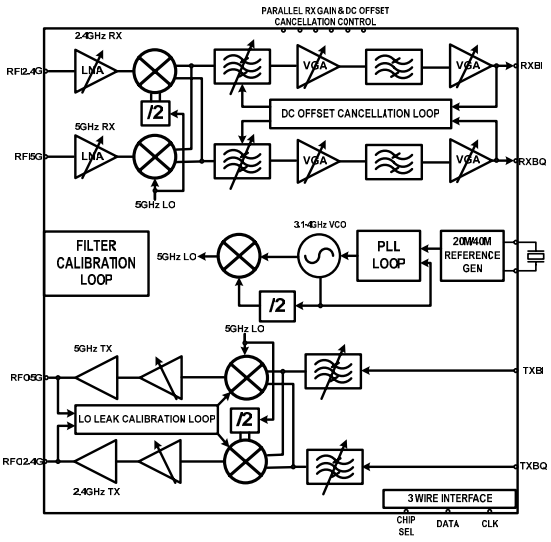

Figure 5.4.1: Transceiver block diagram.

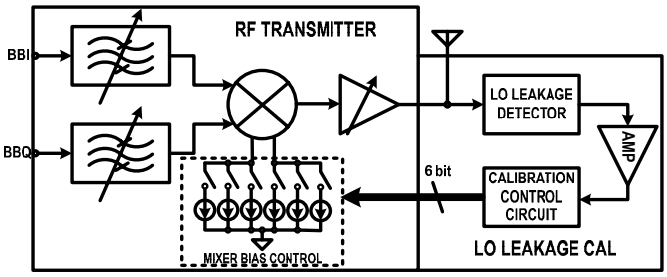

Figure 5.4.2: LO Leakage Calibration Circuit in the Transmitter

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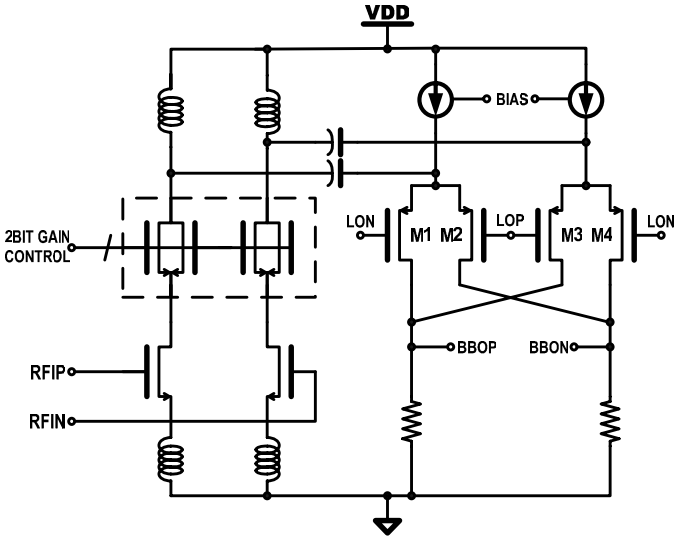

Figure 5.4.3: Receiver RF front-end schematic.

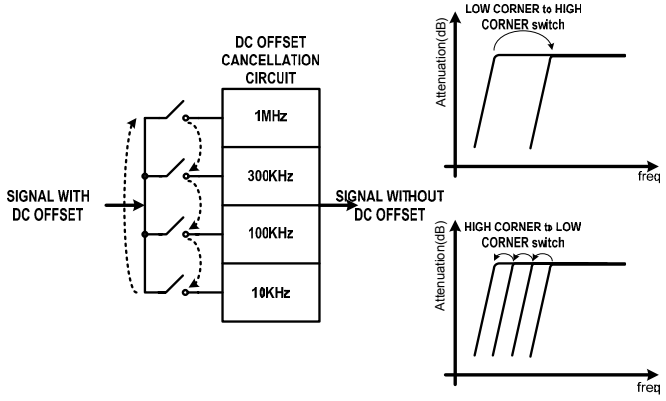

Figure 5.4.4: Successive switching technique in DC offset cancellation.

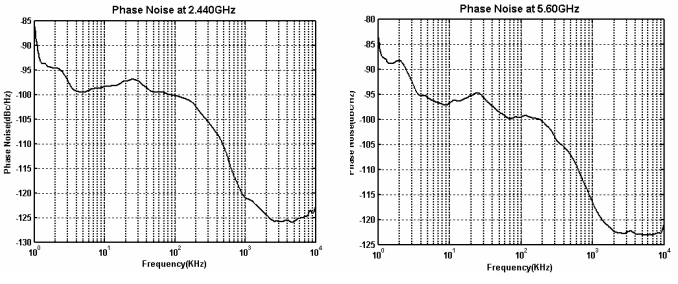

Figure 5.4.5: Measured carrier phase Noise from TX output.

Parameter	Results for 2.4GHz Band	Results for 5GHz Band
Technology	TSMC 0.18μm CMOS	
Die Size	6mm²(2.4mmx2.5mm)	
Supply	1.8V±10%	
RX Power Consumption	68mA	64mA
TX Power Consumption	76mA @ 2.5dBm output power	101mA @ 1dBm output power
RX Dynamic Range	90dB	92dB
RX Noise Figure	4.9dB	5.0dB
RX IIP3 (max front-end gain)	-7.3dBm	-8dBm
RX IIP3 (min front-end gain)	10dBm	14.5dBm
RX EVM	-32dB	-31.4dB
TX OIP3	20dBm	23dBm
TX EVM	-31dB @ 2.5dBm output power	-32dB @ 1dBm output power

Figure 5.4.6: Chip performance summary.

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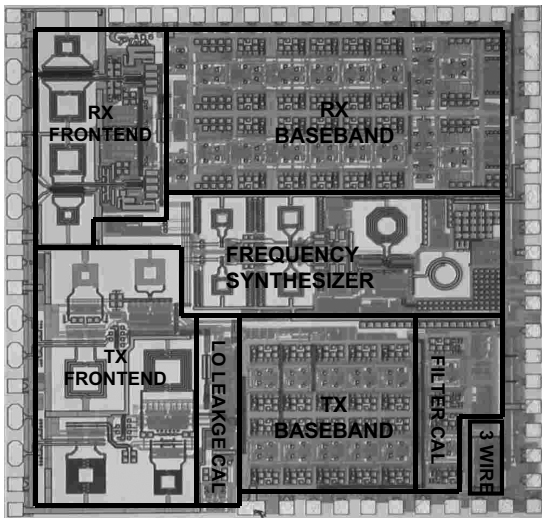

Figure 5.4.7: Die micrograph.

