Three-Dimensional Circuit Integration Based on Self-Synchronized RF-Interconnect Using Capacitive Coupling

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Abstract

A self-synchronized RF-interconnect (SSRFI), based on capacitive coupling and peak signal detection, is presented. In this SSRFI, small coupling capacitor (60fF) is used to interconnect vertical active layers in 3-Dimensional IC. The demonstrated SSRFI system, including both transmitter and receiver, has been designed, fabricated and verified in UMC 0.18μm CMOS with a PRBS data rate of 3Gbit/s, a BER of $1.2x10^{-10}$ and a rms jitter of 1.28ps. The core circuit burns 4mW from a 1.8V supply and occupies $0.02mm^2$ chip area.

1. Introduction

With the dramatic development in semiconductor technology and circuit design, more sophisticated systems have been implemented on a single chip. While the expanding market keeps pushing for the higher speed, lower power, more powerful and cheaper single chip systems, it actually becomes harder and harder for using conventional planar technology to design multi-function and low-cost chip systems with more parasitic interconnect effects in deep sub-micron technologies, such as high parasitic capacitance, short-channel effect and strong cross talk between wires [1]. Furthermore, conventional planar technology also faces fundamental physical limits in scaling down interconnect dimensions and will encounter more significant interconnect issues in the near future. All of these heavily impact the next generation IC development. 3-Dimensional IC (3D IC) has been proposed to overcome above drawbacks to allow the stacking of active device layers or chips. With this alternative, the 3D ICs will surpass traditional 2D ICs in reducing chip area, power consumption, timing constraints and even cost [2]. Therefore, 3D IC has gradually become a mainstream approach in future IC development.

In 3D IC, several key obstacles must be solved, one of which is to interconnect multiple device layers effectively. Generally, vertical connections are formed by etching vias through layers and depositing metal studs to physically connect active device layers (Fig. 1)[3]. This conventional method, however, becomes less manufacturable when the total number of vertical active layers becomes large, leading to increased etching depth and vertical line parasitics [4]. In order to overcome the above drawbacks, a self-synchronized RF Interconnect (SSRFI) is presented in this paper as shown in Fig. 2.

Unlike the traditional via/stud interconnects, the proposed SSRFI is based on the capacitive coupling and peak signal detection. Since the coupling is accomplished through capacitors, there is no need of fabricating vias and studs and would not consume any DC power along the transmission line.

However, the previous RFI [5] requires the transmitter to upconvert baseband signal with the RF carrier before sending it to the channel through the coupling capacitor; and the receiver to downconvert the signal with the same RF carrier to recover the baseband signal. [6] Although it enables the data transmission/receiving successfully and improves the transmission efficiency, the previous RFI still has some constraints. First, both transmitter and receiver demand precise LO carriers for signal modulation and demodulation, which increases the design complexity and manufacturing cost. Second, the LO carriers at both Tx/Rx sides must be synchronized, which requires matching crystal and power-hungry oscillation circuits.

2. System Architecture and Circuit Design

In this paper, a novel SSRFI architecture with smaller chip area and less power dissipation has been realized to overcome the above drawbacks. Instead of using LO for demodulation in the receiver, a peak signal detection circuitry is used to recover the baseband signal without using any additional synchronization scheme, which simplifies the circuit design and relaxes the need to generate precise frequency from a receiver synthesizer.

This SSRFI circuit architecture is shown in Fig. 3, in which the transmitter (Tx) includes an input buffer and ASK modulator blocks and the receiver (Rx) consists of peak signal detector and output buffer. This SSRFI system is fabricated in UMC 0.18μm CMOS technology.

A. Transmitter

Since the amplitude of the baseband signal is generally small, an input buffer of Tx, shown in Fig. 4, is used to amplify and regenerate the baseband signal with sufficient gain to drive the subsequent ASK generator and isolate the input noise from the output signal. Therefore, the sizes of M1-M6 devices must be chosen carefully to satisfy the above function requirements.

Owing to the high pass characteristic of capacitor coupling, baseband signal should be upconverted with LO at high frequencies to pass through the coupling capacitor. ASK modulation was chosen for its simplicity and efficiency. The ASK signal is generated by switching on and off the LO carrier, as shown in Fig. 5. When the baseband signal is high, the LO carrier passes through, otherwise the LO is blocked.

B. Receiver

The ASK signal, after passing through the channel, is recovered in the Rx by using a peak signal detector, in which both PMOS and NMOS are used as diodes so that logic "1" and logic "0" can be efficiently passed without a threshold loss, as shown in Fig. 6. An Output Buffer following the peak signal detector is used to rectify signals and drives the off-chip load.

C. Jitter Performance

The SSRFI system reduces the jitter by several methods. First, the self-synchronization structure removes the extra synthesizer circuits in Rx, which dramatically reduces the jitter generation by the system. Second, due to their low frequency nature, jitters transferred from the digital switching noise and flick noise are suppressed by the high pass SSRFI system [7]. Third, the latch structures in both input and output buffers serve as noise discriminators, which further increases the jitter tolerance ability of the system. Therefore, by reducing jitter generation, improving jitter transfer and jitter tolerance, this open loop SSRFI circuit, without systematic jitter accumulation, has better jitter performance than traditional close loop data recovery circuits. The measured rms. value of the output signal jitter is 1.28ps at 3Gb/s.

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3. Measurement Results

The prototype SSRFI chip has been fabricated in UMC 0.18μm CMOS technology. The chip photo is shown in Fig. 7. The 3Gb/s 500mvpp differential PRBS (Pseudo Random Binary Sequence) signals from Agilent 71612 pattern generator are the chip inputs. The LO is set at 10GHz and with amplitude of 900mvpp. Fig. 8 shows the eye diagram of the output signal. The eye height is about 220mv rms, and the width is 257ps rms approximately. Fig. 9 shows the output signal jitter measurement result. The measured BER (Bit Error Rate) is $1.2x10^{-10}$.

4. Conclusion

A self-synchronized RF-interconnect technology (SSRFI), based on capacitive coupling and peak signal detection, has been successfully demonstrated in 0.18μm CMOS. This SSRFI can be used effectively for vertical interconnects in future 3D IC with a small coupling capacitor of 60fF ($8x8\mu m^2$). The SSRFI circuit is measured with transmission/receiving PRBS data rate of 3Gbit/s and a BER of $1.2x10^{-10}$ and consuming 4mW from a 1.8V supply. The rms jitter value of output signal is measured as 1.28ps. The combined Tx/Rx occupies $0.02mm^2$ in chip area.

Acknowledgement

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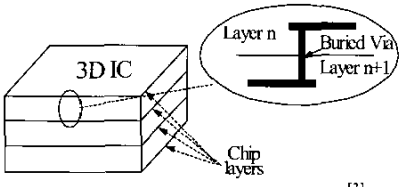

Fig. 1 Buried via interconnect method [3]

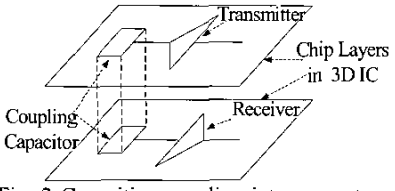

Fig. 2 Capacitive coupling interconnect scheme

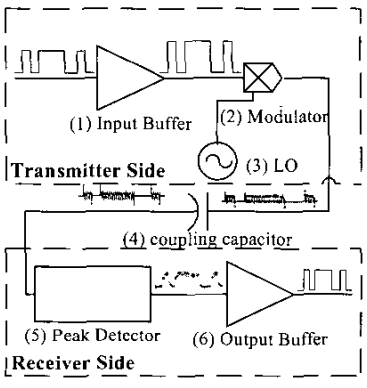

Fig. 3 SSRFI circuit architecture

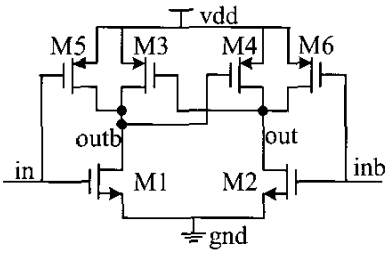

Fig. 4 Input Buffer structure

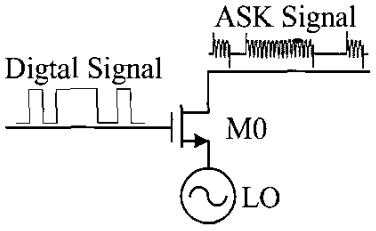

Fig. 5 ASK modulation circuit

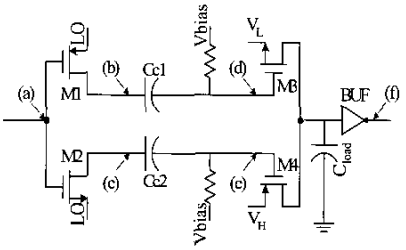

Fig. 6 Peak signal detection circuit

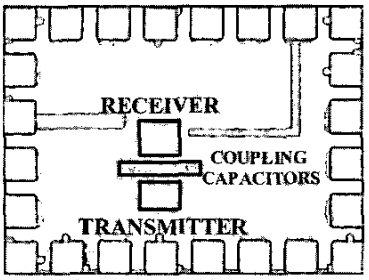

Fig. 7 SSRFI circuit chip photo

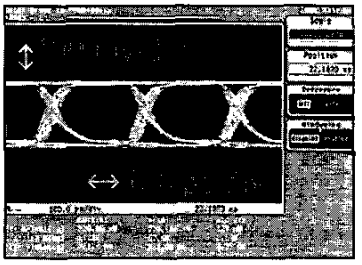

Fig. 8 The widely opened eye diagram of output signal at 3Gb/s

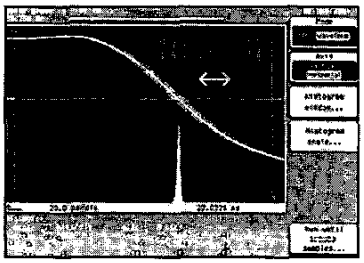

Fig. 9 Jitter Measurements for 3Gb/s PRBS (<1.28ps)