A SELF-SYNCHRONIZED RF-INTERCONNECT FOR 3-DIMENSIONAL INTEGRATED CIRCUITS

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ABSTRACT

A self-synchronized RF-interconnect technology (SSRFI), based on capacitor coupling and peak signal detection, is presented in this paper. It can be easily implemented in 3-Dimensional ICs (3D-ICs) with small coupling capacitors (60fF) to interconnect vertical active layers. The demonstrated SSRFI system, including both transmitter and receiver, has been designed, fabricated and verified in UMC 0.18μm CMOS with a verified PRBS (Pseudo Random Binary Sequence) data rate of 3Gbit/s and a BER (Bit Error Rate) of $1.2x10^{-10}$. The core circuit burns about 4mW from a 1.8V supply and occupies $0.02mm^2$ chip area.

1. INTRODUCTION

With the dramatic developments in semiconductor technology and circuit design, more sophisticated systems have been implemented on a single chip. While the expanding market keeps pushing for the requirements for the higher speed, lower power, more powerful and cheaper single chip systems, it is actually becoming harder and harder for conventional planar technology to design multi function and low cost chip systems with the more parasitic interconnect effect in deep sub-micron technologies, such as high parasitic capacitance, short-channel effect and strong cross talk between wires [1]. Furthermore, conventional planar technology also faces fundamental physical limits and will encounter more significant interconnect issues in the future. All these have huge impacts on the next generation IC development. 3-Dimensional IC (3D IC) has been proposed to overcome above drawbacks to allow the stacking of active device layers or chips. With this alternative, the 3D ICs will surpass traditional 2D ICs in reducing chip area, power consumption, timing constraints and even cost [2]. Therefore, 3D IC has gradually become a mainstream in future IC development.

In 3D IC, several key obstacles must be solved, one of which is to interconnect multiple device layers effectively. Generally, vertical connections are formed by etching vias through layers and depositing metal studs to physically connect active device layers (Fig. 1)[3]. This conventional method, however, becomes less manufacturable when the total number of vertical active layers becomes large, leading to increased etching depth and vertical line parasitics [4]. In order to overcome the above drawbacks, a self-synchronized RF Interconnect (SSRFI) is presented in this paper as shown in figure 2.

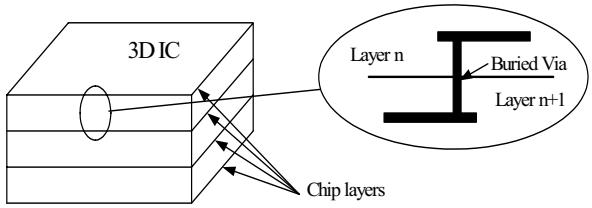

Figure 1: Buried via interconnect method [3]

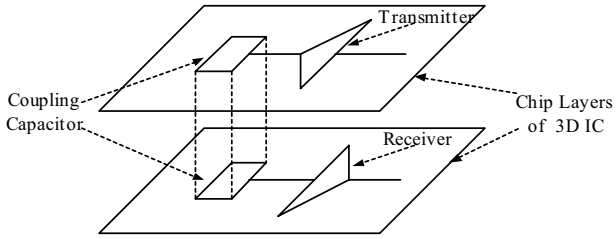

Figure 2: Capacitor coupling interconnect method

Unlike the traditional via/stud interconnect, the proposed SSRFI is based on capacitor coupling and peak signal detection. Since the coupling is accomplished through capacitors, there is no need of fabricating vias and studs and would consume no DC power along the transmission line.

For many decades, RF/Microwave signals have been transmitted through either free space or guided mediums for data/signal communication. In free space, the efficient transmission and receiving of RF/Microwave signals require the antenna size to be comparable with the signal wavelength, which is too large to be implemented in ULSI [5]. When transmitting RF/microwave signals through a guided medium, the conventional method is to use a direct coupled interconnect (DCI) over a matched transmission line as shown in figure 3(a), which typically keeps high signaling level (0.8v swing plus dc 0.8-1.2v at the terminations) and high output driver current (30mA/pin) to secure sufficient noise margin. In addition, DCIs

consume significant dc power during the data transmission because of the use of direct coupling. All these constraints have limited the application of DCI for ULSI interconnects [6].

Capacitive coupled interconnect (CCI), as shown in figure 3(b), has been used in high data rate back planes communication. Although it has no dc interaction between I/Os, CCI has limited data transmission efficiency because it requires extra data encoding/decoding. All of these constraints imposed by DCIs and CCIs could be solved by using a previously proposed RFI for efficient clock distribution or signal/data transmission [6].

However, the previous RFI requires the transmitter to upconvert baseband signal with the RF carrier before sending it to the channel through the coupling capacitor and the receiver to downconvert the signal with the same RF carrier to recover the baseband signal as shown in Fig. 3(c). Although it enables the data transmission/receiving successfully and improves the transmission efficiency, the previous RFI still has some constraints. First, both transmitter and receiver demand precise LO carriers for signal modulation and demodulation, which increases the design complexity and manufacturing cost. Second, the LO carriers at both sides must be synchronized, which requires better crystal and oscillation circuits.

2. SYSTEM ARCHITECTURE AND CIRCUIT DESIGN

In this paper, an improved SSRFI architecture with smaller chip area and less power dissipation has been realized to overcome the above drawbacks. Instead of using LO for demodulation in receiver, a peak signal detection circuitry is used to recover the baseband signal without using extra synchronization scheme, which simplifies the circuit design and relaxes the need to generate precise frequency from a receiver synthesizer. In this architecture, the two transformation blocks shown in figure 3(c) are an ASK (Amplitude Shift Keying) Modulator and a Peak Detector. The Modulator in the transmitter side is to generate ASK signal before sending it out. The Peak Detector in the receiver side is to recover the received ASK signal back to the original baseband signal.

This SSRFI circuit architecture is shown in figure 4, in which the transmitter includes input buffer and ASK modulator blocks and the receiver consists of Peak Detector and output buffer. This SSRFI system is fabricated in UMC 0.18μm CMOS technology with measured transmission/receiving PRBS signal up to 3Gbit/s and consumes only 4mW from a 1.8V supply.

Since the amplitude of baseband signal is generally small, an input buffer block, shown in figure 5, is used to amplify signal with sufficient gain to drive the subsequent ASK generator. Owing to the high pass characteristic of capacitor coupling, baseband signal should be upconverted with LO at high frequencies to pass through the coupling capacitor. ASK modulation was chosen for its simplicity and efficiency. The ASK signal is generated by switching on and off the LO carrier, as shown in figure 6. When the baseband signal is high, the LO carrier goes through, otherwise the LO is blocked.

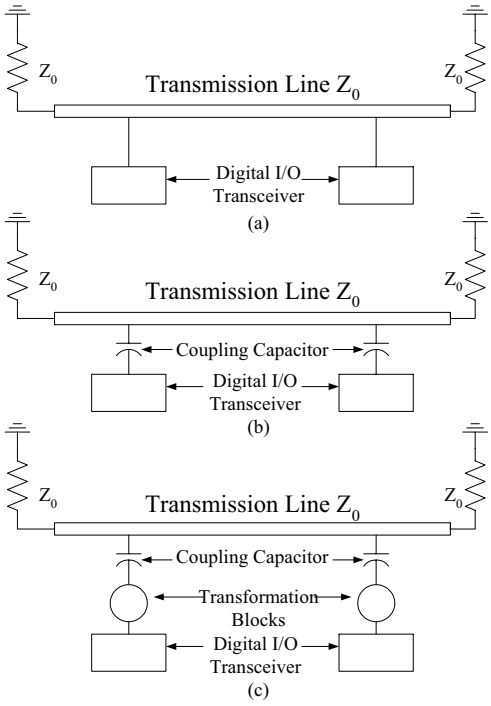

Figure 3: High speed digital interconnect architecture: (a) Direct-Coupled Interconnect (DCI), (b) Capacitive-Coupled Interconnect (CCI), (c) RF-Interconnect (RFI)[6]

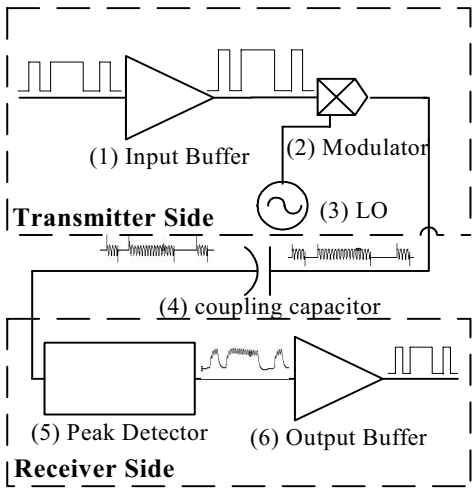

Figure 4: SSRFI circuit architecture

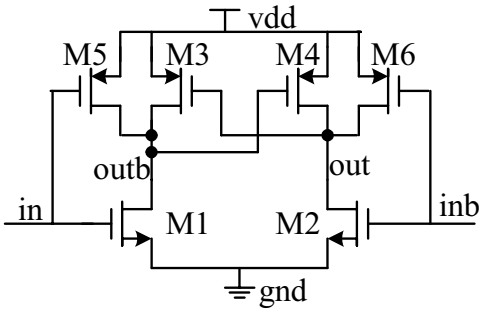

Figure 5: Input Buffer structure

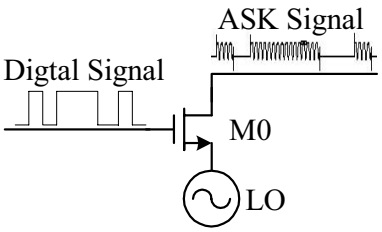

Figure 6: ASK modulation implementation

The ASK signal, after passing through the channel, is recovered in the receiver by using a simple peak detector, which is to use a diode in serial with a capacitor as shown in figure 7. When input signal is high, the diode is forward-biased to charge the capacitor. After reaching the peak of the input signal, the diode becomes reverse-biased to be turned off so that the capacitor maintains the peak value of the input signal. On the other hand, when input signal is low, the switch is turned on to discharge the capacitor [7]. As this process continues, the original baseband signal can be recovered by using peak signal detection. Since the signal is still accompanied with some noise due to current leakage in-and-out of the capacitor, it must be rectified by the subsequent output buffer circuitry to become clear digital signal. The output buffer is also designed to drive the off-chip load.

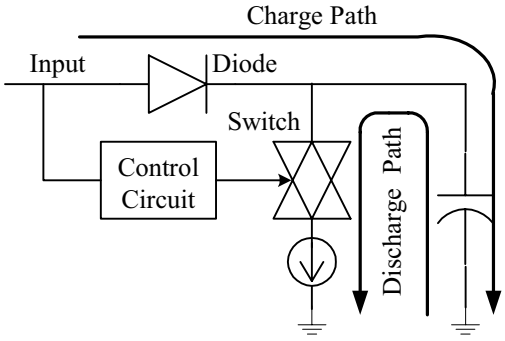

Figure 7: Peak signal detection scheme

To save the chip area, the coupling capacitor must be designed small by using higher carrier frequency for efficient signal modulation. In reality, the carrier frequency is limited by the f_T of CMOS devices. As a rule of thumb, the highest LO frequency can be reached up to about 50% of f_T. The simulated f_T's of PMOS and NMOS are 20GHz and 50GHz, respectively, in 0.18μm CMOS technology. It implies that the highest LO frequency can be reached is 25GHz for the NMOS-only circuit. But NMOS-only circuit comes with two drawbacks. First, it is hard to generate reliable loading with polysilicon resistors with high variation in resistance due to process inconsistency. In addition, the resistor load consumes high static power. On the other hand, if an NMOS load is used, the signal headroom will be significantly reduced and most importantly, the f_T of the cascaded NMOS circuit goes down dramatically with the increased V_{sb} (voltage between source and bulk). Table 1 shows the simulated f_T of cascaded NMOS changes with the V_{sb}. In order to avoid the above constraints, CMOS circuit structure has been chosen to implement the whole SSRFI interconnect system. The LO carrier frequency is designed at 10GHz by using a small coupling capacitor of 60fF (area of $8x8\mu m^2$ in this specific process).

Table 1: f_T of NMOS changes with the $V_{sb.}$

Vsb (v)	0	0.4	0.5	0.6
f_T (GHz)	49.1	29.4	20.8	8

3. MEASUREMENT RESULTS

The prototype chip has been fabricated by using UMC 0.18μm CMOS technology. The chip photo is shown in figure 8. The 3Gb/s 500mvpp PRBS signal from Agilent 71612 pattern generator goes through a broadband balun to generate differential input signals to the chip. The LO is set at 10GHz and with amplitude of 900mvpp. Both the input and output baseband signals are fed into an HP54750 digitizing oscilloscope to be monitored simultaneously. Figure 9 shows the input versus output signal waveforms. Due to the low-pass cable loss in testing, the displayed input digital signal has been attenuated above the 1.5GHz. Figure 10 shows the eye diagram of the output signal. The eye height is about 220mv rms, and width is 257ps rms approximately. The measured BER of the receiving signal is $1.2x10^{-10}$.

4. CONCLUSION

A self-synchronized RF-interconnect technology (SSRFI), based on capacitor coupling and peak signal detection, has been successfully demonstrated in 0.18μm CMOS. This SSRFI can be used effectively for vertical interconnects in future 3D IC and also for chip-to-chip

communication between conventional 2D ICs. The SSRFI circuit is tested with transmission/receiving PRBS (Pseudo Random Binary Sequence) data rate of 3Gbit/s and $1.2x10^{-10}$ BER and consuming 4mW from a 1.8V supply. The combined Tx/Rx occupies $0.02mm^2$ in chip area.

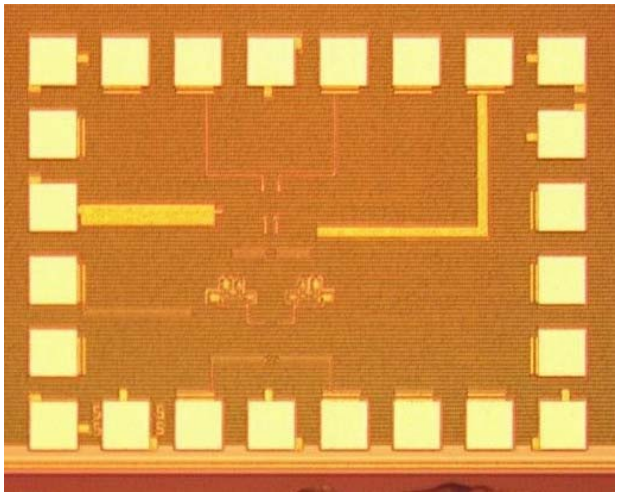

Figure 8: SSRFI chip photo

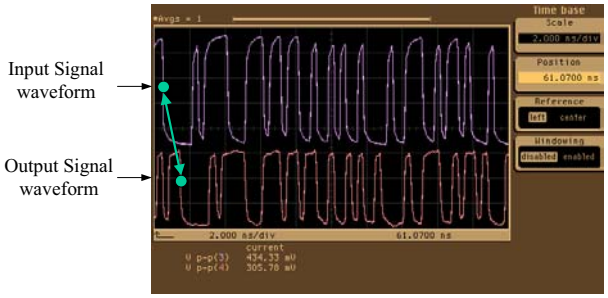

Figure 9: Input versus output signal waveform at 3Gb/s

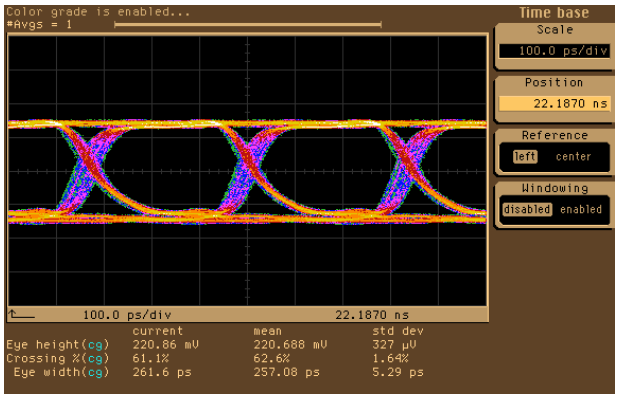

Figure 10: The eye diagram of output signal at 3Gb/s

5. ACKNOWLEDGEMENT

The authors are grateful to the contract support of US DARPA and MARCO IFC and the Foundry fabrication of UMC.

6. REFERENCE

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