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# Surface depletion thickness of p-doped silicon nanowires grown using metal-catalysed chemical vapour deposition

**I Kimukin**[1], **M Saif Islam**[1] **and R Stanley Williams**[2]

[1] Electrical and Computer Engineering, University of California Davis, Davis, CA 95616, USA
[2] Quantum Science Research, Hewlett-Packard Laboratories, Palo Alto, CA 94304, USA

E-mail: saif@ece.ucdavis.edu

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**Abstract**
An accurate evaluation of the radial dopant profile in a nanowire is crucial for designing future nanoscale devices synthesized using bottom-up techniques. We developed a very slow wet chemical etchant for gradually reducing the diameters of metal-catalysed, boron-doped silicon nanowires with varying diameters and lengths. Particular care has been taken to perform the experiment at room temperature to prevent dopant segregation, which is common in high temperature processes. By ensuring identical surface conditions subsequent to diameter reduction, the resistance of the nanowires was measured and, as anticipated, was found to increase with decreasing diameter. As the diameters were shrunk using wet-chemical etching, nanowires exhibited a non-linear increase of the resistance when the diameter was reduced to ∼50 nm. This is an indication of near-complete depletion in the nanowires caused by nanowire surface charges. The dopant concentration of the nanowires was found to be $2.1 \times 10^{18}$ cm$^{-3}$ and the corresponding surface charge density was around $2.6 \times 10^{12}$ cm$^{-2}$.

(Some figures in this article are in colour only in the electronic version)

Semiconductor and metallic nanostructures have gained tremendous attention because of their possible applications in photonics, sensing, and further miniaturization of electronic devices [1–6]. With their high surface to volume ratio, nanowires are used for sensing biological and chemical agents in solutions and atmosphere [7–11]. Silicon nanodevices are especially good candidates for biological applications due to easy fabrication and being friendly to living organisms [12]. Surface properties of the nanowires play a very important role in the electrical properties of devices such as field-effect sensors or transistors. The variation of either the resistance or capacitance of the sensor is measured; both properties are directly related to the surface charges. Therefore, it is important to know the surface charges and the resulting depletion layer thickness of field effect devices, such as MOSFETs and sensors for optimal operation. Although surface potential and the depletion layer thickness of wafers can be measured by surface voltage characterization techniques such as Kelvin probe measurements [13], these techniques are very hard or impossible to use in nanowires because of their small size and cylindrical shape.

Electrical and optical properties of nanowires are usually measured by making contacts to nanowires placed on an insulating substrate, which is usually an oxidized silicon wafer. However, for an accurate measurement of conductivity, the nanowires need to be free from contact with any object and to be surrounded by nonconductive material to eliminate possible artifacts due to current paths other than those through the nanowire itself [9]. In this work, we used our previously reported method of growing suspended nanowires between

  

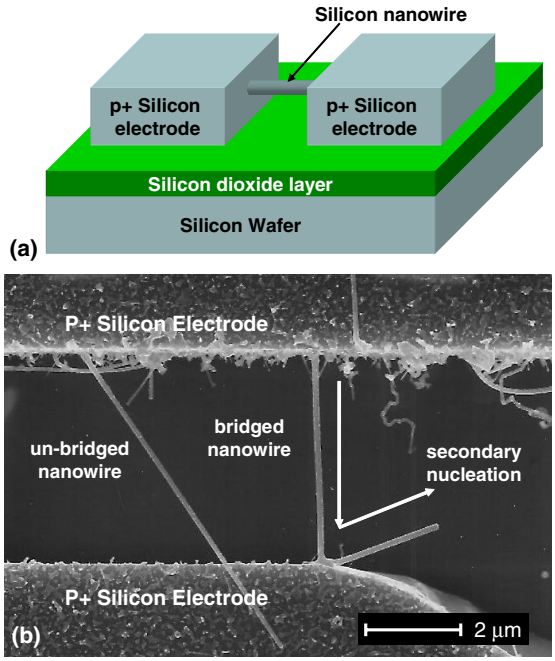


**Figure 1.** (a) Three-dimensional schematic diagram of device with a nanowire bridge. (b) SEM image of device 6 from the top of the electrodes.

two, electrically isolated, prefabricated silicon electrodes to avoid interaction of the surface of the nanowires with the surroundings [14, 15]. The electrodes were fabricated on an SOI silicon wafer with an 8 $\mu$m thick device layer and 150 nm thick buried oxide layers. The SOI wafer was oxidized to form a thin oxide layer on the surface, which is used as a mask during the anisotropic KOH etch. Optical lithography was used to define the electrodes on the wafer. The pattern was transferred onto the oxide layer with reactive ion etching using $CHF_3$ and Ar gases. The device layer of the SOI wafer was etched using a KOH-based solution (44% KOH:$H_2O$ (1:1 by volume) at 110 °C). When the edges of the electrodes are aligned perpendicular to the $\langle 111 \rangle$ planes of the substrate, the sample is etched much faster vertically than in the lateral direction. The sample is etched down to the buried oxide layer; gaps with sidewalls having vertical (111) surfaces are formed between the electrodes. The spacing between electrodes (and therefore the length of the subsequently grown nanowires) was varied between 2 and 10 $\mu$m.

After fabricating the electrodes, a ∼1 nm thick gold layer was deposited on one of the sidewalls of the electrodes. This layer acted as the catalyst for the growth of silicon nanowires. The sample was initially heated in a chemical vapour deposition chamber in a hydrogen rich environment to form Si/Au alloy nanoparticles. These nanoparticles acted as a catalyst for the growth of nanowires. Then the temperature was set to 640 °C for the growth of nanowires. $SiH_4$, HCl and diborane ($B_2H_6$) gases were introduced into the chamber. While $SiH_4$ was used for the growth of nanowires, $B_2H_6$ was used for p-type doping. HCl ensures uniformity in the diameter of the nanowires by suppressing the uncatalysed growth on the sides of the nanowires [16]. The nanowire grows across the gap toward the (111)-oriented side wall of the opposing electrode.

**Table 1.** The dimensions of nanowires grown on the devices measured.

| | Diameter (nm) | | |
|---|---|---|---|
| Device name | At root | At tip | Length ($\mu$m) |
| 1 (6E) | 123 | 89 | 6.96 |
| 2 (6G) | 118 | 102 | 6.11 |
| | 125 | 103 | 6.26 |
| 3 (4B) | 120 | 109 | 4.48 |
| | 127 | 110 | 4.44 |
| | 117 | 113 | 4.43 |
| | 104 | 85 | 4.74 |
| 4 (4D) | 130 | 124 | 4.52 |
| 5 (6B) | 139 | 134 | 6.97 |
| 6 (4C) | 161 | 161 | 4.44 |

When the nanowire reaches the opposite side wall, it is 'self-welded' to the side wall by continued catalysed decomposition. Details of the process are described in [15].

Figure 1(a) shows a schematic diagram of a nanowire fabricated between silicon electrodes and figure 1(b) shows a top-view SEM image of one of the measured devices with one bridged nanowire. Current–voltage ($I$–$V$) characteristics of the nanowires were measured by simultaneously applying DC voltage between the electrodes, and measuring current through the nanowires. The resistance between the probes and the electrodes was negligible with respect to the resistance of the nanowires (less than 0.1%). The current–voltage characteristics of the nanowires were linear, which shows that the nanowires made good electrical contact to the silicon electrodes [15]. The resistance between two unbridged electrodes was measured to be 200 ± 40 GΩ, which is more than two orders of magnitude higher than the resistance of nanowires throughout the size reduction experiments. We did not observe any uncatalysed growth of Si on $SiO_2$. The electrodes in our devices were separated by a thin $SiO_2$ layer (BOX of SOI). This helped to maintain a high degree of isolation even when the nanowires were tapered due to some deposition of uncatalysed Si on all available Si surfaces during the CVD process. Our measurement set-up limited high resistance suggests that there was no conducting Si layer deposition between the electrodes.

Six devices with different numbers of nanowires were selected with diameters ranging from 90 to 160 nm. Most of the nanowires were found to be cylindrical, and some of them were tapered. For the most tapered nanowire, the diameter at the tip was 72% of the diameter at the root. Table 1 lists the length, diameter at the root and diameter at the tip of the nanowires used in this experiment. Diameter reduction of the nanowires was done with successive isotropic silicon etching and native oxide etching.

Isotropic etching of silicon was performed with a wet etch solution at room temperature. Although the etch rate of anisotropic etch solutions at room temperature is very low, the etch rate of isotropic etch solutions can be appreciable [17]. We developed a low etch rate isotropic etchant for silicon by modifying a solution reported previously by Williams *et al* [18]. (100) and (110) oriented wafers were patterned with Shipley 1813 photoresist and the samples were heated at 120 °C to increase the chemical resistance of the photoresist. Because HF–$HNO_3$–$CH_3COOH$ (HNA) solutions cause loss

**Table 2.** The etch rate of (100) and (110) oriented Si substrates in nitric acid based solutions with ammonium fluoride at different temperatures.

| | Etch rate of solution (nm min$^{-1}$) | | | |
|---|---|---|---|---|
| | $HNO_3$:$H_2O$:$NH_4F$ (60:125:6) | | $HNO_3$:$H_2O$:$NH_4F$ (150:75:5) | |
| Orientation | At 32 °C | At 27 °C | At 27 °C | At 23 °C |
| ⟨100⟩ | 356 | 276 | 78 | 46 |
| ⟨110⟩ | 280 | 214 | 76 | 47 |

of photoresist adhesion, diluted ammonium fluoride ($NH_4F$) was used as the silicon etchant. $HNO_3$:$H_2O$:$NH_4F$ solution was reported by Williams *et al* as an isotropic etchant for silicon [18]. We varied the water to nitric acid ($HNO_3$) ratio and measured the etch rates for both wafer crystal orientations. Table 2 shows the etch rates of the two solutions at different temperatures. $HNO_3$:$H_2O$:$NH_4F$ solution with 150:75:5 volume ratios gave the best isotropy with a slow etch rate at 23 °C.

Native oxide on the surface of the nanowires was etched with a diluted HF solution (1 HF (49%):20 de-ionized $H_2O$). The nanowires were etched for 15–30 s in the solution, which was enough to remove native oxide, estimated to be ∼3 nm in thickness based on our experimentally measured values. We did not increase the etch duration as it has been reported that extended treatment in concentrated HF solution causes roughening of nanowire surfaces [15].

Initially, we treated the devices with native oxide etchant to observe the effect of $H^+$ ion rich solution on the resistance of the nanowires. At each step we measured the $I$–$V$ characteristics as described before. After the treatment, we observed that the resistance of the nanowires increased. The increase is attributed mainly to the $H^+$ ions adsorbed to the surface of the nanowires [19]. The additional positive charges on the surface of p-doped nanowires increase the depletion layer thickness, which in turn decreases the cross-section area of the conductive inner core as shown in figure 2(a). After the HF treatment, the resistance remained unchanged for more than 7 days if the devices were kept at room temperature. We heated the devices in an uncontrolled room ambient to sever the bonds between the surface and the hydrogen ions, which decreased the positive charge density by desorbing $H_2$ from the surface. The devices were heated at 120, 150 and 180 °C for 1 min. We did not further increase the temperature or the duration of heating in order to avoid any dopant segregation, which typically starts around 500 °C for bulk Si wafer surfaces. As the temperature was increased, we observed a decrease in the resistance of the devices. Most of the devices were found to approach their initial resistance values, consistent with modification of surface charges by etching and annealing. Figures 2(b) and 3(a) show the results of current–voltage ($I$–$V$) measurements, and the corresponding resistance values. Immediately after the $I$–$V$ measurements, the diameter and the length of the nanowires were measured with high-resolution SEM. The sample was then kept in an uncontrolled room environment for about two months and the resistance was measured again. We observed an increase of 30% in the resistance, which we attribute to oxidation of the surface

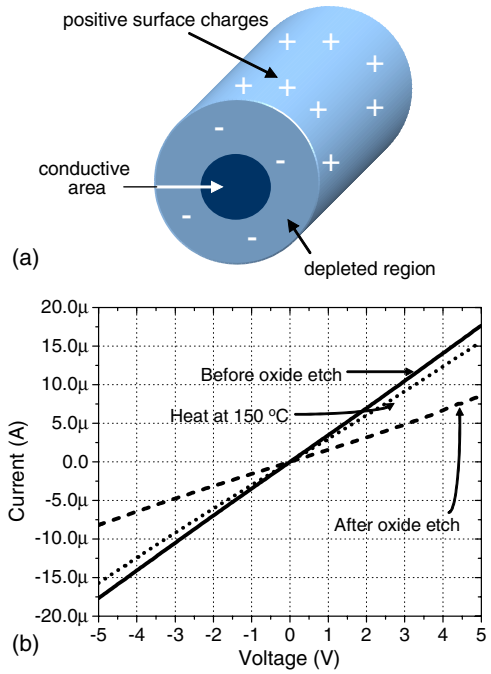


**Figure 2.** (a) Schematic diagram of a p-doped nanowire with positive surface charges and depleted region. (b) The current–voltage characteristics of device 2 during the native oxide etch and the heat treatment.

contributing to the reduction of nanowire diameter. Based on our measurements, we estimated the thickness of the oxide layer to be around 3 nm.

The diameter of the nanowires was reduced with an isotropic silicon etch solution. Before applying the silicon etchant, we removed the oxide layer from the surface of the nanowires. We then etched the devices in isotropic silicon etch solution for about 1.5 s. Similar heat treatment was applied as after the native oxide etch. The resistance of the device increased to a very high level after the isotropic etch due to the reduction of the diameters of the nanowires and increase of surface charge. With subsequent heat treatment the resistance decreased further, as shown in figure 3(b). SEM measurements indicated that the diameters of the nanowires were reduced to ∼37 nm. This showed that the etch rate of nanowires with the isotropic silicon etch solution was around 10 nm s$^{-1}$, which was about 13 times faster than that of bulk silicon wafers. It is not clear why the etch rate of Si nanowires was more than an order of magnitude faster than that of bulk Si wafer. Several possibilities, including the circular cross-section that causes a different liquid–solid interface compared to a plane semi-infinite surface, catalyst assisted growth of nanowires at low temperature (∼640 °C in our experiments) or the presence of catalysts (Au in this experiment) throughout the nanowire stem (as was reported by Perea *et al* [20]), need to be investigated. A discernable chemical difference in the material quality between bulk Si and the nanowires was also recently observed by Mayer *et al* while oxidizing Si nanowires, that resulted in a faster nanowire oxidation rate [21].

The surface roughness of the nanowires before and after the isotropic etch were compared to see the effect of etchant. Although most of the as-grown nanowires had smooth

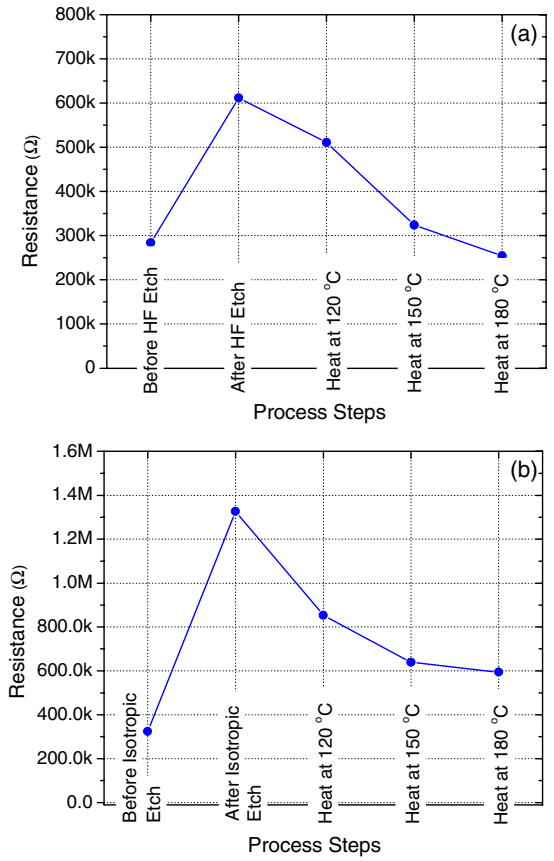


**Figure 3.** Resistance of the nanowires of device 2 during (a) the native oxide etch and (b) the isotropic silicon etch.

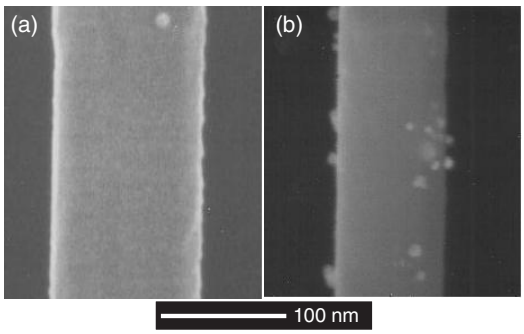


**Figure 4.** The SEM images of nanowires before (a) and after (b) etching.

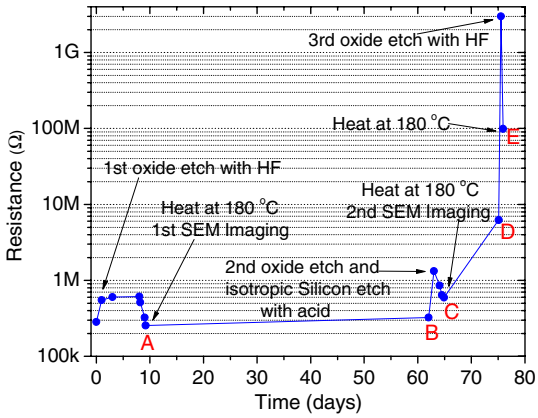


**Figure 5.** Resistance of device 2 measured as a function of time. The increase in resistance after each etch step can be seen. As the diameter was reduced, the ratio of the resistance after the etch to the resistance before the etch increased, which shows that the increase of the depletion layer thickness due to additional $H^+$ charges becomes more effective in increasing the total resistance. The identical states of the surface are indicated by letters: A, C, and E correspond to low surface charge state after the etches; B and D correspond to surfaces with native oxide.

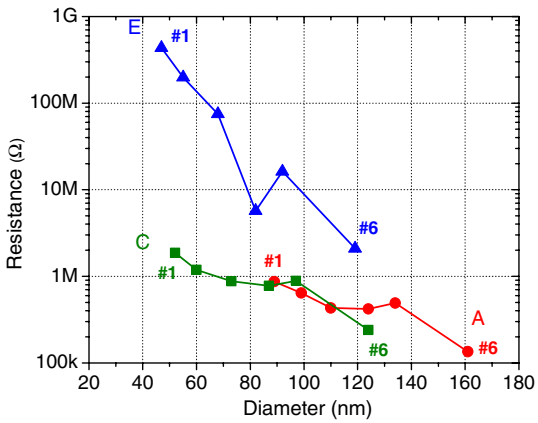


**Figure 6.** The resistance of six devices measured at process steps indicated by A (-●-, after first oxide etch), C (-■-, after isotropic silicon etch), and E (-▲-, after third oxide etch).

sidewalls, some of them had sawtooth facets. This kind of roughness is caused by the instability of the Au catalyst during the growth, which has previously been reported by *in situ* observations of nanowires during growth [22]. Figure 4 shows the SEM micrographs of nanowires before and after the etch. Although we observed some particles on the surface of the nanowires (probably caused by a redeposition of etched residues from the etching solutions), no roughness was observed on the sidewalls.

Because of the high etch rate of the isotropic silicon etch solution, the final etch used for the wire thinning experiments was an oxide etch instead of the silicon etch. After the previous etch step, devices were exposed to air for 10 days, which was enough to form ∼2 nm thick oxide layer on the surface, then etched using the oxide etch solution. The resistance of the devices increased after the native oxide etch, and decreased as the devices were heated, as observed in the previous etch steps.

Figure 5 shows the resistance of device 2 measured during the size reduction process. The same characteristics were also observed for other devices. The total process consisted of three etch steps followed by heat treatments. After etching and heating the devices at 180 °C, we assume that identical surface conditions are achieved as similar numbers of $H^+$ ions were present in the etchant solution (points A, C, and E in figure 5). Figure 6 shows the resistance per nanowire for the six devices used in the measurements. It is clear that the resistances of the nanowires increased as the diameters were reduced through steps A–E, contributing to a reduction in the cross-section area of the conductive inner volume. We observed a nonlinear

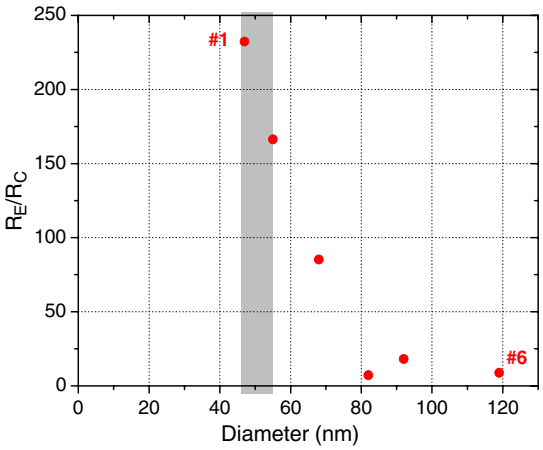


**Figure 7.** The resistance ratio of the devices after the final etch to the isotropic silicon etch. Although this ratio is almost the same for large area nanowires, a non-linear increase can be seen for small area nanowires. This non-linear increase is due to the nearly complete depletion of the small-area nanowires. The shaded area shows the range of diameter over which the nearly complete depletion was observed.

increase in the resistance of the nanowires as we did the final native oxide etch. Although the amount of the reduction in the diameter was quite low when compared to the isotropic etch step, the effect of this final etch on the nanowire resistances was very high. We calculated the ratio of resistance between steps C and E. Figure 7 shows the ratio ($R_E/R_C$) as a function of the nanowire diameter. It is seen that the resistances of small nanowires (devices 1 and 2, which had 47 and 55 nm final diameters respectively) increased by more than two orders of magnitude. This is an indication of near complete depletion of the nanowires. We concluded that the depletion layer thickness for small area nanowires was around 25 nm for the surface charge corresponding to state E. The depleted layer occupies the majority of the volume, and the conductive cross-section area is much less than the physical cross-section for the nanowires, with the depletion layer thickness comparable to the nanowire radius. By assuming a uniform density of dopant atoms throughout the cross-section of a nanowire, we estimated the doping concentration of the nanowire. The resistance of the nanowire is given by

$$R = \rho \frac{L}{A_{\text{con}}} = \rho \frac{L}{\pi \left(\frac{d}{2} - \delta\right)^2}, \tag{1}$$

where $A_{\text{con}}$ is the cross-section area of the conductive region, $\rho$ is the resistivity of the nanowire, $d$ is the diameter of the nanowire, and $\delta$ is the depletion layer thickness. After calculating the resistivity, we estimate the dopant concentration to be $(2.1 \pm 0.60) \times 10^{18}$ cm$^{-3}$. It has previously been observed that the resistivity of highly doped Si nanowire is very similar to bulk silicon [23], and we also used the resistivity of bulk silicon to find the corresponding doping concentration of nanowires. The total charge of the nanowire is zero, which implies that the charges in the depleted region should be equal to the surface charges. The surface charge density can be expressed as

$$\sigma = N_A \delta \left(1 - \frac{\delta}{d}\right), \tag{2}$$

where $\sigma$ is the surface charge density, and $N_A$ is the dopant concentration. Given the estimate for $N_A$ above, the surface charge density is found to be $(2.6 \pm 0.75) \times 10^{12}$ cm$^{-2}$. This value is one order of magnitude higher than the value measured for the bulk silicon wafer [13]. This can be attributed to the cylindrical shape of the nanowires, and thus the large number of dangling bonds on the curved surface, or the oxide formation at room temperature.

In conclusion, we developed a slow isotropic silicon etchant to reduce the diameter of nanowires at room temperature. By comparing the resistance of nanowires with identical surface conditions throughout the etching process, we found a depletion layer thickness of ~25 nm for the nanowires doped to ~$2.1 \times 10^{18}$ cm$^{-3}$. Our observation indicates that a non-negligible depletion layer thickness is present in the doped silicon nanowires, and it needs to be carefully evaluated when designing nanowire-based devices. Although we assumed an unvarying radial dopant profile, a careful study is needed to determine the actual dopant profile. The results of this work will facilitate the integration of 1D nanowires in existing devices and circuits for further enhancement of functionality in electronic and photonic systems.

## Acknowledgments

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