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Ultra-Low Contact Resistance of Epitaxially Interfaced Bridged Silicon Nanowires

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ABSTRACT

Laterally oriented single-crystal silicon nanowires are epitaxially grown between highly doped vertically oriented silicon electrodes in the form of nanobridges. Resistance values extracted from the current–voltage measurements for a large number of nanobridges with varying lengths and diameters are used to propose a model which highlights the relative contribution of the contact resistance to the total resistance for nanowire-based devices. It is shown that the contact resistance depends on the effective conducting cross-section area and hence is influenced by the presence of a surface depletion layer. On the basis of our measured data and constructed model, we estimated the specific contact resistance to be in the range 3.74×10^{-6} to 5.02×10^{-6} Ω cm^2 for our epitaxial interfacing method. This value is at least an order of magnitude lower than that of any known contact made to nanowires with an evaporated metal film, a common method for integrating semiconductor nanowires in devices and circuits.

Granted that the technological momentum is pushing for the incorporation of nanostructures in devices, integrated circuits (ICs), and systems and that the technology is there to synthesize diminishingly small nanostructures such as nanodots, nanowires, or nanotubes, it becomes obvious that we must now look for ways to take advantage of them in solving pressing issues in electronics, photonics, defense, energy conversion, sensing, and biomedical applications. The functionality of conventional electronics (e.g., CMOS technology) and photonics can be significantly augmented by using one-dimensional, self-assembled nanowires as device channels,[1,2] interconnects,[3] light emitters, and detectors.[4,5] Despite substantial progress in the demonstration of novel applications of nanowires, interfacing and integrating nanowires in devices and circuits has remained a formidable challenge since they were first envisioned as building blocks of many future applications. A significant roadblock to wide-scale integration of functional nanowire-based devices is the difficulty in forming contacts to the nanowires.[6] A scheme aimed at integrating nanowires in devices and circuits should be universal, compatible with current IC processing methods, and cost-effective. In addition, precise control on the nanowire length, reliable and low contact resistance, and good mechanical robustness will be highly desirable. To date, many reported techniques for fabricating nanowires in controlled and reproducible fashion did not meet most of the above-mentioned requirements and a dramatically new approach is needed for integrating nanowires with conventional circuitry.

Islam et al. reported a novel epitaxial bridging technique for interfacing Si[7] and InP[8] nanowires between Si electrodes. The technique resulted in highly linear ohmic contacts caused by an epitaxial connection between the nanowire and electrodes[9] and thus contributing to very low noise.[10] Yang[11] and Lin[12] et al. also reported similar techniques for interfacing Si nanowires. By avoiding the deteriorations of nanowires during the postprocessing, the technique addresses the issue of mass manufacturability to make the nanowire-based devices a commercial reality with a major improvement in the cost/performance ratio. In this Letter we report very low contact resistance for Si nanowires estimated using an empirical model which is based on current−voltage ($I-V$) measurements on Si nanobridges. Contact resistance was found to inversely depend on the effective wire cross-section area and calculated to be in the range 3.74×10^{-6} to 5.02×10^{-6} Ω cm^2 for bridged silicon (Si) nanowires. Comparison of these results with reported literature on contact resistance of nanowires highlights the potential of bridged nanowires for manufacturable device integration.

The bridged Si nanowires used in this study are boron doped (p-type) and were synthesized by the metal-catalyzed chemical vapor deposition (CVD) between two electrically isolated Si electrodes as described previously.[7] In brief, a silicon-on-insulator (SOI) wafer with a 5 μm thick device layer and a 100 nm thick buried oxide layer was patterned

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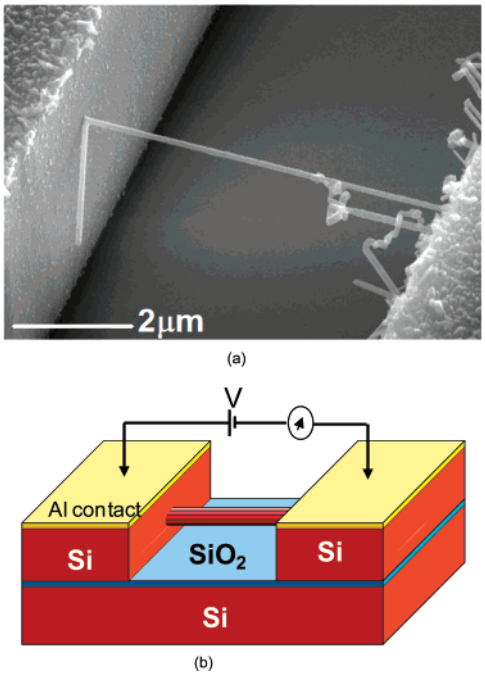

Figure 1. A bridged Si nanowire between two Si electrodes. (a) SEM image of a single Si nanowire grown using Au-catalyzed CVD process. The nanowire grows perpendicular to the (111) lattice planes visible in the micrograph. (b) Schematic view of a setup for measuring the current−voltage ($I-V$) data of a bridged Si nanowire. The Al contact pads are biased with an external power supply, and the current flowing through the nanowire is measured. This is repeated for wires with different lengths and diameter. Resistance values are extracted from the $I-V$ data.

and etched using RIE to form two electrically isolated electrodes with their edges perpendicular to the ⟨111⟩ planes of the substrate. The gap between electrodes was varied between 1 and 10 μm. A ∼1 nm thick layer of gold (Au) was deposited on one of the sidewalls of the electrodes to act as catalyst for the Si nanowire growth. The sample was then heated in a CVD chamber in a hydrogen-rich ambient to form Si/Au alloy nanoparticles. Subsequently, at a temperature of 640 °C, a gas mixture of SiH_4, HCl, and diborane (B_2H_6) (for p-type doping) was introduced into the chamber. HCl suppresses uncatalyzed growth on the sides of the nanowires ensuring uniformity of the wire diameter.[9] The nanowires grew across the gap toward the (111) oriented sidewall of the opposite electrode. Upon reaching the opposite sidewall, the nanowire "self-welded" by continued catalyzed decomposition. Aluminum (Al) contact pads (∼400 μm × 200 μm × 250 nm thick) were then deposited on the Si electrodes after resist patterning, oxide etch, Al deposition, and lift-off process. The devices were then annealed at 450 °C in forming gas. Figure 1a shows a scanning electron micrograph (SEM) image of our bridged Si nanowire.

Figure 1b shows a schematic of a typical two-terminal current−voltage ($I-V$) measurement setup on such suspended nanowires. The nanowire device samples were measured by applying a dc voltage sweep from −5 V to +5 V and simultaneously reading the current flowing in the circuit. A four-probe measurement setup was used to eliminate the effect of the resistance between the probes and the electrodes. Moreover, resistance between the electrodes and the probes was found to be negligible (less than 0.1% in comparison to the measured nanowire resistance). The $I-V$ measurements yielded linearly varying current as the applied bias voltage was increased, indicating Ohmic behavior for Si nanobridges. As can be seen from Figure 2, the total resistance of the suspended nanowire extracted from typical $I-V$ measurements can be modeled as three separate components: (1) resistance of the electrode region, i.e., due to the Si electrode along with the resistance contributed due to Al contact with p-type Si electrode; (2) resistance of the nanowire; (3) contact resistance (between the nanowires and the Si electrode).

Resistance of the Electrode Region. Figure 2 identifies the electrode region in a nanowire measurement setup. The electrode region includes only the "top-half" of the p-doped Si electrode since the insulating oxide layer over the Si substrate precludes the current flow through the bottom-half of the electrodes. This resistance ($R_{\text{electrode-region}}$) can be analyzed using a transmission line (TL) based model.[13] As expected, the resistance of the electrode region decreases as doping of the Si electrodes increases and is considerably low for large metal contact pads. Resistance measurements on Si electrodes (without any Al contact pad) using two-probe and four-probe techniques confirmed that the $R_{\text{electrode-region}}$ is ∼50−100 Ω. This is about 0.01% of the total measured resistance, R_{Total}.

Hence for the heavily doped electrode regions and large Al contact pads, the contribution of this component to the total resistance is negligible.

Resistance of the Si Nanowire. The doping profile in a Si nanowire influences its resistance. In this Letter, we assume a uniformly doped nanowire. This is a reasonable assumption given the boron dopant concentration in the low 10^{18} cm^{-3} range.[7a] Assuming the resistivity of the nanowire as ρ_{NW}, the resistance of a nanowire of length L_{NW} and a cross-section area A_{NW} is given as

$$R_{NW} = \frac{\rho_{NW} L_{NW}}{A_{NW}} \tag{1}$$

Published works[14] have made the observation that the Si nanowire surface could be depleted of charge carriers due to an accumulation of positive surface charges resulting in a reduction of conducting cross-section diameter and hence the effective conducing area. We estimated the surface charge density on our nanobridge surfaces to be ∼3 × 10^{12} cm^{-2}, which is at least one order of magnitude higher than the value measured for a bulk Si wafer.

Contact Resistance. This resistance (R_{contact}) is defined as the resistance at the interface of the nanowires and the Si electrodes. A schematic of a nanowire/electrode interface is shown in Figure 3 along with a SEM micrograph of an actual contact of a nanowire impinging end. Modeling this resistance is challenging since it depends on the quality of contact made to the electrodes. Moreover, the two contacts of the nanowire to the electrodes are not expected to be the identical in performance, since the vapor−liquid−solid (VLS) process

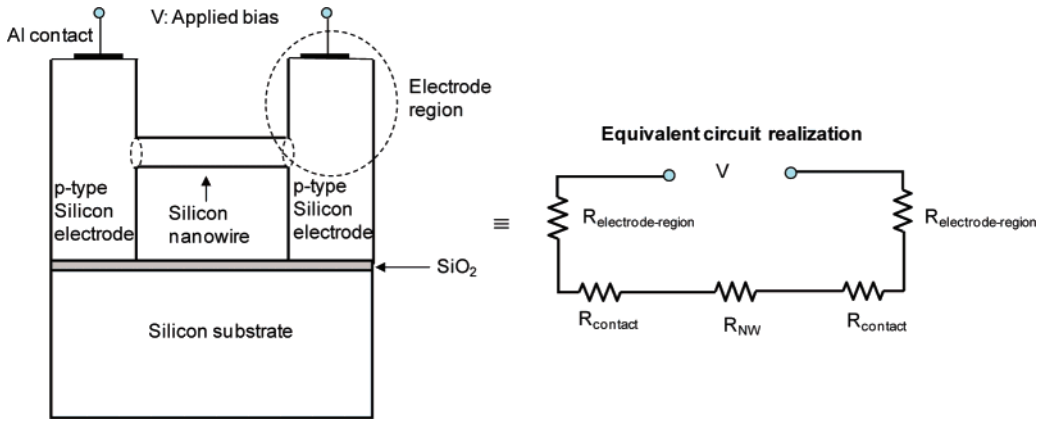

Figure 2. Schematic to illustrate the resistive components of the total measured resistance. The current flows through the electrode region (top half of the Si electrodes) and the bridged nanowire. Hence, the total measured resistance can be modeled as a sum, $R_{\text{Total}} = 2R_{\text{electrode-region}} + 2R_{\text{contact}} + R_{\text{NW}}$.

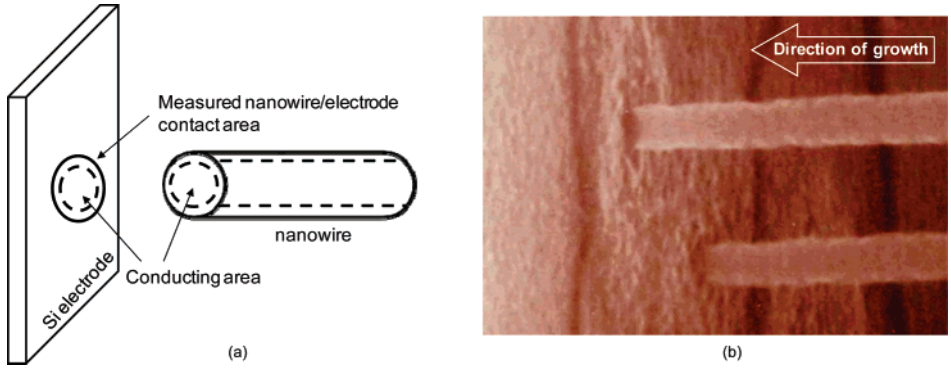

Figure 3. Schematic view of a nanowire/electrode contact. An SEM of an actual contact is also shown to illustrate the potential impact of contact quality on R_{contact}. The presence of a depletion layer on the Si nanowire surface reduces the effective conducting cross-section area. The nanowire−electrode interface resistance or R_{contact} depends on the effective conducting cross-section area.

characteristic of Si nanowire growth generally leads to a "better" contact at the root of the nanowire as compared to the tip or the impinging end.[10] The tip of a nanowire makes contact to the Si electrode through the pinholes of the residual native oxide,[9] and hence its resistance is expected to be dominant. In the next section, we describe the method of establishing an empirical relationship based on measured data of bridged Si nanowires.

The total resistance extracted from the $I-V$ measurements for a nanowire with given length L_{NW} and radius r_{NW} (cross-section area, $A_{\text{NW}} = \pi r_{\text{NW}}^2$) is given by

$$R_{\text{Total}} = 2R_{\text{electrode-region}} + 2R_{\text{contact}} + R_{\text{NW}} \qquad (2)$$

The Si electrodes are generally heavily doped and with large contact pads it is reasonable to assume that the contribution of $R_{\text{electrode-region}}$ to the total resistance is negligibly small. Figure 4 shows a plot of the measured resistance (normalized by length) versus square of cross-section radius (proportional to the cross-section area, A). We see that the observed dependence of R/L decreases approximately as $A^{-1.20}$. This is greater than A^{-1} and hence suggests the existence of near surface depletion region due to the presence of positive charges on the surface of the nanowire. Seo et al. also recently reported a similar observation on the surface-charge density of p-doped Si nanowires.[14]

Equation 2 indicates that we can calculate the contribution due to R_{contact} by subtracting the nanowire resistance R_{NW} from the total resistance R_{Total}. To compute the nanowire resistance R_{NW} considering the effect of surface depletion, an estimate of the Si nanowire resistivity ρ_{NW} is required. Since we expect the Si nanowire resistance to be the dominating component, a way to extract ρ_{NW} is to find the slope from the plot (Figure 5) of measured total resistance as a function of length/(area)$^{1.20}$. Considering the best linear fit to the dataset, we find the nanowire resistivity as

$$\rho_{\text{NW}} = \text{slope(from Figure 5)}\ \pi^{1.20} = 0.29\ \Omega\cdot\text{cm}$$

Now using this value of ρ_{NW}, we can estimate the contribution of R_{contact} to the total resistance R_{Total}. Since R_{contact} is at the interface of the nanowire with the Si electrodes, it is expected to be inversely dependent on the nanowire cross-sectional area. Figure 6 shows a plot of $0.5|R_{\text{Total}} - R_{\text{NW}}|$ versus r_{NW}^2. A reciprocal fit to the data confirms the inverse dependence of the R_{contact} ($=0.5*|R_{\text{Total}} - R_{\text{NW}}|$) on the nanowire cross-section area as in eq 3

$$R_{\text{contact}} = 0.06(r_{\text{NW}}^2)^{-1.14} \qquad (3)$$

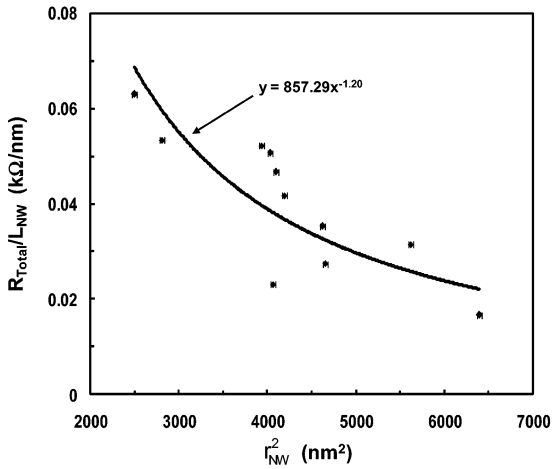

Figure 4. Total resistance (normalized by length) as a function of measured cross-section area. Resistance values were extracted from the measured $I-V$ charactersitcs of bridged Si nanowires. The presence of surface depletion layer enhances the dependence of resistance on the nanowire cross-section area. Error bars on the figure indicate the uncertainty associated with nanowire diameter measurement using SEM imaging.

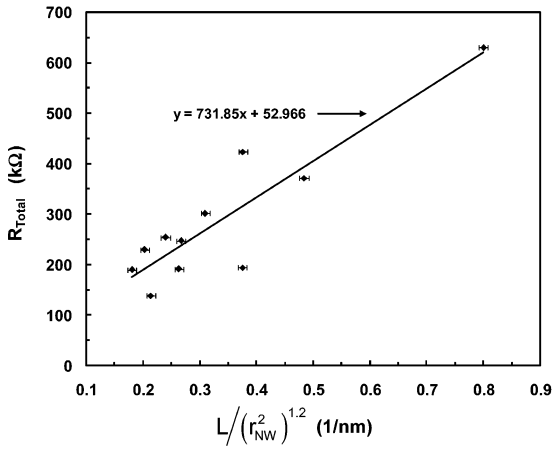

Figure 5. Total measured resistance as a function of length/(radius^2)$^{1.20}$. Nanowire resistivity can be estimated by the effect of surface depletion on the effective conducting cross-section area.

This shows an increase in the relative contribution of the nanowire−electrode junction resistance for small-diameter nanowires. This dependence on r_{NW}^2 is very close to the dependence of the measured total resistance R_{Total} on r_{NW}^2 as in Figure 4. This leads us to believe that the "actual conducting contact area" between the Si nanowire and the Si electrode at the interface is almost the same as effective wire cross-sectional area. We conjecture that this behavior will continue until the quantum effects begin to dominate in nanowires with very small diameters. It has also been shown that the contact resistance of metal−semiconductor nanoscale contacts depends on the nanowire cross-section area.[13,15] In particular, increased tunneling distance and reduced range of tunneling energies are found to be responsible for rapid increase in contact resistance as the nanowire diameter is decreased in heavily doped semiconductor nanostructures.[15]

We estimated the specific contact resistance to be 3.74×10^{-6} to 5.02×10^{-6} Ω cm^2 for bridged Si nanowires. This

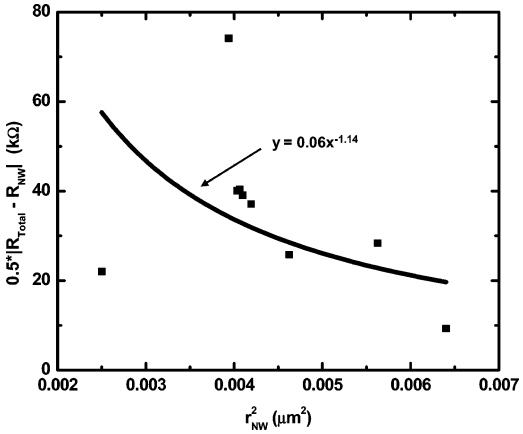

Figure 6. $0.5|R_{Total} - R_{NW}|$ as a function of square of nanowire radius. The total contact resistance $R_{contact}$ can be estimated as the difference $R_{Total} - R_{NW}$. The contribution of the electrode-region resistance can be safely neglected for heavily doped Si electrodes and large Al contact pads.

value reflects almost 2 orders of magnitudes of improvement over 5.0×10^{-4} Ω cm^2 measured for Ti/Au contacts to p-type Si nanowires[13] and an order of magnitude improvement over 1.7×10^{-5} Ω cm^2 measured for Ti/Au contacts to GaN nanowires,[16] highlighting the superior characteristics of our barrier-free epitaxial nanowire interfacing process. The value is an average of the contact resistances of both root and the tip ends, and we believe the tip (impinging end) contributes more to the total contact resistance. More work isolating each contact will shed light on the individual contact properties.

The considerably low contact resistance extracted for bridged Si nanowires can be attributed to the metal-catalyzed CVD growth technique used to synthesize the Si nanobridges. Sharma et al. reported that the nanowire/electrode contact at the impinging end of the trench was epitaxial.[9] They observed that the catalyst (gold) remains active until a firm Si-to-Si contact forms between the nanowire and the uncatalyzed silicon deposited on the impinging sidewall. This epitaxial Si−Si connection at the nanowire/electrode junction yields very low resistance contacts to our bridged Si nanowires.

It is of interest to compare this result with the popular nickel silicide (NiSi) contacts to planar Si devices.[17a,b] NiSi is an attractive choice for achieving contacts with low resistance to both p-type and n-type Si substrates because of its low Si consumption, low-temperature rapid thermal annealing process, and low sheet resistivity. NiSi contacts to planar Si can have contact resistance as low as $10^{-6}-10^{-7}$ Ω cm^2. Recently, Wu et al. demonstrated low-resistance single-crystal NiSi nanowires with diameters in the range of 15−45 nm.[17c] A maximum current density of 3×10^8 A cm^{-2} was reported for these NiSi nanowires. Moreover, an FET made using NiSi/Si nanowire heterostructure with metallic NiSi nanowire sections as source/drain showed that the NiSi/Si contacts behave as ohmic contacts for practical purposes. This shows the potential of NiSi toward realizing ultralow contact resistance nanoscale devices. Our technique of epitaxially grown nanowires between Si electrodes, however, achieves almost the same order of magnitude of

contact resistance as demonstrated for planar devices using NiSi contacts. Further process optimization toward the contact connections is likely to yield extremely low contact resistance in Si nanobridges.

The methodology adopted for extracting the contact resistance of bridged Si nanowires benefits from their unique growth process which allows for in-circuit measurements. This is unlike the commonly adopted techniques of separating nanowires from their substrate and then depositing contact electrodes at the ends of a nanowire placed on electrically insulating substrate such as SiO_2.[6b] Contacts formed with deposited metals are known to pose challenges like Schottky barrier[6c,16] which are hard to overcome. Moreover, our results show that for nanowires with depleted surface area (due to the presence of surface charges) the "effective conducting cross-section area" of the nanowire is related to both the nanowire resistance and the contact resistance. This observation could be potentially useful for calibrating nanowire sensors for biological and chemical applications which rely on nanowire conductivity modulation to detect the presence of analyte molecules in the ambient.

To gain further insight on the impact of this finding on a nanowire-based integrated circuit, it would be useful to consider an application such as a gas sensor. We consider an array of few thousand nanowire-based sensors integrated with associated signal processing electronics on a SOI wafer. To enhance the sensitivity of the nanowires, they are functionalized by selective coatings specific to the target gas molecules. Upon exposure to the gas molecules, the conductivity of the nanowires will be modulated by the binding of the gas molecules on the nanowire surface.[18] We have shown that as the effective conducting nanowire cross-sectional area reduces, its resistance increases along with the contact resistance. Assuming that very few gas molecules bind to the surface close to the contacts, a careful calibration of the nanowire resistance is required to avoid false alarms. This requirement is expected to be stringent for small diameter nanowires when the contact resistance contribution to the total measured resistance is significant. Moreover, for the associated signal processing circuitry a sizable percentage of transistors are analog. Assuming these field effect transistors (FETs) are fabricated using Si nanowires, such nanotransistors would have to be carefully designed to minimize the contact resistance to avoid deleterious effects of noise[10] apart from increased source and drain resistance due to the nanowire contact resistance. We should also consider the effect of nanowire contact resistance on power dissipation for such an integrated circuit. For small diameter nanowires, contact resistance cannot be neglected in comparison with the nanowire resistance and hence its consequent contribution toward increased Joule heating would be detrimental to the limited power budget of such nanosensor integrated circuits.

In conclusion, we have empirically shown that the relative contribution of the nanowire/electrode interface resistance (or contact resistance, $R_{contact}$) to the total resistance becomes significant for small diameter bridged Si nanowires. The technique presented in this Letter is useful for a fast and reliable estimate of the nanowire contact resistance from the in-circuit current−voltage measurements of nanobridges synthesized by metal-catalyzed CVD deposition. The specific contact resistance is calculated to be 3.74×10^{-6} to 5.02×10^{-6} Ω cm^2 for bridged Si nanowires. This is almost an order of magnitude lower than previously reported contact resistances measured for nanowire-based devices fabricated using evaporated metal contacts. In addition, we analyzed the potential implications of enhanced contact resistance for small diameter nanowires integrated on a Si ICs. Bridged Si nanowires have demonstrated highly linear contact characteristics along with potential benefits of their good mechanical robustness, precise control on the lengths, and ease of integration in the Si processing technology. Our interfacing technique emerges as a promising candidate to realize massively parallel and mass-manufacturable synthetic "*bottom-up*" technique for high-density integration of nanowire-based devices and circuits beyond the capability of conventional technologies with a small fraction of the present-day fabrication cost.

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