An Approach to
Low-power, High-performance,
Fast Fourier Transform Processor Design

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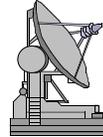
May 23, 1997

Outline

- ## Motivation and Introduction

- **Energy-Efficient VLSI Processing**

- **Fast Fourier Transform Overview**

- **FFT Chip Architectures**

- **The Spiffee Processor**

- **Conclusion**

The Fast Fourier Transform (FFT)

- **One of the most widely used digital signal processing algorithms**
- **Used in:**
  - ◆ Communications
  - ◆ Radar
  - ◆ Instrumentation
  - ◆ Medical imaging

Low Power

- **As semiconductor processing technology advances....**
  - ◆ Clock speeds increase
  - ◆ Integration increases
    - ⇨ Power increases

Year	1995	1998	2001	2004	2007
Technology	0.35μm	0.25μm	0.18μm	0.13μm	0.10μm
Vdd	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V
Clock	300 MHz	450 MHz	600 MHz	800 MHz	1000 MHz
Power	80 W	100 W	120 W	140 W	160 W

Source: SIA Roadmap

- **More and more applications are power-limited**

Areas of Contribution

- **FFT algorithm and architecture for high energy-efficiency and high-performance**

- **Circuits for low voltage operation**

- **Design of a single-chip, 1024-point, FFT processor**

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CMOS Power Consumption

- **Power = P_{active} + $P_{leakage}$ + $P_{short\text{-}circuit}$**

Active
Short-circuit
Leakage

C_{LOAD}
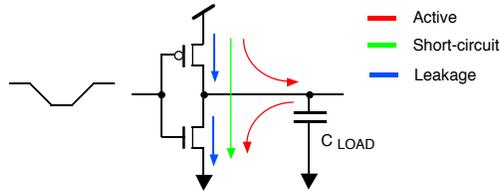
- **P_{active} = $\sum\limits_{all\ nodes}$ activity * C * V^2 * frequency**

Energy-Efficiency

- **Goal is energy-efficiency with good performance**
  - ◆ Not just low-power, which can be easily obtained by reducing performance

- **For DSP, high energy-efficiency is key**
  - ◆ Algorithms are often easily parallelized
  - ◆ Often insensitive to latency
  - ◆ Therefore, high-performance can usually be obtained through parallel processors

4

Ultra Low Power (ULP) Overview

- **Key idea: Biggest gain by lowering supply voltage**
  - ◆ Switching energy is a strong function of V^2
- **To maintain performance, must also lower V_t**
  - ◆ Lowering V_t significantly requires a process change
- **Adjust V_t by biasing substrate/wells**
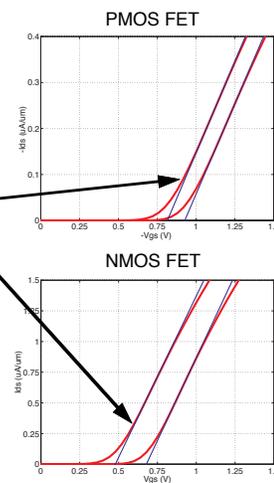 - ◆ Substrate/well nodes
    routed to pads

Vpsub   Vnwell
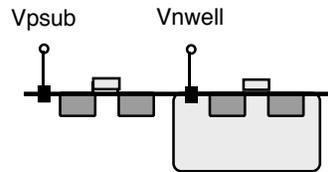
Measured V_t Adjustments

- **V_t shifted by adjusting nwell/p-substrate bias**

PMOS FET

-Ids (uA/um)

-Vgs (V)

Bias reduces V_t

NMOS FET

Ids (uA/um)

Vgs (V)

| Well / Substrate Bias	NMOS V_t	PMOS V_t
(Volts)	(Volts)	(Volts)
0.0 V	0.63	-0.88
0.5 V	0.43	-0.77

ULP Implications

- **Circuits operate with "leaky" transistors (low $\frac{I_{on}}{I_{off}}$ ratio)**

- **Static circuits generally ok**

- **No pure dynamic circuits, nmos pass gates,....**

- **Redesign high fan-in circuits**

I_{on} I_{off}
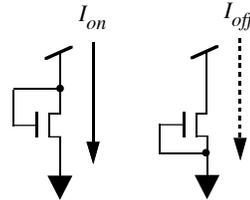
Low Vt Design

- **Nodes with high fan-in require re-design**

- **Memory bitline is a common structure with high fan-in**

- **Worst case: Reading a '0' in a column with M-1 '1's**
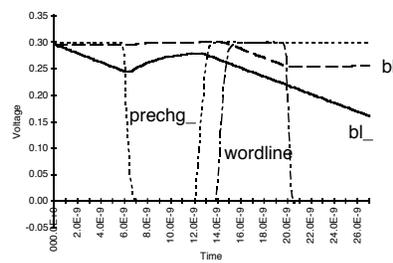
1

1

1

0

wordline on

SA
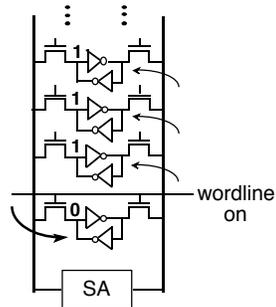
Hierarchical-Bitline SRAM

- **2-level hierarchical bitlines**
  - ◆ Reduces cell leakage on bitlines
  - ◆ Reduces bitline capac-itance by almost 50%
- **8 Local-bitlines
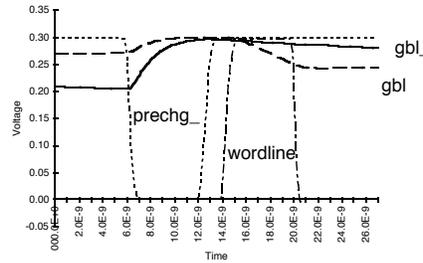 x 16 cells each**
- **3 Separate nwell biases**
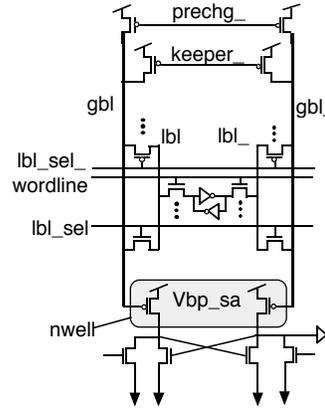
Simulation Results

- **128 word memory, Vdd=300mV, parasitics included**

Non-hierarchical bitline
read failure

Hierarchical bitline
read

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# The Fast Fourier Transform (FFT)

- **Efficient method of calculating the Discrete Fourier Transform (DFT)**
- **Believed discovered by Gauss in 1805**
- **Re-discovered by Cooley and Tukey in 1965**
- **N = length of transform, must be composite**
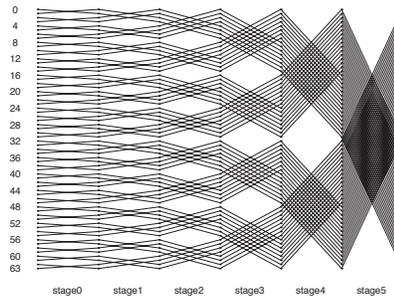 - ◆ $N = N_1 * N_2 * ... * N_m$

Transform Length	DFT Operations	FFT Operations	DFT ops / FFT ops
64	4,096	384	**11**
256	65,536	2,048	**32**
1,024	1,048,576	10,240	**102**
65,536	4,294,967,296	1,048,576	**4,096**

FFT Notation

- **Butterfly**

A   X
B   Y

- **Dataflow diagram**

stage0   stage1   stage2   stage3   stage4   stage5
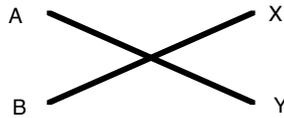
FFT Hardware Algorithms

- **Simple, compact design more important than the number of operations**
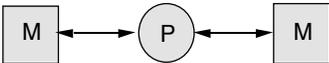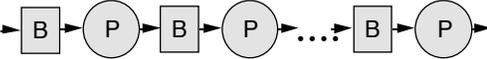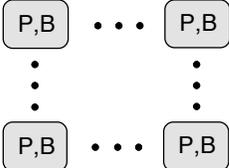- **Nearly all modern FFT processors use common-factor, radix-2^m processors**

Processor	Architecture
LSI, L64280	radix-2
Plessey, PDSP16510A	radix-4
Dassault Electronique	radix-4
Cobra, Colorado State	radix-4
CNET, E. Bidet	radix-2,4

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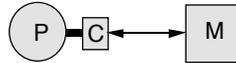- **Conclusion**

Common FFT Architectures

- **Single memory**

  P ⟷ M

- **Dual memory**
  (ping-pong)

  M ⟷ P ⟷ M

- **Pipelined**
  - Log$_r$ N stages

  B → P → B → P → . . . → B → P →

- **Array**

  P,B • • • P,B

  P,B • • • P,B

Cached Memory

- **Small cache used to hold frequently-used data**

- **Cache size** $C = 2^{\left\lceil \log_2 \sqrt[E]{N} \right\rceil}$
  - ◆ E = Number of "Epochs" or passes through the data
- **Partition processor based on activity**
  - ◆ High activity: processor, cache
  - ◆ Low activity: main memory
  - ◆ Reduce leakage in low activity portion by increasing V_t

Cached Memory Algorithm

- **Previous Caching algorithms**
  - ◆ Gentleman and Sande, 1966
  - ◆ Singleton, 1967
  - ◆ Brenner, 1969
  - ◆ Rabiner and Gold, 1975
  - ◆ Bailey, 1990
  - ◆ Carlson, 1990
- **Processor's view: Fast, large memory**
- **Memory's view: Very large radix processor**
  - ◆ Similar to Radix $N^{1/E}$
- **Especially good algorithm for large N**

Radix-2 Decimation-in-time Dataflow
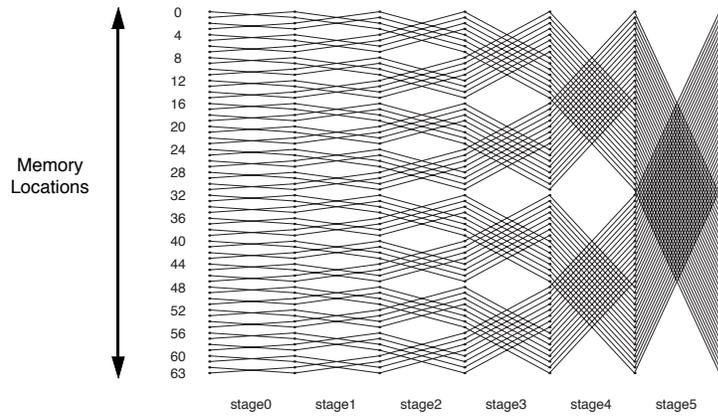
Radix-2 Decimation-in-time Cached FFT Dataflow Diagram
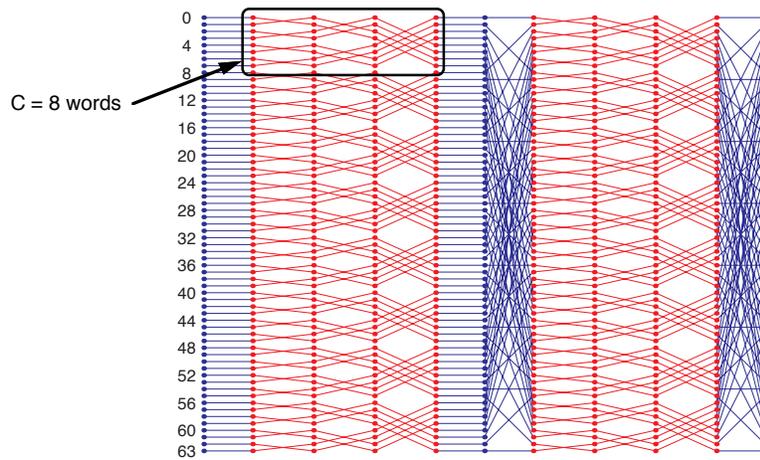
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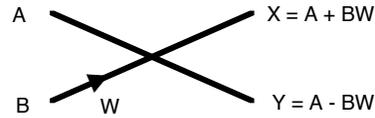- **The Spiffee Processor**
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Design Goals

- **1024 complex point FFT processor**
- **Single-chip**
- **Deep pipelining**
- **Functional and good performance at low Vdd (400mV), low V_t (0V)**
- **Robust circuits to operate in a possibly noisy environment**

Algorithm

- **Radix-2**
  - One butterfly / cycle
    - 1 complex multiply and 2 complex add/subtracts
      ⇨ 4 multiplies and 6 adds

- **Cached FFT Algorithm**
  - Mem = 1024 words x 36 bits
  - C = $1024^{1/2}$ = 32 words x 40 bits

- **Non-iterative datapath**
  - High usage ⇨ good area efficiency

A X = A + BW

B W Y = A - BW

Block Diagram

- **SRAM Arrays (8)**
  - Hierarchical bitlines, 6T cells, 128 x 36-bit

- **Caches (4)**
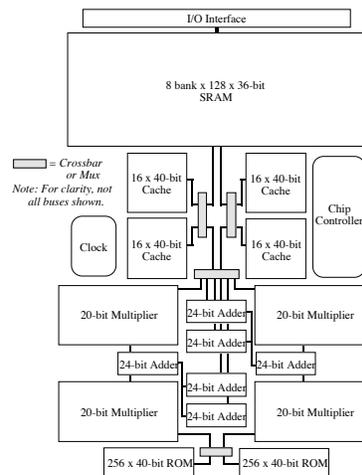 - Dual-ported, 10T cells, 16 x 40-bit

- **Multipliers (4)**
  - 20-bit x 20-bit, 24-bit product 2's complement

- **Adder/Subtractors (6)**
  - 24-bit, CLA-Ripple

- **ROMs (2)**
  - Hierarchical bitlines, 256 x 40-bit

I/O Interface

8 bank x 128 x 36-bit SRAM

= Crossbar or Mux
Note: For clarity, not all buses shown.

16 x 40-bit Cache
16 x 40-bit Cache
Chip Controller
Clock
16 x 40-bit Cache
16 x 40-bit Cache

20-bit Multiplier
24-bit Adder
20-bit Multiplier
24-bit Adder
24-bit Adder
24-bit Adder
20-bit Multiplier
24-bit Adder
20-bit Multiplier
24-bit Adder

256 x 40-bit ROM
256 x 40-bit ROM

Pipeline Diagram

● **9-stage pipeline**

MEM RD	CROSSB RD	MULT1	MULT2	MULT3	ADD/SUB CMULT	ADD/SUB XY	CROSSB WR	MEM WR
A B W	—		B x W			X = A+BW Y = A-BW	—	X Y

● **Throughput of one complex butterfly per cycle**
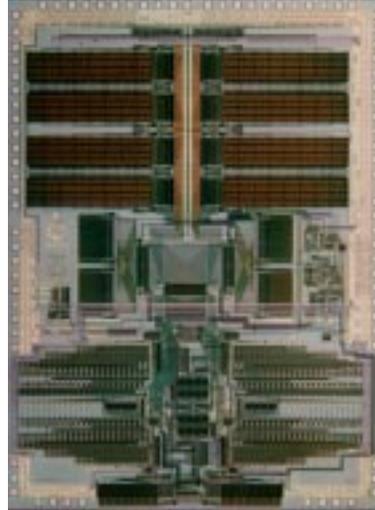● **Stall 1 out of every 80 cycles due to Read-after-Write hazard**

Clocking

● **Single-phase clock**
● **Each flip-flop contains minimum-size local clock buffers**
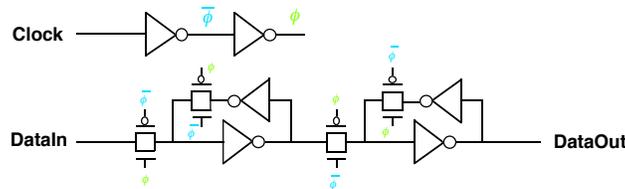
● **Selectable on-chip programmable oscillator or external clock**

Spiffee

- **460,000 transistors**
- **5.985mm x 8.204mm (0.7μm design rules, L_{poly}=0.6μm)**
- **V_{tn} = 0.63V, V_{tp} = -0.88V**
- **1 poly, 3 metal layers**
- **Full custom**
- **650-element scan path**

Energy-Efficiency Comparison

- **17 times more efficient @ 1.1V**

Processor	Year	CMOS Tech (μm)	Datapath width (bits)	Supply Voltage (V)	1024-pt Exec Time (μsec)	Power (mW)	Clock (MHz)	Number of chips	Adjusted transforms / mJ *
LSI, L64280	1990	1.5	20	5	26	20,000	40	20	11
Plessey, PDSP16510A	1989	1.4	16	5	96	3,000	40	1	12
Dassault Electronique	1990	1	12	5	128	12,000	20	6	1
Texas Mem Sys, TM-66	-	0.8	32	5	65	7,000	50	3	16
Cobra, Colorado State	1994	0.75	23	5	9.5	7,700	40	16	**49**
Sicom, SNC960A	1996	0.6	16	5	20	2,500	65	1	29
CNET, E. Bidet	1994	0.5	10	3.3	51	330	20	1	30
Spiffee1	1995	0.7	20	1.1	330	9.5	16	1	**819**
Spiffee1	1995	0.7	20	3.3	30	845	173	1	101

$$* \quad \text{Adjusted\_transforms\_per\_mJ} \quad = \quad \frac{\text{Tech} * ((DPath*2/3) + (DPath^2*1/3))_{10}}{\text{Power} * \text{Exec\_Time}}$$
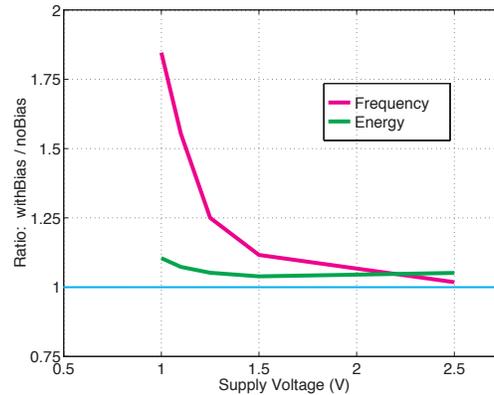
Clock Speed Comparison

● **Caching algorithm allows deep pipelining and high performance**
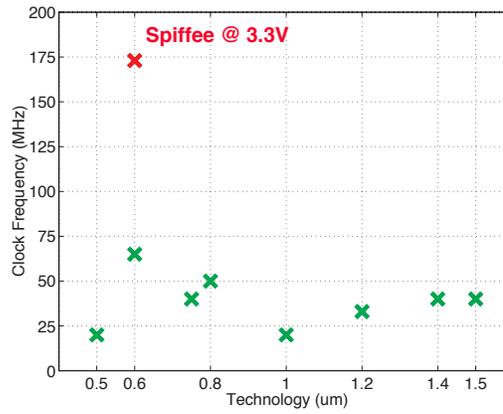
Energy x Time
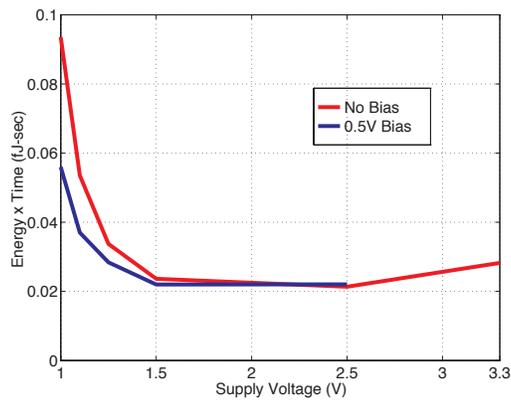
Improvements Using
Well/Substrate Biasing

Estimated Performance in a
Low-V_t Process

- **Portions of Spiffee were fabricated in a low-V_t 0.8μm process with L_{poly}=0.26μm and included an identical programmable oscillator**

  High Vt OSC

  Low Vt OSC
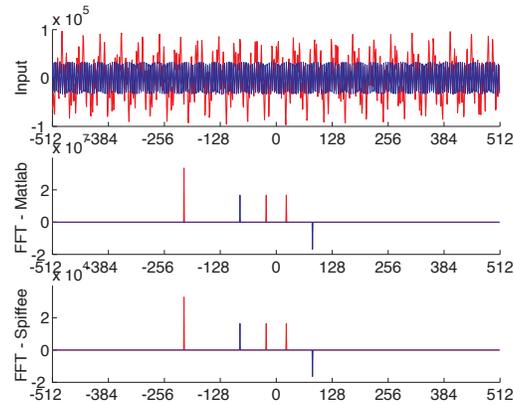
- **Measurements predict at Vdd=0.4V:**
  - ◆ 57MHz @ less than 9.7mW
  - ◆ 1024-pt FFT in 93μsec
  - ◆ More than **66** times more efficient than previously best known

Example Input - Output

- **Input = cos(2π*23/N) + sin(2π*83/N) + cos(2π*211/N) - j sin(2π*211/N)**


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Contributions

- **FFT caching algorithm for high energy-efficiency**
- **Hierarchical-bitline SRAM and ROM memories for low-V_t operation**
- **Design of a 1024-point, single-chip, full-custom, FFT processor**
  - Fabricated and fully functional on first-pass silicon
  - 17 times more efficient than the previously most efficient known
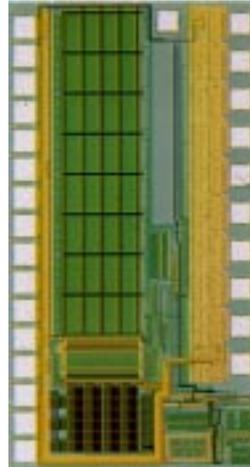 - Functional at 173MHz @ 3.3V

ULPAcc

- **16-word x 24-bit dual-ported memory**
- **24-bit accumulator**
- **On-chip controller and oscillator**
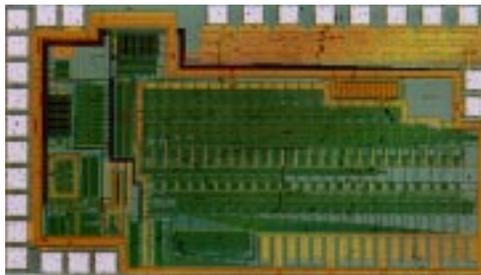- **11,700 transistors**
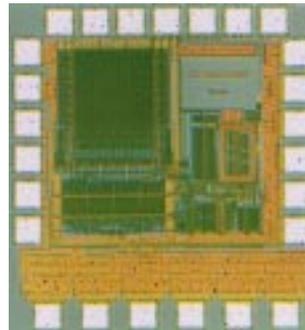
Srambb

- **128-word x 36-bit array**

- **On-chip controller, buffers, and oscillator**

- **46,200 transistors**

Multbb

- **20-bit x 20-bit multiplier**
- **On-chip controller, buffers, and oscillator**
- **28,500 transistors**

Other Projects and Publications

- **Memory optimizing simulator**
- **MCM Test Chip**
- **Publications**
  - B. M. Baas, "An Energy-Efficient Single-Chip FFT Processor," Proceedings of the 1996 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, 13-15 June 1996.
  - J. B. Burr, Z. Chen, B. M. Baas; "Stanford Ultra-Low-Power CMOS Technology and Applications," in Low-power HF Microelectronics, a Unified Approach. Stevage, UK: The Institution of Electrical Engineers, 1996.
  - B. M. Baas, "An Energy-Efficient FFT Processor Architecture," StarLab Technical Report NGT-70340-1994-1, January 25, 1994.
  - B. M. Baas, "A Pipelined Memory System For an Interleaved Processor," StarLab Technical Report NSF-GF-1992-1, June 18, 1992.

Future Work

- **Investigate multiple datapath/cache pair systems**

- **Investigate multiple processor systems**

- **Modify Spiffee to be usable in a system**

- **Possible commercialization**

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- ◆ Parents and family
- ◆ Advisors and mentors
  - ■ Prof. Len Tyler, Prof. Kunle Olukotun, Prof. Allen Peterson, Jim Burr, Masataka Matsui
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